

# J309, J310

Preferred Device

## JFET VHF/UHF Amplifiers

### N-Channel — Depletion

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

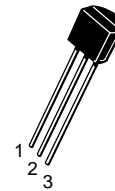
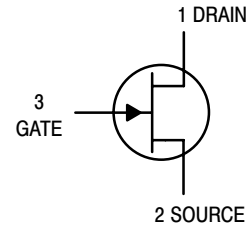
Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Gate-Source Voltage	$V_{GS}$	25	Vdc
Forward Gate Current	$I_{GF}$	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above = $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/°C
Junction Temperature Range	$T_J$	-65 to +125	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



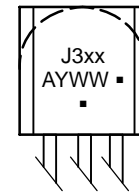
ON Semiconductor®

<http://onsemi.com>



TO-92  
CASE 29-11  
STYLE 5

#### MARKING DIAGRAM



J3xx = Device Code  
xx = 09 or 10  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# J309, J310

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Gate–Source Breakdown Voltage ( $I_G = -1.0 \mu\text{Adc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	-25	-	-	Vdc
Gate Reverse Current ( $V_{GS} = -15 \text{Vdc}$ , $V_{DS} = 0$ , $T_A = 25^\circ\text{C}$ ) ( $V_{GS} = -15 \text{Vdc}$ , $V_{DS} = 0$ , $T_A = +125^\circ\text{C}$ )	$I_{GSS}$	-	-	-1.0 -1.0	nAdc $\mu\text{Adc}$
Gate Source Cutoff Voltage ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 1.0 \text{nAdc}$ )	$V_{GS(off)}$	-1.0 -2.0	-	-4.0 -6.5	Vdc
<b>ON CHARACTERISTICS</b>					
Zero–Gate–Voltage Drain Current <sup>(1)</sup> ( $V_{DS} = 10 \text{Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	12 24	-	30 60	mAdc
Gate–Source Forward Voltage ( $V_{DS} = 0$ , $I_G = 1.0 \text{mAdc}$ )	$V_{GS(f)}$	-	-	1.0	Vdc
<b>SMALL–SIGNAL CHARACTERISTICS</b>					
Common–Source Input Conductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{MHz}$ )	$\text{Re}(y_{is})$	-	0.7 0.5	-	mmhos
Common–Source Output Conductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{MHz}$ )	$\text{Re}(y_{os})$	-	0.25	-	mmhos
Common–Gate Power Gain ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{MHz}$ )	$G_{pg}$	-	16	-	dB
Common–Source Forward Transconductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{MHz}$ )	$\text{Re}(y_{fs})$	-	12	-	mmhos
Common–Gate Input Conductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{MHz}$ )	$\text{Re}(y_{ig})$	-	12	-	mmhos
Common–Source Forward Transconductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 1.0 \text{kHz}$ )	$g_{fs}$	10000 8000	-	20000 18000	$\mu\text{mhos}$
Common–Source Output Conductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 1.0 \text{kHz}$ )	$g_{os}$	-	-	250	$\mu\text{mhos}$
Common–Gate Forward Transconductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 1.0 \text{kHz}$ )	$g_{fg}$	-	13000 12000	-	$\mu\text{mhos}$
Common–Gate Output Conductance ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 1.0 \text{kHz}$ )	$g_{og}$	-	100 150	-	$\mu\text{mhos}$
Gate–Drain Capacitance ( $V_{DS} = 0$ , $V_{GS} = -10 \text{Vdc}$ , $f = 1.0 \text{MHz}$ )	$C_{gd}$	-	1.8	2.5	pF
Gate–Source Capacitance ( $V_{DS} = 0$ , $V_{GS} = -10 \text{Vdc}$ , $f = 1.0 \text{MHz}$ )	$C_{gs}$	-	4.3	5.0	pF
<b>FUNCTIONAL CHARACTERISTICS</b>					
Equivalent Short–Circuit Input Noise Voltage ( $V_{DS} = 10 \text{Vdc}$ , $I_D = 10 \text{mAdc}$ , $f = 100 \text{Hz}$ )	$\bar{e}_n$	-	10	-	$\text{nV}/\sqrt{\text{Hz}}$

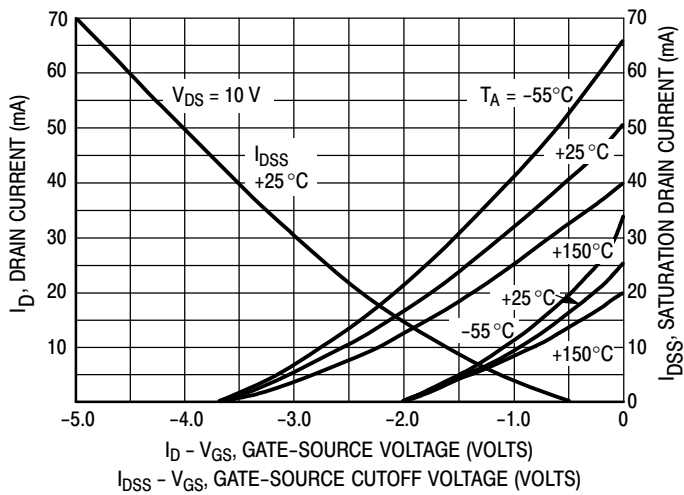
1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 3.0\%$ .

# J309, J310

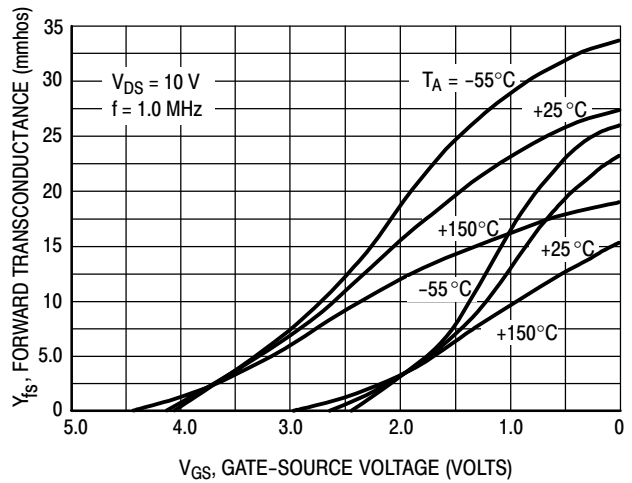
## ORDERING INFORMATION

Device	Package	Shipping†
J309	TO-92	1000 Units / Bulk
J309G	TO-92 (Pb-Free)	
J310	TO-92	1000 Units / Bulk
J310G	TO-92 (Pb-Free)	
J310RLRP	TO-92	2000 Units / Tape & Ammo Box
J310RLRPG	TO-92 (Pb-Free)	
J310ZL1	TO-92	2000 Units / Tape & Ammo Box
J310ZL1G	TO-92 (Pb-Free)	

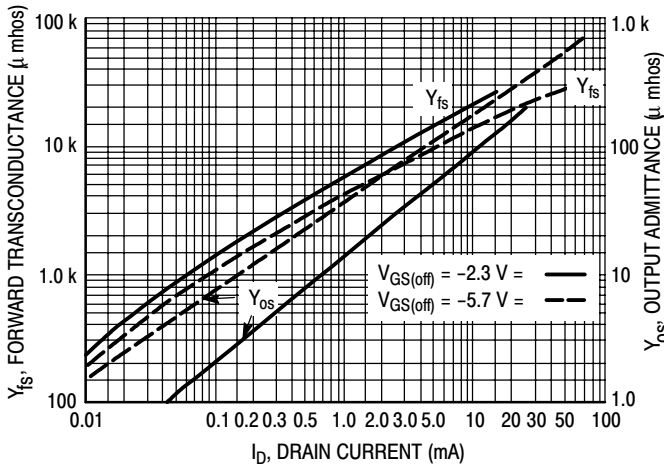
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



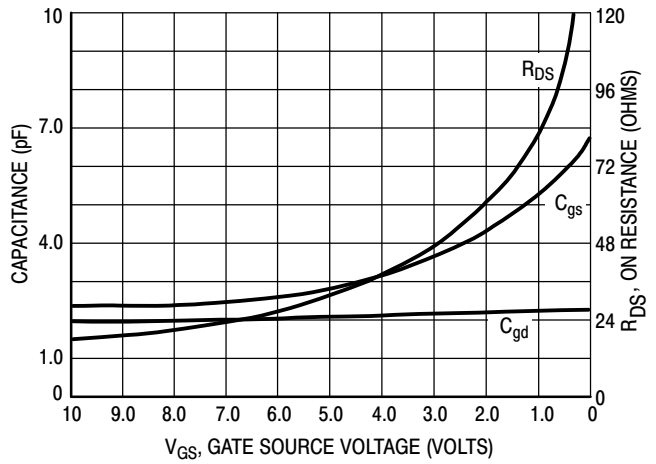
**Figure 1. Drain Current and Transfer Characteristics versus Gate-Source Voltage**



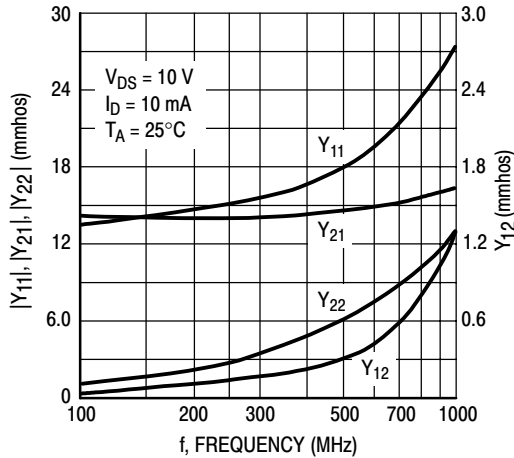
**Figure 2. Forward Transconductance versus Gate-Source Voltage**



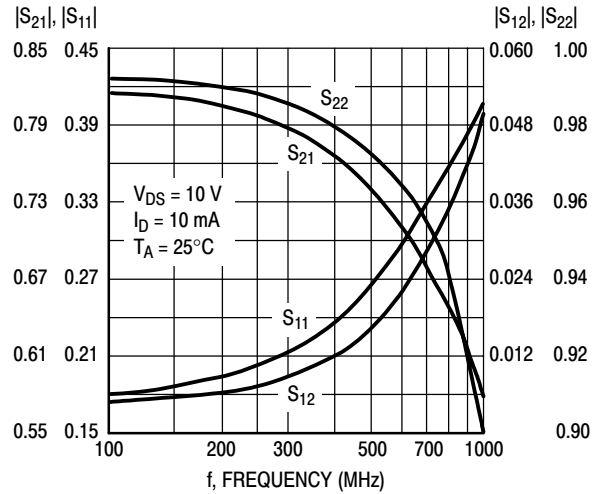
**Figure 3. Common-Source Output Admittance and Forward Transconductance versus Drain Current**



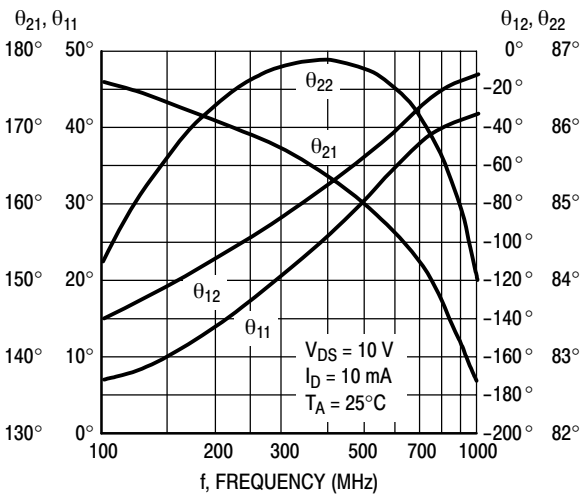
**Figure 4. On Resistance and Junction Capacitance versus Gate-Source Voltage**



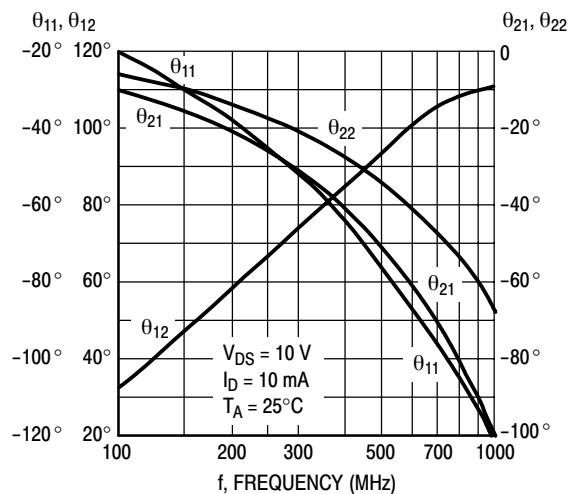
**Figure 5. Common-Gate Y Parameter Magnitude versus Frequency**



**Figure 6. Common-Gate S Parameter Magnitude versus Frequency**



**Figure 7. Common-Gate Y Parameter Phase-Angle versus Frequency**



**Figure 8. S Parameter Phase-Angle versus Frequency**

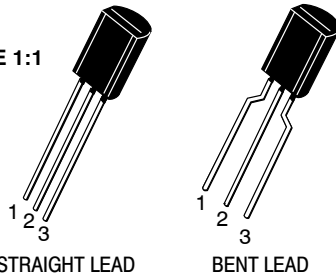
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

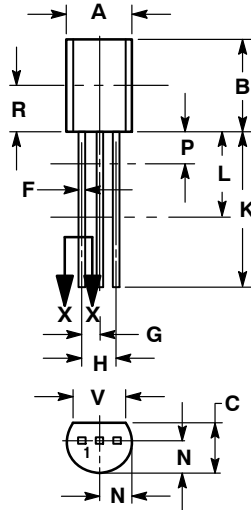


TO-92 (TO-226) 1 WATT  
CASE 29-10  
ISSUE A

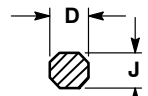
DATE 08 MAY 2012

STRAIGHT LEAD

BENT LEAD



STRAIGHT LEAD

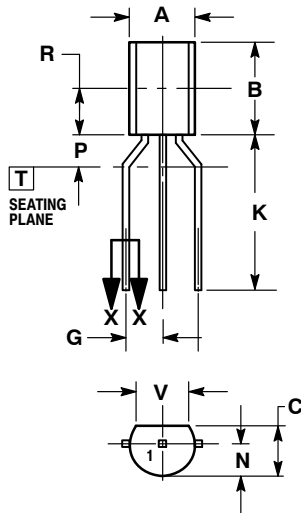


SECTION X-X

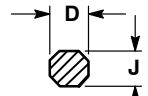
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X-X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
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C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

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CASE 29-10  
ISSUE A**

DATE 08 MAY 2012

- |   |  |  |   |   |
|---|--|--|---|---|
| <p>STYLE 1:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. COLLECTOR</p>             | <p>STYLE 2:<br/>PIN 1. BASE<br/>2. EMITTER<br/>3. COLLECTOR</p>                | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. ANODE<br/>3. CATHODE</p>               | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. CATHODE<br/>3. ANODE</p>            | <p>STYLE 5:<br/>PIN 1. DRAIN<br/>2. SOURCE<br/>3. GATE</p>            |
| <p>STYLE 6:<br/>PIN 1. GATE<br/>2. SOURCE &amp; SUBSTRATE<br/>3. DRAIN</p>  | <p>STYLE 7:<br/>PIN 1. SOURCE<br/>2. DRAIN<br/>3. GATE</p>                     | <p>STYLE 8:<br/>PIN 1. DRAIN<br/>2. GATE<br/>3. SOURCE &amp; SUBSTRATE</p> | <p>STYLE 9:<br/>PIN 1. BASE 1<br/>2. EMITTER<br/>3. BASE 2</p>            | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. GATE<br/>3. ANODE</p>          |
| <p>STYLE 11:<br/>PIN 1. ANODE<br/>2. CATHODE &amp; ANODE<br/>3. CATHODE</p> | <p>STYLE 12:<br/>PIN 1. MAIN TERMINAL 1<br/>2. GATE<br/>3. MAIN TERMINAL 2</p> | <p>STYLE 13:<br/>PIN 1. ANODE 1<br/>2. GATE<br/>3. CATHODE 2</p>           | <p>STYLE 14:<br/>PIN 1. EMITTER<br/>2. COLLECTOR<br/>3. BASE</p>          | <p>STYLE 15:<br/>PIN 1. ANODE 1<br/>2. CATHODE<br/>3. ANODE 2</p>     |
| <p>STYLE 16:<br/>PIN 1. ANODE<br/>2. GATE<br/>3. CATHODE</p>                | <p>STYLE 17:<br/>PIN 1. COLLECTOR<br/>2. BASE<br/>3. EMITTER</p>               | <p>STYLE 18:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. NOT CONNECTED</p>      | <p>STYLE 19:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE</p>              | <p>STYLE 20:<br/>PIN 1. NOT CONNECTED<br/>2. CATHODE<br/>3. ANODE</p> |
| <p>STYLE 21:<br/>PIN 1. COLLECTOR<br/>2. EMITTER<br/>3. BASE</p>            | <p>STYLE 22:<br/>PIN 1. SOURCE<br/>2. GATE<br/>3. DRAIN</p>                    | <p>STYLE 23:<br/>PIN 1. GATE<br/>2. SOURCE<br/>3. DRAIN</p>                | <p>STYLE 24:<br/>PIN 1. EMITTER<br/>2. COLLECTOR/ANODE<br/>3. CATHODE</p> | <p>STYLE 25:<br/>PIN 1. MT 1<br/>2. GATE<br/>3. MT 2</p>              |
| <p>STYLE 26:<br/>PIN 1. V<sub>CC</sub><br/>2. GROUND 2<br/>3. OUTPUT</p>    | <p>STYLE 27:<br/>PIN 1. MT<br/>2. SUBSTRATE<br/>3. MT</p>                      | <p>STYLE 28:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE</p>               | <p>STYLE 29:<br/>PIN 1. NOT CONNECTED<br/>2. ANODE<br/>3. CATHODE</p>     | <p>STYLE 30:<br/>PIN 1. DRAIN<br/>2. GATE<br/>3. SOURCE</p>           |
| <p>STYLE 31:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE</p>                 | <p>STYLE 32:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER</p>               | <p>STYLE 33:<br/>PIN 1. RETURN<br/>2. INPUT<br/>3. OUTPUT</p>              | <p>STYLE 34:<br/>PIN 1. INPUT<br/>2. GROUND<br/>3. LOGIC</p>              | <p>STYLE 35:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER</p>      |

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