





40V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(on)}	I _D T _A = 25°C
-40V	51mΩ @ V _{GS} = -10V	-10.5A
	85mΩ @ V _{GS} = -4.5V	-8.4A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance (R_{DS(on)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- DC-DC Converters
- Power management functions

Features and Benefits

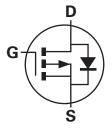
- 100% Unclamped Inductive Switch (UIS) test in production
- Low on-resistance
- Fast switching speed
- "Green" component and RoHS compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: TO252
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.33 grams (approximate)







Equivalent Circuit

Ordering Information (Notes 1 & 2)

Product	Grade	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP4051LK3-13	Commercial	P4051L	13	16	2,500
DMP4051LK3Q-13	Automotive	P4051L	13	16	2,500

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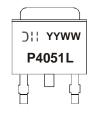
Pin-Out

S

Notes:

- 1. Diodes, Inc. defines "Green" products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.'s "Green" Policy can be found on our website. For packaging details, go to our website.
- 2. Products with Q-suffix are automotive grade. Automotive products are electrical and thermal the same as the commercial, except where specified.

Marking Information



⊃¦¦ = Manufacturer's Marking P4051L = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 09 = 2009)WW = Week (01 - 53)





Maximum Ratings $@T_A = 25^{\circ}C$ unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source voltage			V_{DSS}	-40	V
Gate-Source voltage (Note 3)		V _{GS}	±20	V	
Single Pulsed Avalanche Energy (Note 9)		(Note 9)	E _{AS}	50	mJ
Single Pulsed Avalanche Current (Note 9)		I _{AS}	20.3	A	
		(Note 5)		-10.5	
Continuous Drain current	$V_{GS} = 10V$	$T_A = 70^{\circ}C \text{ (Note 5)}$	I_{D}	-8.40	Α
		(Note 4)		-7.2	
Pulsed Drain current	$V_{GS} = 10V$	(Note 6)	I _{DM}	-28.9	Α
Continuous Source current (Body diode) (Note 5)		I _S	-10.1	Α	
Pulsed Source current (Body diode) (Note 5)		I _{SM}	-28.9	A	

Thermal Characteristics @TA = 25°C unless otherwise specified

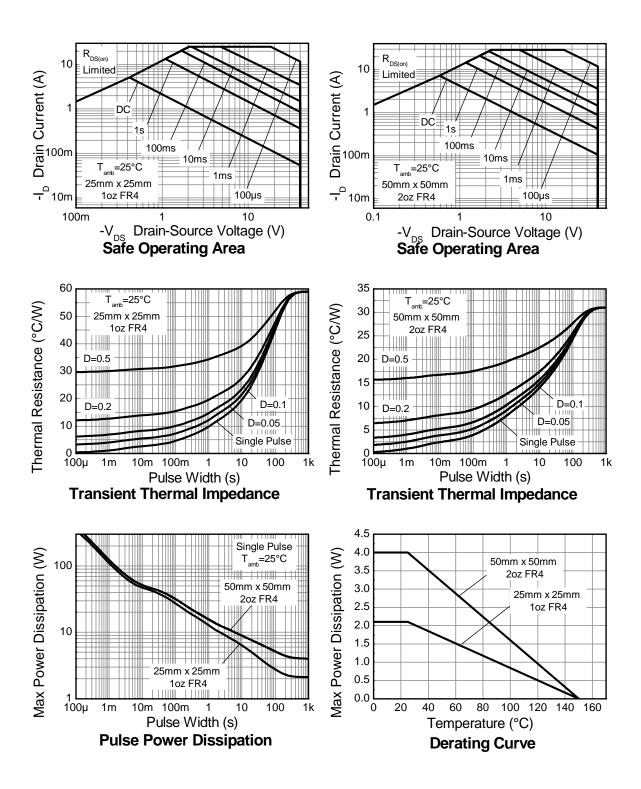
Characteristic	Symbol	Value	Unit	
	(Note 4)		4.18 33.4	
Power dissipation Linear derating factor	(Note 5)	P _D	8.9 71.4	W mW/°C
	(Note 7)		2.14 17.1	
	(Note 4)		29.9	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{ hetaJA}$	14.0	2011
	(Note 7)	Ť	58.4	°C/W
Thermal Resistance, Junction to Lead	(Note 8)	$R_{ heta JL}$	2.46	
Operating and storage temperature range	•	T _J , T _{STG}	-55 to 150	°C

Notes:

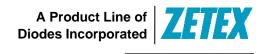
- 3. AEC-Q101 V_{GS} maximum is ±16V.
- 4. For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- 5. Same as note 4, except the device is measured at t ≤ 10 sec.
 6. Same as note 4, except the device is pulsed with D = 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
- 7. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- 8. Thermal resistance from junction to solder-point (at the end of the drain lead).
 9. UIS in production with L = 100μH, V_{DD} = -40V.



Thermal Characteristics







Electrical Characteristics @TA = 25°C unless otherwise specified

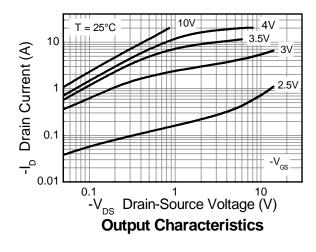
Characteristic	Symbol	Min	Тур	Max	Unit	Test Co	ndition
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	-40	_	_	V	$I_D = -250 \mu A, V_{GS}$	= 0V
Zero Gate Voltage Drain Current	I _{DSS}	_	_	-0.5	μΑ	$V_{DS} = -40V, V_{GS}$	= 0V
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS}$	= 0V
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(th)}	-1.0		-3.0	V	$I_D = -250 \mu A, V_{DS}$	= V _{GS}
Static Drain Source On Decistones (Note 10)			0.041	0.051	Ω	$V_{GS} = -10V, I_{D} = -$	-12A
Static Drain-Source On-Resistance (Note 10)	R _{DS (ON)}	_	0.059	0.085	12	$V_{GS} = -4.5V, I_{D} =$	-8A
Forward Transconductance (Notes 10 & 11)	9fs	_	16.6	_	S	$V_{DS} = -15V, I_{D} = -15V$	-12A
Diode Forward Voltage (Note 10)	V_{SD}	_	-0.98	-1.2	V	$I_S = -12A, V_{GS} = 0$	VO
Reverse recovery time (Note 11)	t _{rr}		138	_	ns	I _S = -12A, di/dt = 100A/μs	
Reverse recovery charge (Note 11)	Qrr	_	841	_	nC		
DYNAMIC CHARACTERISTICS (Note 11)							
Input Capacitance	Ciss	_	674	_	pF	.,	0) /
Output Capacitance	Coss	_	115	_	pF	$V_{DS} = -20V, V_{GS} = -100$	= UV
Reverse Transfer Capacitance	C_{rss}	_	67.7	_	pF	71 = 1101112	
Total Gate Charge (Note 12)	Q_g	_	7.0	_	nC	$V_{GS} = -4.5V$	
Total Gate Charge (Note 12)	Q_g	_	14	_	nC	V _{DS} = -20V I _D = -12A	
Gate-Source Charge (Note 12)	Qgs	_	2.2	_	nC		
Gate-Drain Charge (Note 12)	Q_{gd}	_	3.7	_	nC		
Turn-On Delay Time (Note 12)	t _{D(on)}	_	2.3	_	ns	$V_{DD} = -20V, V_{GS} = -10V$ $I_{D} = -12A, R_{G} \cong 6.0\Omega$	
Turn-On Rise Time (Note 12)	t _r	_	14.1	_	ns		
Turn-Off Delay Time (Note 12)	t _{D(off)}	_	25.1	_	ns		
Turn-Off Fall Time (Note 12)	t _f	_	14.3	_	ns		

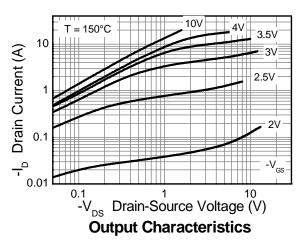
Notes:

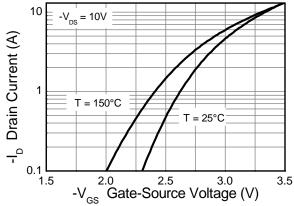
- 10. Measured under pulsed conditions. Pulse width $\leq 300 \mu s;$ duty cycle $\leq 2\%$
- 11. For design aid only, not subject to production testing.12. Switching characteristics are independent of operating junction temperatures.

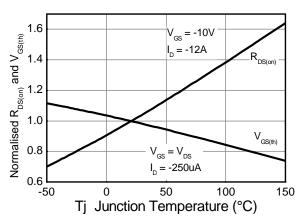


Typical Characteristics



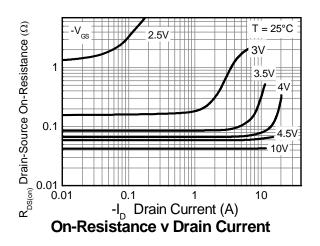


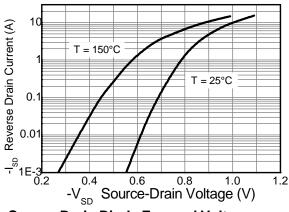




Typical Transfer Characteristics



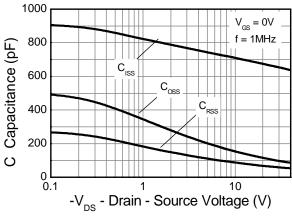




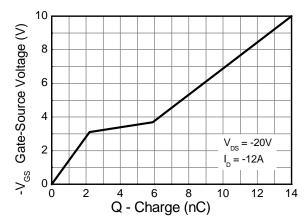
Source-Drain Diode Forward Voltage



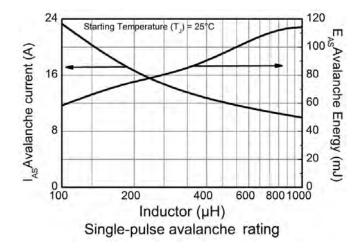
Typical Characteristics - continued





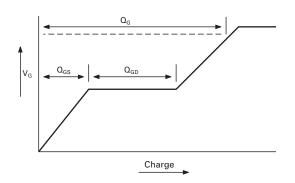


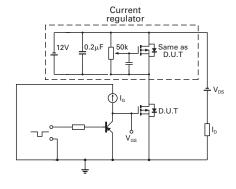
Gate-Source Voltage v Gate Charge





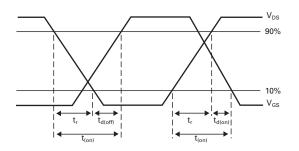
Test Circuits

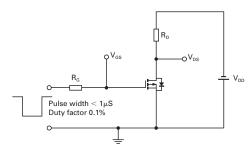




Basic gate charge waveform

Gate charge test circuit





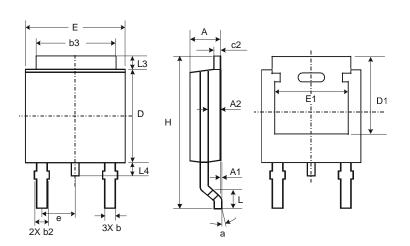
Switching time waveforms

Switching time test circuit



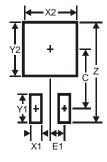


Package Outline Dimensions



TO252					
Dim	Min	Max	Тур		
Α	2.19	2.39	2.29		
A1	0.00	0.13	0.08		
A2	0.97	1.17	1.07		
b	0.64	0.88	0.783		
b2	0.76	1.14	0.95		
b3	5.21	5.46	5.33		
c2	0.45	0.58	0.531		
D	6.00	6.20	6.10		
D1	5.21	_	-		
е	_	_	2.286		
Ε	6.45	6.70	6.58		
E1	4.32	_	_		
Н	9.40	10.41	9.91		
L	1.40	1.78	1.59		
L3	0.88	1.27	1.08		
L4	0.64	1.02	0.83		
а	0°	10°	_		
All Dimensions in mm					

Suggested Pad Layout



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
С	6.9
E1	2.3





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