

SN74AUP1T08 Low Power, 1.8, 2.5, 3.3-V Input, 3.3-V CMOS Output, Single 2-Input Positive-AND Gate

1 Features

- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Single-Supply Voltage Translator
- Output Level Up to Supply V_{CC} CMOS Level
 - 1.8 V to 3.3 V (at $V_{CC} = 3.3$ V)
 - 2.5 V to 3.3 V (at $V_{CC} = 3.3$ V)
 - 1.8 V to 2.5 V (at $V_{CC} = 2.5$ V)
 - 3.3 V to 2.5 V (at $V_{CC} = 2.5$ V)
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial Power Down ($V_{CC} = 0$ V)
- Very Low Static Power Consumption: 0.1 μ A
- Very Low Dynamic Power Consumption: 0.9 μ A
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Pb-Free Packages Available: SC70 (DCK) 2 x 2.1 x 0.65 mm (Height 1.1 mm)
- More Gate Options Available at www.ti.com/littlelogic

2 Description

The SN74AUP1T08 performs the Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ with designation for logic-level translation applications with output referenced to supply V_{CC} .

AUP technology is the industry's lowest-power logic technology designed for use in extending battery-life in operating. All input levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply. This product also maintains excellent signal integrity (see [Figure 5-1](#) and [Figure 5-2](#)).

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of switching output level to connect to external controllers or processors.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T08 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74AUP1T08	SC70 (5)	2mm x 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (AND Gate)



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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2010) to Revision A (September 2020)	Page
• Added <i>Device Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

4 Pin Configuration and Functions

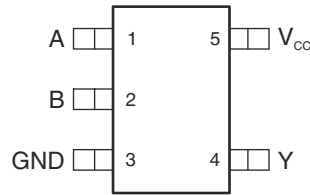


Figure 4-1. DCK Package 5-Pin SC70 Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±20 mA
	Continuous current through V _{CC} or GND			±50 mA
θ _{JA}	Package thermal impedance ⁽³⁾	DCK package		259 °C/W
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC 51-7.

5.2 Recommended Operating Conditions

See⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V		-3.1 mA
		V _{CC} = 3 V		-4 mA
I _{OL}	Low-level output current	V _{CC} = 2.3 V		3.1 mA
		V _{CC} = 3 V		4 mA
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.3 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
		3 V to 3.6 V	0.75		1.16	0.75	1.19	
V _{T-} Negative-going input threshold voltage		2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
		3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV _T Hysteresis (V _{T+} - V _{T-})		2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
		3 V to 3.6 V	0.25		0.56	0.15	0.56	
V _{OH}	I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1		V	
	I _{OH} = -2.3 mA	2.3 V	2.05		1.97			

5.3 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
	I _{OH} = -3.1 mA	3 V	1.9			1.85		
	I _{OH} = -2.7 mA		2.72			2.67		
	I _{OH} = -4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	2.3 V to 3.6 V				0.1		V
	I _{OL} = 2.3 mA	2.3 V				0.31		
	I _{OL} = 3.1 mA					0.44		
	I _{OL} = 2.7 mA	3 V				0.31		
	I _{OL} = 4 mA					0.44		
I _I	All inputs V _I = 3.6 V or GND	0 V to 3.6 V				0.1		μA
I _{off}	V _I or V _O = 0 V to 3.6 V	0 V				0.1		μA
ΔI _{off}	V _I or V _O = 3.6 V	0 V to 0.2 V				0.2		μA
I _{CC}	V _I = 3.6 V or GND, I _O = 0	2.3 V to 3.6 V				0.5		μA
ΔI _{CC}	One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , I _O = 0	2.3 V to 2.7 V				4		μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , I _O = 0	3 V to 3.6 V				12		
C _i	V _I = V _{CC} or GND	3.3 V	1.5					pF
C _o	V _O = V _{CC} or GND	3.3 V	3					pF

5.4 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

5.5 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_I = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

5.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

5.8 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

5.9 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

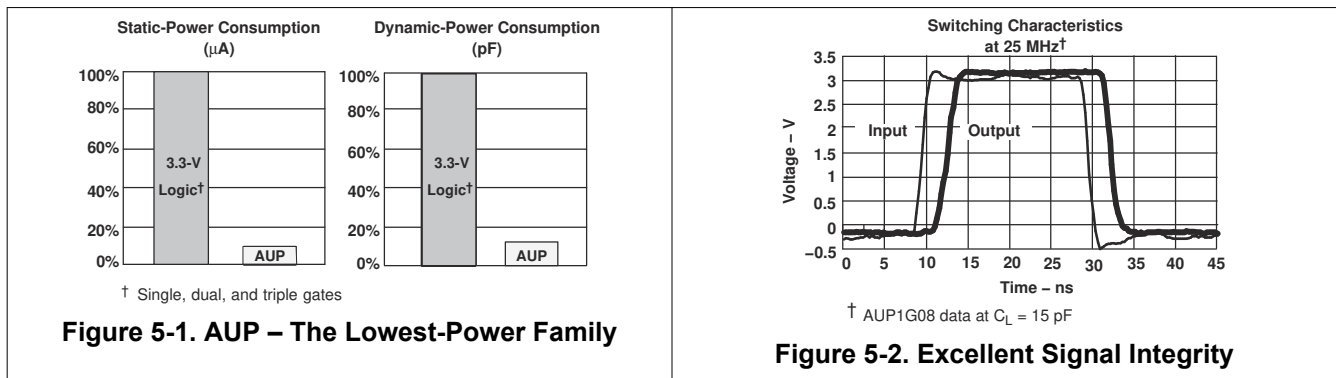
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

5.10 Operating Characteristics

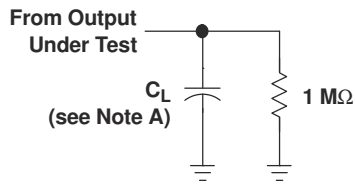
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

5.11 Typical Characteristics

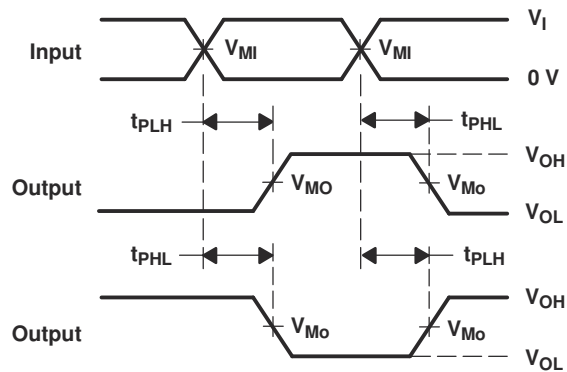


6 Parameter Measurement Information



LOAD CIRCUIT

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$, slew rate \geq 1 V/ns.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-1. Load Circuit And Voltage Waveforms

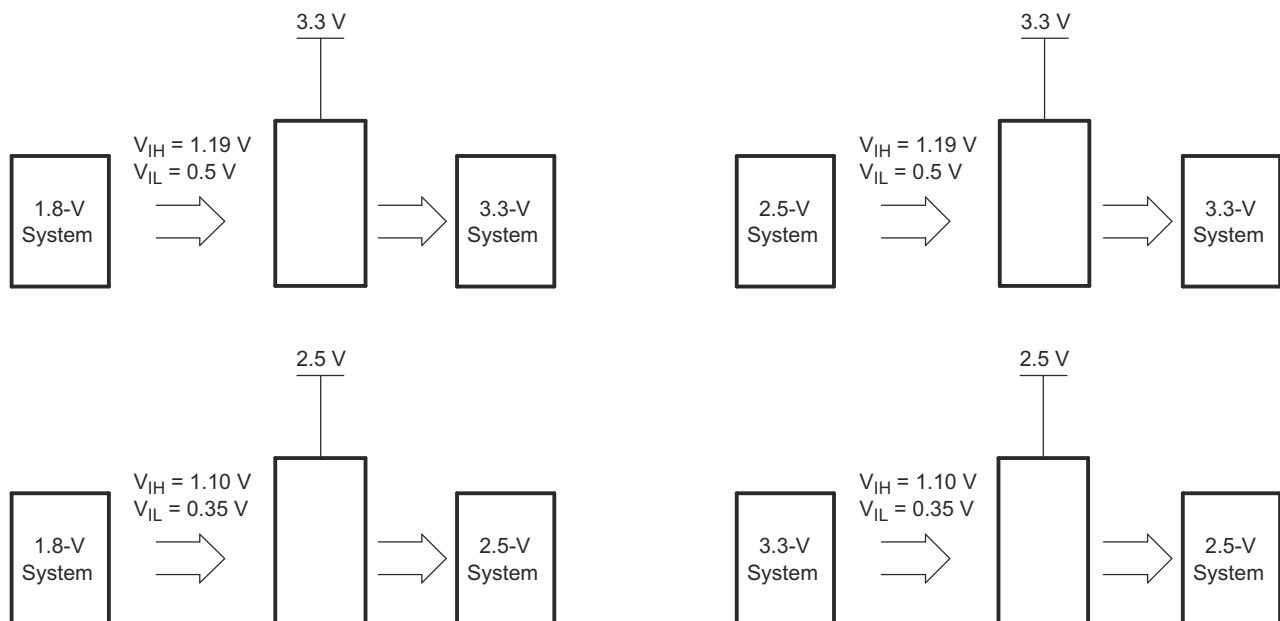


Figure 6-2. Typical Design Examples

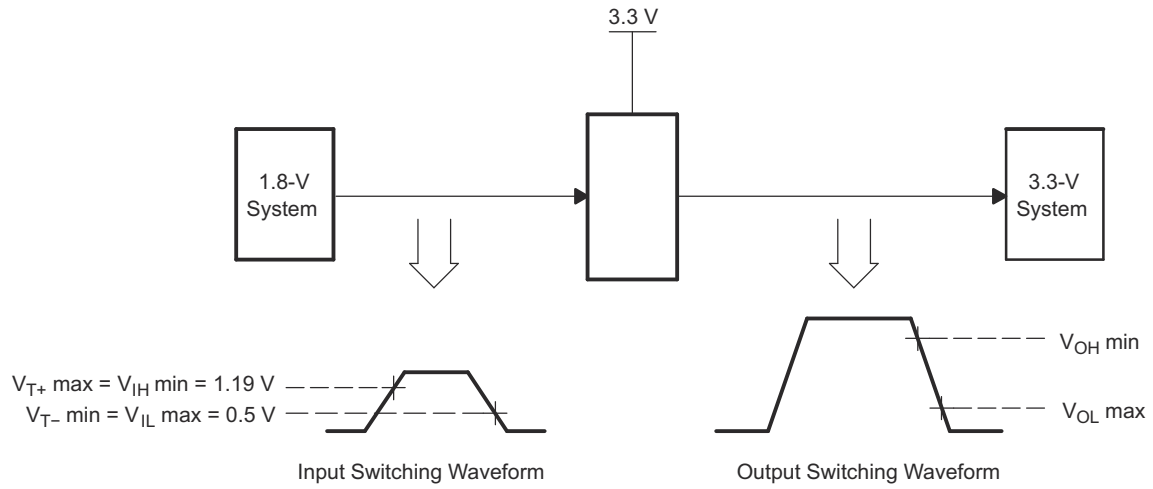


Figure 6-3. Switching Thresholds For 1.8-V To 3.3-V Translation

7 Detailed Description

7.1 Functional Block Diagram



Figure 7-1. Logic Diagram (AND Gate)

7.2 Device Functional Modes

Table 7-1 through Table 7-3 list the functional modes of the SN74AUP1T08 device.

Table 7-1. Function Table

INPUTS (Lower Level Input)		OUTPUT (V _{CC} CMOS)
A	B	Y
H	H	H
L	X	L
X	L	L

Table 7-2. Supply V_{CC} = 2.3 V To 2.7 V (2.5 V)

INPUTS V _{T+} max = V _{IH} min V _{T-} min = V _{IL} max		OUTPUT CMOS
A	B	Y
V _{IH} = 1.1 V V _{IL} = 0.35 V		V _{OH} = 1.85 V V _{OL} = 0.45 V

Table 7-3. Supply V_{CC} = 3 V To 3.6 V (3.3 V)

INPUTS V _{T+} max = V _{IH} min V _{T-} min = V _{IL} max		OUTPUT CMOS
A	B	Y
V _{IH} = 1.19 V V _{IL} = 0.5 V		V _{OH} = 2.55 V V _{OL} = 0.45 V

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T08DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	6EF	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

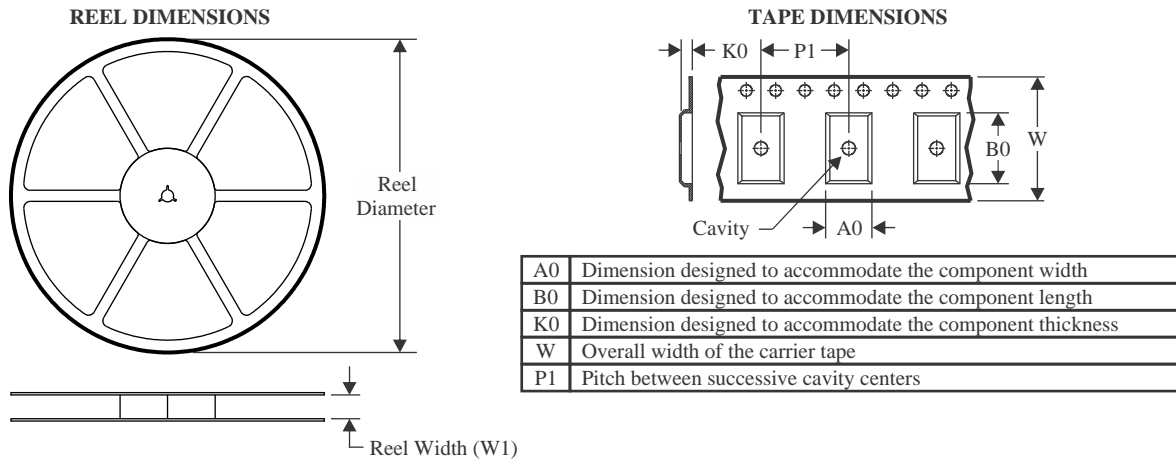
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

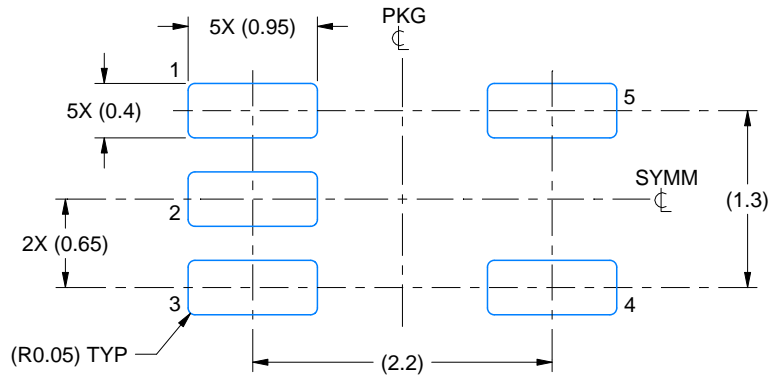
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

EXAMPLE BOARD LAYOUT

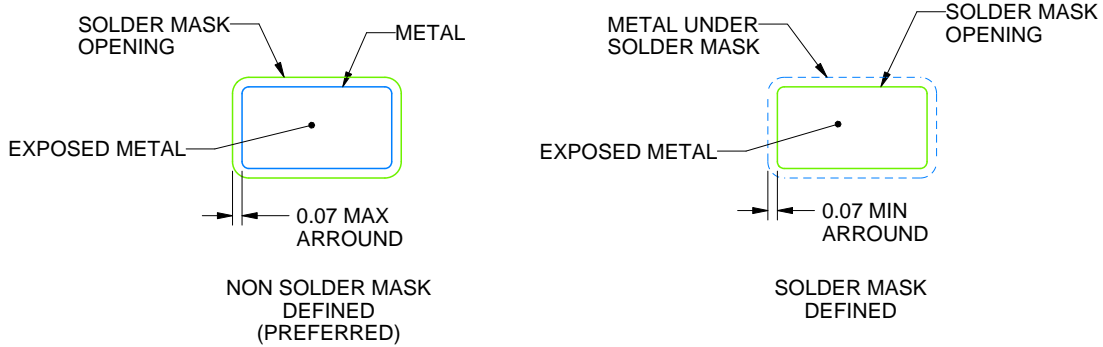
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

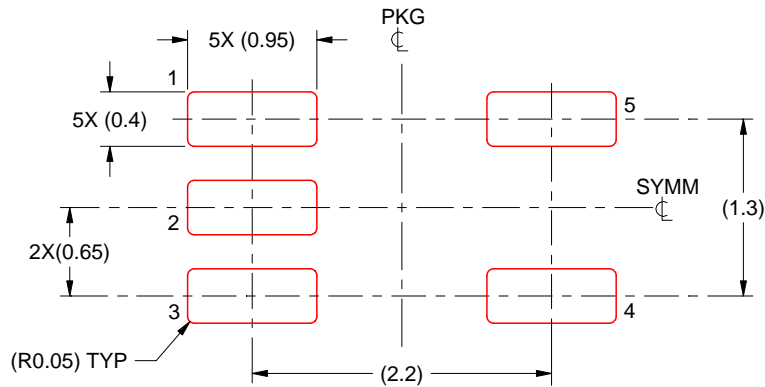
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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