Positive High-Voltage Power-Limiting Hotswap Controller With Analog Current Monitor Output

Check for Samples: TPS2492 , TPS2493

FEATURES

- 9-V to 80-V Operation
- High-Side Drive for External N-FET
- Programmable FET Power Limit
- Programmable Load Current Limit
- Programmable Fault Timer
- Load Current Monitor Output
- Power Good and Fault Outputs
- Enable/UV, OV Inputs
- Latch or Auto Restart After Fault
- EVM Available SLUU425
- Calculation Tool Available SLVC033

APPLICATIONS

- Server Backplanes
- Storage Area Networks (SAN)
- Medical Systems
- Plug-in Modules
- Base Stations

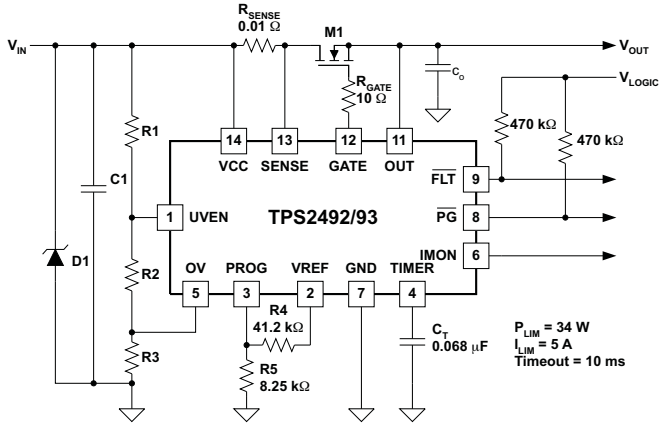
DESCRIPTION

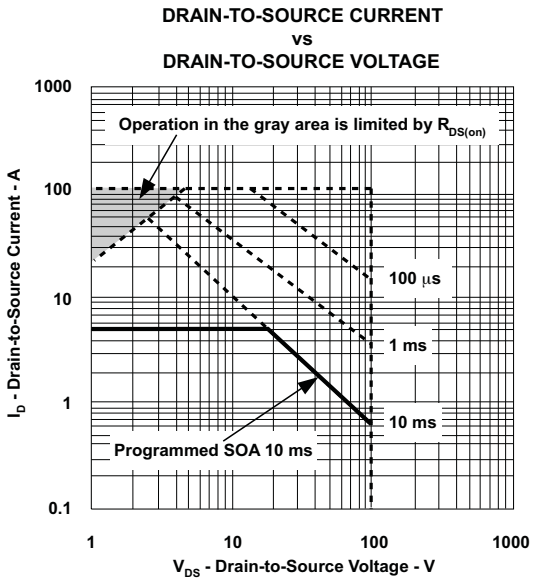
The TPS2492 and TPS2493 are easy-to-use, positive high voltage, 14-pin Hotswap Controllers that safely drive an external N-channel FET to control load current. The programmable power foldback protection ensures that the external FET operates inside its safe operating area (SOA) during overload conditions by controlling of power dissipation. The programmable current limit and fault timer ensure the supply, external FET, and load are not harmed by overcurrent. Features include inrush current limiting, controlled load turn-on, interfacing to down-stream DC-to-DC converters, and power feed protection.

The analog current monitor output provides a signal ready for sampling with an external A/D converter.

Additional features include programmable overvoltage and undervoltage shutdown, power-good for coordinating loads with inrush, and a fault indicator to indicate an over-current shutdown.

Typical Application Circuit





PRODUCT INFORMATION(1)

TEMPERATURE	FUNCTION	PACKAGE	PART NUMBER
-40°C to 125°C	Latched	PW14	TPS2492PW
	Retry		TPS2493PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over recommended T_J and voltages with respect to GND (unless otherwise noted)

		VALUE	UNIT
VCC, SENSE, UVEN, OUT	Input voltage range	-0.3 to 100	V
PROG, OV		-0.3 to 6	
VCC – SENSE	Differential voltage	-1.5 to 1.5	
GATE, $\overline{PG}$, $\overline{FLT}$	Output voltage range	-0.3 to 100	
TIMER, VREF, IMON		-0.3 to 6	
$\overline{PG}$, $\overline{FLT}$	Sink current	10	mA
PROG		2	
VREF	Source current	2	
HBM	ESD rating	2	kV
CDM		0.5	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		VALUE	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	116.4	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)	53.8	
ψ_{JT}	Junction-to-top characterization parameter(4)	1.4	
ψ_{JB}	Junction-to-board characterization parameter(5)	58.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

over recommended T_J and voltages with respect to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage range	9		80	V
PROG		0.4		4	
VREF	Sourcing current	0		1	mA
	capacitive loading	0		1000	pF
IMON	Sourcing current			1.9	mA
T_J	Junction operating temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS

9 V ≤ V_{VCC} ≤ 80 V, -40°C ≤ T_J ≤ 125°C, V_{TIMER} = 0 V and all outputs unloaded. Typical specification are at T_J = 25°C, V_{VCC} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (VCC)						
I_{VCC}	Enabled	V_{UVEN} = Hi, V_{SENSE} = V_{OUT} = V_{VCC}		665	1000	µA
I_{VCC}	Disabled	V_{UVEN} = Lo, V_{SENSE} = V_{VCC}, V_{OUT} = 0		120	250	µA
Input Supply UVLO (VCC)						
	V_{VCC} turn on	Rising		8.4	8.8	V
	Hysteresis		50	100	150	mV
Current Sense Input (SENSE)						
I_{SENSE}	Input bias current	V_{SENSE} = V_{OUT} = V_{VCC}		7.5	20	µA
Reference Voltage Output (VREF)						
V_{REF}	Reference voltage	0 ≤ I_{VREF} ≤ 1 mA	3.9	4	4.1	V
Power Limiting Input (PROG)						
I_{PROG}	Input bias current; device enabled; sourcing or sinking	0.4 ≤ V_{PROG} ≤ 4 V V_{UVEN} = 48 V			5	µA
R_{PROG}	Pull down resistance; device disabled	I_{PROG} = 200 µA; V_{UVEN} = 0 V		375	600	Ω
Power Limiting and Current Limiting (SENSE)						
	Current limit threshold $V_{(VCC-SENSE)}$ with power limiting trip	V_{PROG} = 2.4 V; V_{OUT} = 0 V; V_{VCC} = 48 V	17	25	33	mV
		V_{PROG} = 0.9 V; V_{OUT} = 30 V; V_{VCC} = 48 V	17	25	33	
	Current limit threshold $V_{(VCC-SENSE)}$ without power limiting trip	V_{PROG} = 4 V; V_{SENSE} = V_{OUT}	45	50	55	
t_{F_TRIP}	Large overload response time to GATE low	V_{PROG} = 4 V; V_{OUT} = V_{SENSE}; $V_{(VCC-SENSE)}$: 0 rising to 200 mV; $C_{(GATE-OUT)}$ = 2 nF; $V_{(GATE-OUT)}$ = 1 V			1.2	µs
TIMER Operation (TIMER)						
I_{SOURCE}	TIMER source current	V_{TIMER} = 0 V	17	27	36	µA
		V_{TIMER} = 0 V; T_J = 25°C	22	27	32	
I_{SINK}	TIMER sink current	V_{TIMER} = 5 V	1.5	2.7	3.7	
		V_{TIMER} = 5 V; T_J = 25°C	2.1	2.7	3.1	
V_{TIMER}	TIMER upper threshold		3.9	4 0	4.1	V
	TIMER lower reset threshold	TPS2492 only	0.96	1.00	1.04	
D_{RETRY}	Fault retry duty cycle	TPS2493 only	0.5	0.75	1	%
Fault Indicator Output ($\overline{FLT}$)						
	Low voltage (sinking)	$I_{\overline{FLT}}$ = 2 mA		0.1	0.25	V
		$I_{\overline{FLT}}$ = 4 mA		0.25	0.5	
$I_{LEAKAGE}$	Leakage current	$\overline{FLT}$ high impedance			10	µA
Under-Voltage and Enable Input (UVEN)						
V_{UVEN_H}	Threshold voltage	UVEN rising	1.31	1.35	1.39	V
		Hysteresis	80	100	120	mV
	Leakage current	V_{UVEN} = 48 V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

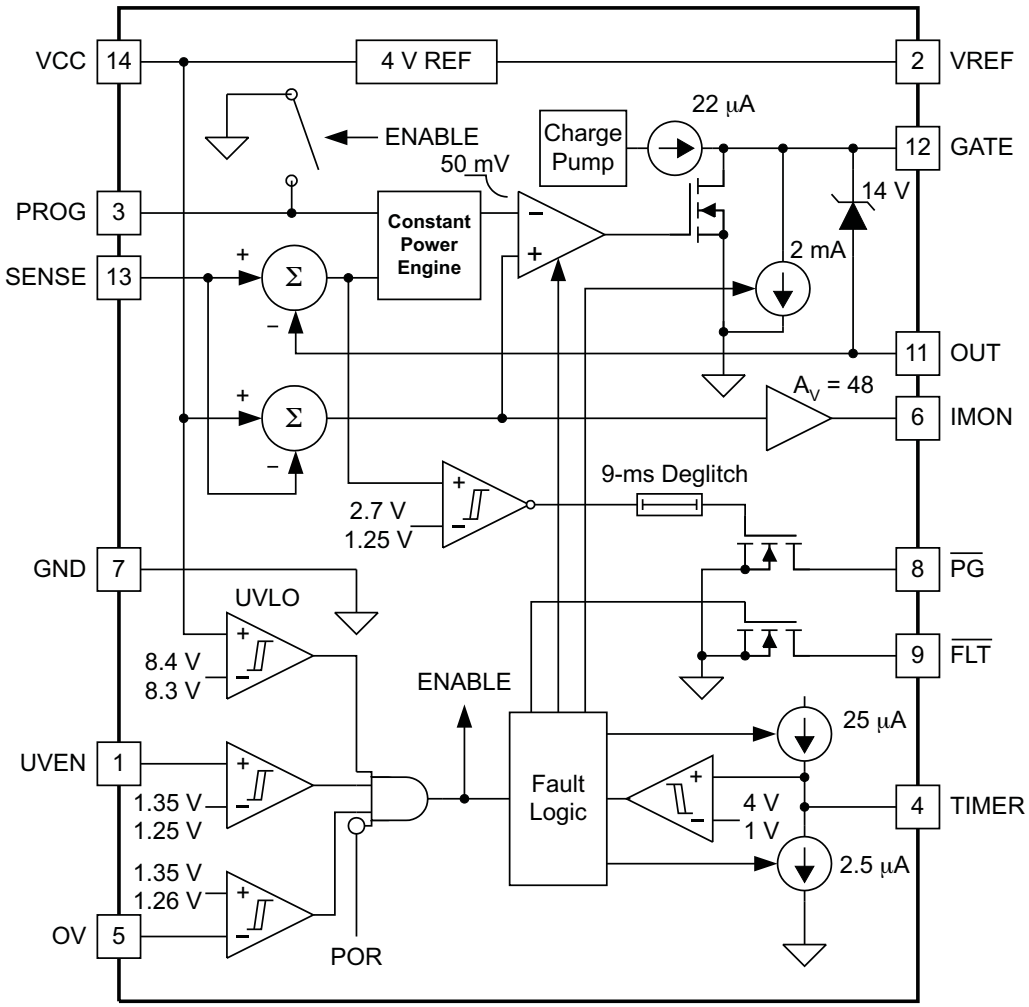
9 V ≤ V_{VCC} ≤ 80 V, -40°C ≤ T_J ≤ 125°C, V_{TIMER} = 0 V and all outputs unloaded. Typical specification are at T_J = 25°C, V_{VCC} = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Drive Output (GATE)						
I_{GATE}	GATE sourcing current	V_{SENSE} = V_{VCC}; $V_{(GATE-OUT)}$ = 7 V; V_{UVEN} = Hi	15	22	35	µA
	GATE sinking current	V_{UVEN} = Lo; V_{GATE} = V_{VCC}	1.8	2.4	2.8	mA
		V_{UVEN} = Hi; V_{GATE} = V_{VCC}; V_{VCC}- V_{SENSE} = 200 mV	75	125	250	
V_{GATE}	GATE output	V_{UVEN} = Hi, VCC = SENSE = OUT, measure V_{GATE} -V_{OUT}	12		16	V
t_{D_ON}	Propagation delay: UVEN going high to GATE output high	V_{UVEN} = 0 → 2.5 V, 50% of V_{UVEN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ		25	40	µs
t_{D_OFF}	Propagation delay: UVEN going low to GATE output low	V_{UVEN} = 2.5 V → 0 V, 50% of V_{UVEN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ, t_{FALL} < 0.1 µs		0.5	1	
t_{D_FAULT}	Propagation delay: TIMER expires to GATE output low	V_{TIMER}: 0 → 5 V, t_{RISE} < 0.1 µs. 50% of V_{TIMER} to 50% of V_{GATE}, V_{OUT} = VCC , $R_{(GATE-OUT)}$ = 1 MΩ,		0.8	1	
Power Good Output ($\overline{PG}$)						
	Low voltage (sinking)	$I_{\overline{PG}}$ = 2 mA		0.1	0.25	V
		$I_{\overline{PG}}$ = 4 mA		0.25	0.5	
	$\overline{PG}$ threshold voltage; V_{OUT} rising; $\overline{PG}$ goes low	V_{SENSE} = V_{VCC}; measure $V_{(VCC-OUT)}$	0.8	1.25	1.7	
	$\overline{PG}$ threshold voltage; V_{OUT} falling; $\overline{PG}$ goes open drain	V_{SENSE} = V_{VCC}; measure $V_{(VCC-OUT)}$	2.2	2.7	3.2	
	$\overline{PG}$ threshold hysteresis voltage; $V_{(SENSE-OUT)}$	V_{SENSE} = V_{VCC}		1.4		
t_{DPG}	$\overline{PG}$ deglitch delay; detection to output; rising and falling edges	V_{SENSE} = V_{VCC}	5	9	15	ms
$I_{LEAKAGE}$	Leakage current; $\overline{PG}$ false	open drain			10	µA
Overvoltage Input (OV)						
V_{OV_H}	Threshold voltage	OV rising	1.31	1.35	1.39	V
		Hysteresis	70	90	110	mV
$I_{LEAKAGE}$	Leakage current (sinking)	V_{OV} = 5 V			1	µA
t_{OFF}	Turn off time	V_{OV} = 0 → 2.5 V to V_{GS} < 1 V, C_{GATE} = 2 nF			2	µs
	Maximum duration of OV strong pull down	Gate pull down	40	100	220	
Output Voltage Feedback (OUT)						
I_{OUT}	Bias current	V_{OUT} = V_{VCC}, V_{UVEN} = Hi; sinking		8	20	µA
		V_{OUT} = GND; V_{UVEN} = Lo; sourcing		18	40	
Load Current Monitor (IMON) Output						
	Maximum output voltage	V_{CC} – V_{SENSE} = 200 mV	2.6	2.8	3	V
I_{SOURCE}	Source current		1.9			mA
I_{SINK}	Sink current			60		µA
	Gain (V_{IMON}/$V_{(VCC-SENSE)}$)		46	48	50	V/V
V_{OFFSET}	Offset voltage		-50	-5	30	mV
	Linearity(1)	Error relative to curve fit, 5 mV < (V_{CC} – V_{SENSE})		0.3%		
	Output Ripple(1)			8		mV_{PP}

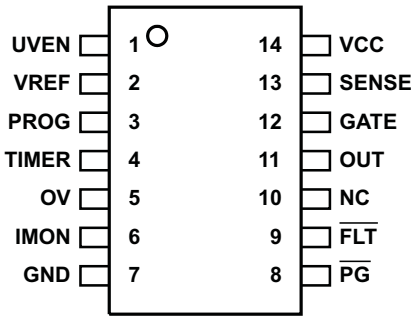
(1) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

DEVICE INFORMATION

Functional Block Diagram



PW PACKAGE
(top view)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
UVEN	1	I	A low input inhibits GATE. A logic input can drive this pin as an enable.
VREF	2	O	4-V reference voltage used to set the power threshold on PROG pin.
PROG	3	I	FET power-limit programming pin
TIMER	4	I/O	A capacitor from TIMER to ground sets the fault timer period.
OV	5	I	Overvoltage sensing input. A high input inhibits GATE.
IMON	6	O	Current monitor output, nominally V_{IMON} = 48 x ($V_{VCC-SENSE}$).
GND	7	PWR	Ground
$\overline{PG}$	8	O	Active low power good output. This is driven by $V_{VCC-SENSE}$.
$\overline{FLT}$	9	O	Active low fault indicator output. $\overline{FLT}$ indicates the fault timer has expired. $\overline{FLT}$ is reset by UVEN, UVLO, or automatic restart.
NC	10		No connect
OUT	11	I	FET source voltage (output) sensing pin. Gate is clamped to a diode drop below OUT.
GATE	12	O	Gate driver output for external FET.
SENSE	13	I	Current sensed as $V_{VCC-SENSE}$ and the FET V_{DS} as $V_{SENSE-OUT}$. For low FET V_{DS}, current limits at 50mV.
VCC	14	I	Input supply and current sense positive input

DETAILED PIN DESCRIPTION

The following description relies on the Typical Application Diagram shown on page 1, and the Functional Block Diagram.

VCC: This pin is associated with three functions:

1. Biasing power to the integrated circuit,
2. Input to power on reset (POR) and under-voltage lockout (UVLO) functions, and
3. Voltage sense at one terminal of R_{SENSE} for M1 current measurement.

The voltage must exceed the POR (about 6 V for roughly 400 µs) and the internal UVLO (about 8 V) before normal operation (driving the GATE) may begin. Connections to VCC should be designed to minimize R_{SENSE} voltage sensing errors and to maximize the effect of C1 and D1; place C1 at R_{SENSE} rather than at the device pin to eliminate transient sensing errors. GATE, PROG, and TIMER are held low when either UVLO or POR are active. $\overline{PG}$ and $\overline{FLT}$ are open drain when either UVLO or POR are active.

SENSE: Monitors the voltage at the drain of M1, and the downstream side of R_{SENSE} providing the constant power limit engine with feedback of both M1 current (I_D) and voltage (V_{DS}). Voltage is determined by the difference between SENSE and OUT, while the current analog is the voltage difference between VCC and SENSE. The constant power engine uses V_{DS} to compute the allowed I_D and is clamped to 50 mV, acting like a traditional current limit at low V_{DS}. The current limit is set by the following equation:

$$I_{LIM} = \frac{50mV}{R_{SENSE}} \quad (1)$$

Design the connections to SENSE to minimize R_{SENSE} voltage sensing errors. Don't drive SENSE to a large voltage difference from VCC because it is internally clamped to VCC. The current limit function can be disabled by connecting SENSE to VCC.

GATE: Provides the high side (above VCC) gate drive for external N-channel FET. It is controlled by the internal gate drive amplifier, which provides a pull-up of 22 µA from an internal charge pump and both strong (125 mA) and weak (2 mA) pull-downs to ground. The strong pull down is triggered by an overvoltage on the OV pin or large overcurrent to the load. The strong pull-down current is a non-linear function of the gate amplifier overdrive; it provides small drive for small overloads, but large overdrive for fast reaction to an output short. There is a separate pull-down of 2 mA to shut the MOSFET off when UVEN or UVLO cause this to happen. If an output short causes the VCC to fall below the UVLO, the turnoff speed will be limited by the 2mA turnoff current. An internal clamp protects the gate of the FET (to OUT).

OUT: This input pin is used by the constant power engine and the $\overline{PG}$ comparator to measure V_{DS} of M1 as $V_{(SENSE-OUT)}$. Internal protection circuits leak a small current from this pin when it is low. If the load circuit can drive OUT below ground, connect a clamp (or freewheel) diode from OUT (cathode) to GND (anode). The diode should clamp the output above -1 V during the transient.

UVEN: The positive threshold of UVEN must be exceeded before the GATE driver is enabled. If the UVEN pin drops below the UVEN negative threshold while the GATE driver is enabled, the GATE driver will be pulled to GND by the 2-mA pull down. UVEN can be used as a logic control input, an analog input voltage monitor as illustrated by R1, R2 and R3 in the Typical Application Circuit, or it can be tied to VCC to always enable the TPS2492/3. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input condition and shutting the downstream circuits off. A TPS2492 that has latched off can be reset by cycling UVEN below its negative threshold and back high.

VREF: Provides a 4.0-V reference voltage for use in conjunction with R4/R5 of the Typical Application Circuit to set the voltage on the PROG pin. The reference voltage is available once the internal POR and UVLO thresholds have been met. It is not designed as a supply voltage for other circuitry, therefore ensure that no more than 1 mA is drawn. Bypass capacitance is not required, but if a special application requires one, less than 1000 pF can be placed on this pin. This limit maintains VREG regulator stability.

PROG: The voltage applied to this pin (0.4 V minimum) programs the power limit used by the constant power engine. Normally, a resistor divider R4/R5 is connected from VREF to PROG to set the power limit according to the following equation:

$$V_{PROG} = \frac{P_{LIM}}{10 \times I_{LIM}} \quad (2)$$

where P_{LIM} is the desired power limit of M1 and I_{LIM} is the current limit set point (see SENSE). P_{LIM} is determined by the desired thermal stress on M1:

$$P_{LIM} < \frac{T_{J(MAX)} - T_{S(MAX)}}{R_{\Theta JC(MAX)}} \quad (3)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature of M1 and $T_{S(MAX)}$ is the maximum case temperature prior to a start or restart. V_{PROG} is used in conjunction with V_{DS} to compute the (scaled) current, $I_{D\_ALLOWED}$, by the constant power engine. $I_{D\_ALLOWED}$ is compared by the gate amplifier to the actual I_D, and used to generate a gate drive. If $I_D < I_{D\_ALLOWED}$, the amplifier turns the gate of M1 full on because there is no overload condition; otherwise GATE is regulated to maintain the $I_D = I_{D\_ALLOWED}$ relationship.

A capacitor may be tied from PROG to ground to alter the natural constant power inrush current shape. If properly designed, the effect is to cause the leading step of current in Figure 13 to look like a ramp. It is not recommended that this mechanism be used to achieve a long and low ramp inrush current because the power limiting accuracy is lower at $V_{PROG} < 0.4$ V. PROG is internally pulled to ground whenever UVEN, POR, or UVLO are not satisfied or the TPS2492 is latched off. This feature serves to discharge any capacitance connected to the pin. Do not apply voltages greater than 4 V to PROG. If the constant power limit is not used, PROG should be tied to VREF through a 47-kΩ resistor.

TIMER: An integrating capacitor, C_T, connected to the TIMER pin sets the fault-time for both versions and the restart interval for the TPS2493. The timer charges at 27 µA whenever the TPS2492/3 is in power limit or current limit and discharges at 2.7 µA otherwise. The charge-to-discharge current ratio is constant with temperature even though there is a positive temperature coefficient to both. If V_{TIMER} reaches 4 V, the TPS2492/3 pulls GATE to ground (with the strong pull down), and discharges C_T. The TPS2492 latches off when the fault timer expires. The TPS2493 holds GATE at ground when the timer expires before it attempts to restart (re-enable GATE) after a timing sequence consisting of discharging TIMER down to 1 V followed by 15 more charge and discharge cycles. Design for the TPS2393 TIMER period must assume a 3-V rise in V_{TIMER} rather than a 4-V rise to accommodate a restart.

The TPS2492 can be reset by either cycling the UVEN pin or the UVLO (e.g. power cycling). TIMER discharges when UVEN is low or the internal UVLO or POR are active. The TIMER pin should be tied to ground if this feature is not used.

$\overline{PG}$: The power good output is an active low, open-drain output intended to interface to downstream DC-to-DC converters or monitoring circuits. $\overline{PG}$ goes low after V_{DS} of M1 has fallen to about 1.25 V and a 9-ms deglitch time period has elapsed. $\overline{PG}$ is open drain whenever UVEN is low, V_{DS} of M1 is above 2.7 V, or UVLO is active. $\overline{PG}$ can also be viewed as having an output voltage monitor function. The 9-ms deglitch circuit operates to filter short events that could cause $\overline{PG}$ to go inactive (open drain) such as a momentary overload or input voltage step. $V_{\overline{PG}}$ can be greater than V_{VCC} because it's ESD protection is only with respect to ground. $\overline{PG}$ may be left open or tied to GND if not used.

GND: This pin is connected to system ground.

IMON: This current monitor output has a voltage equal to 48 times the voltage across R_{SENSE} ($V_{VCC\text{-}SENSE}$). IMON is clamped at 2.7 V to prevent damage to downstream A/D circuits. IMON is a voltage output and does not require a pull up or pull down. IMON will have a small amount of superimposed ripple at 2.5 kHz that is an artifact of the monitoring circuit. The error due to the ripple does not significantly effect accuracy for signals on the order of 1 V, but better accuracy may be achieved for small signals with an external R-C filter. The IMON pull up source is stronger than the pull down. A resistor pull down can be used to improve transient response in designs with large filter capacitors. Leave IMON open if not used.

A curve of Linearity (%) versus $V_{VCC\text{-}SENSE}$ is provided in the Typical Characteristics, providing an indication of error versus signal level. This curve is constructed by first performing a first order curve fit to V_{IMON} versus $V_{VCC\text{-}SENSE}$, yielding Gain and Offset terms for the linear fit. The Linearity (%) plot is calculated as:

$$\text{Linearity}(\%) = \frac{V_{IMON} - \left[\left(\text{Gain} \times V_{VCC-SENSE}\right) + \text{Offset}\right]}{\left[\left(\text{Gain} \times V_{VCC-SENSE}\right) + \text{Offset}\right]} \times 100 \quad (4)$$

$\overline{FLT}$: This active low, open drain output asserts (goes low) when the fault timer expires after a prolonged over current or an OV is detected. $\overline{FLT}$ is open drain whenever UVEN, POR, or UVLO are not satisfied. $\overline{FLT}$ is latched in the TPS2492, clearing when the latch is reset. $\overline{FLT}$ clears automatically in the TPS2493 when a power-up retry occurs. $V_{\overline{FLT}}$ can be greater than V_{VCC} because it's ESD protection is only with respect to ground. $\overline{FLT}$ may be left open or tied to GND when not used.

OV: The over-voltage monitoring pin is programed with a resistor divider such as R1 - R3 in the Typical Application Circuit. This function forces GATE and $\overline{FLT}$ low while the OV condition exists. While V_{OV} exceeds its threshold, the strong GATE pull down (125 mA) is applied for up to 100 µs, followed by the 2 mA pull down. The GATE pull down and $\overline{FLT}$ are released as soon as the OV condition is cleared. Tie OV to GND if not used.

TYPICAL CHARACTERISTICS

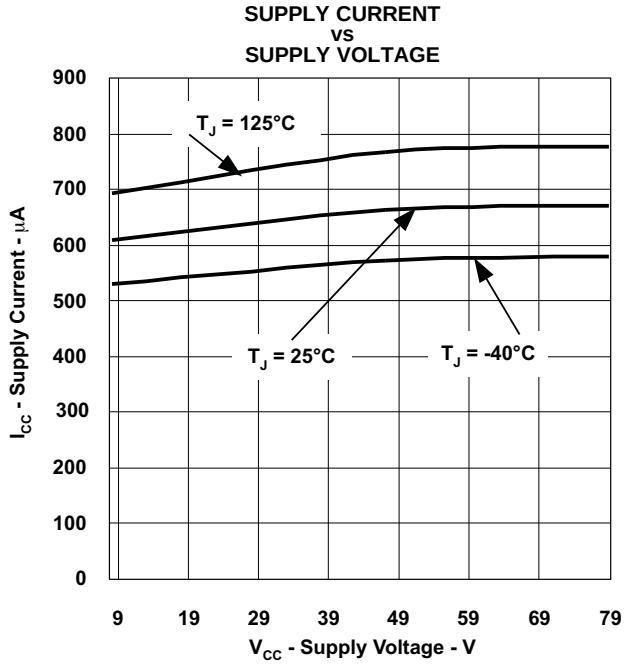


Figure 1.

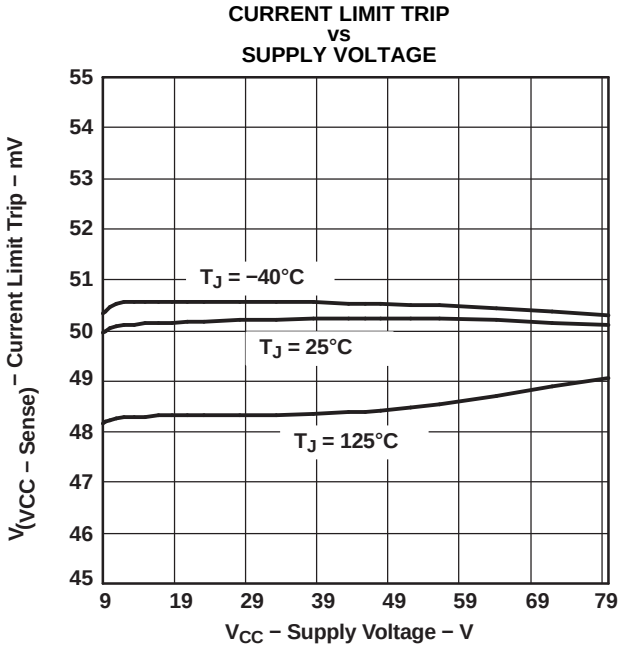


Figure 2.

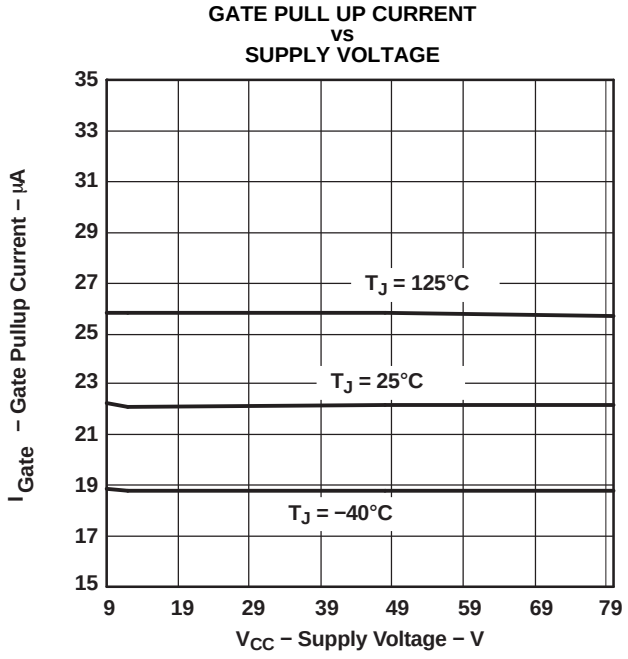


Figure 3.

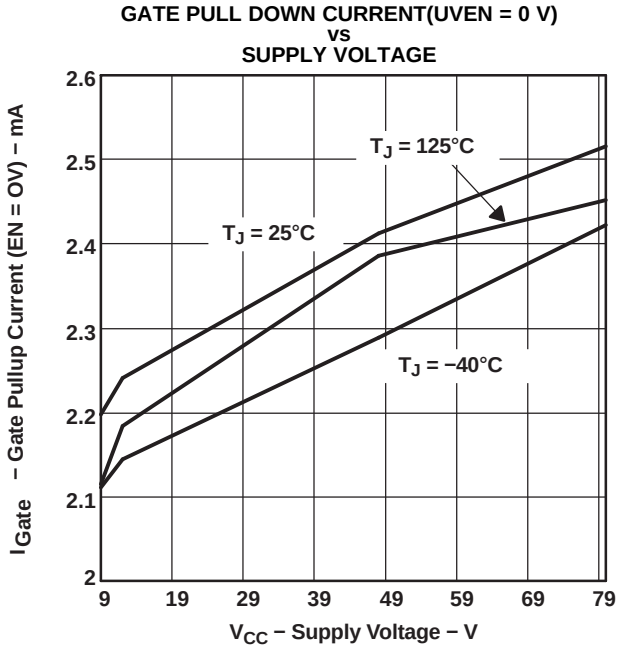


Figure 4.

TYPICAL CHARACTERISTICS (continued)

GATE PULL DOWN CURRENT
vs
SUPPLY VOLTAGE
(UVEN = 4 V, $V_{(VCC - SENSE)}$ = 200 mV)

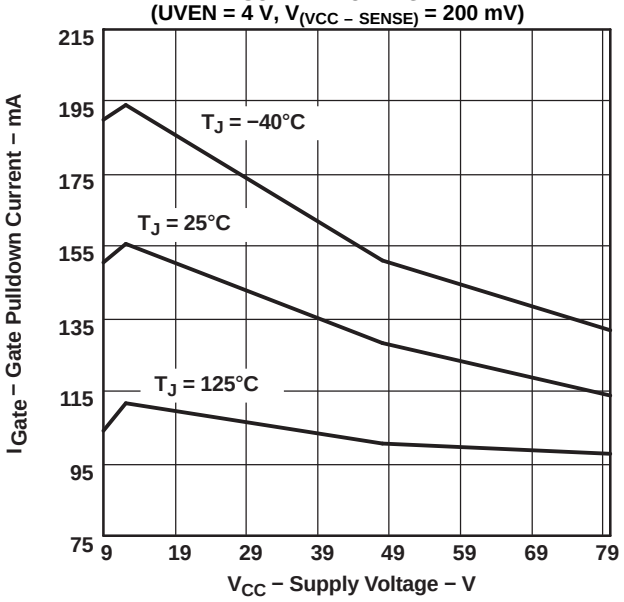


Figure 5.

CURRENT LIMIT RESPONSE TIME
vs
SUPPLY VOLTAGE
(UVEN = 4 V, $V_{(VCC - SENSE)}$ = 200 mV)

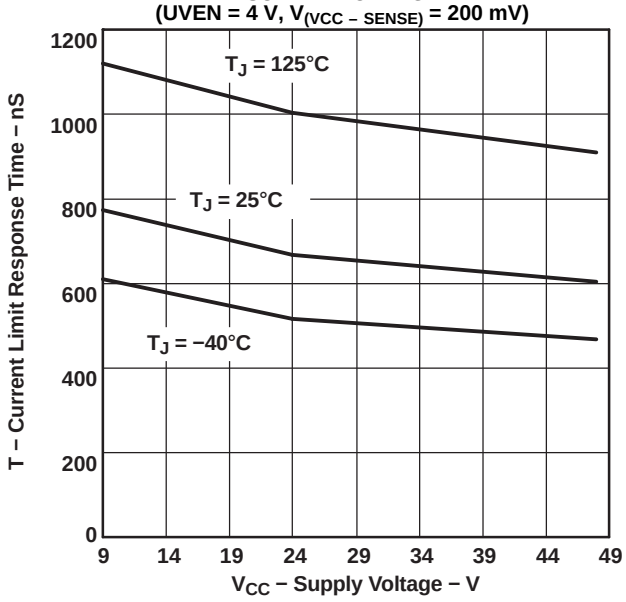


Figure 6.

GATE OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

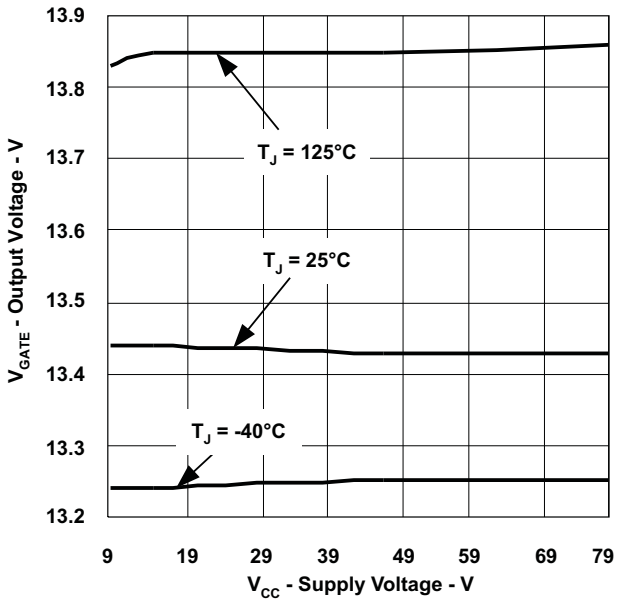


Figure 7.

TIMER PULL UP CURRENT
vs
SUPPLY VOLTAGE

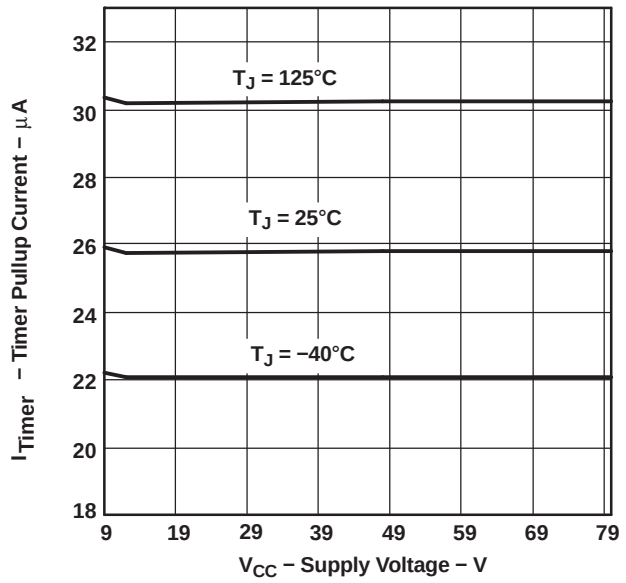


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TIMER CHARGE/DISCHARGE RATIO
vs
SUPPLY VOLTAGE AND TEMPERATURE

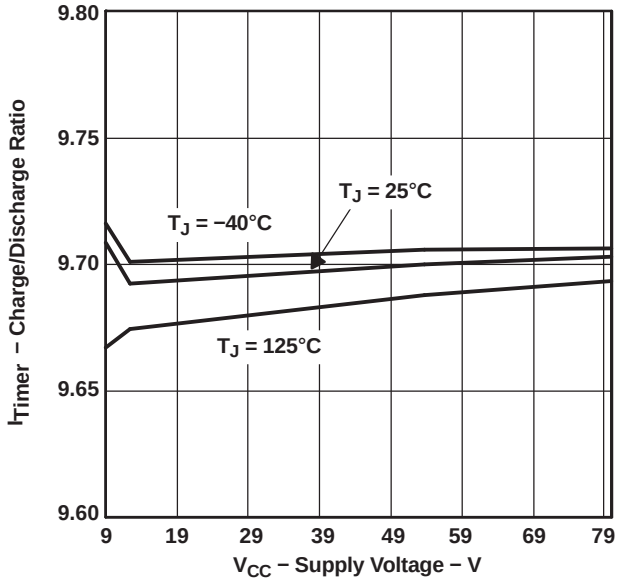


Figure 9.

UVEN AND OV THRESHOLD VOLTAGE (falling)
vs
SUPPLY VOLTAGE

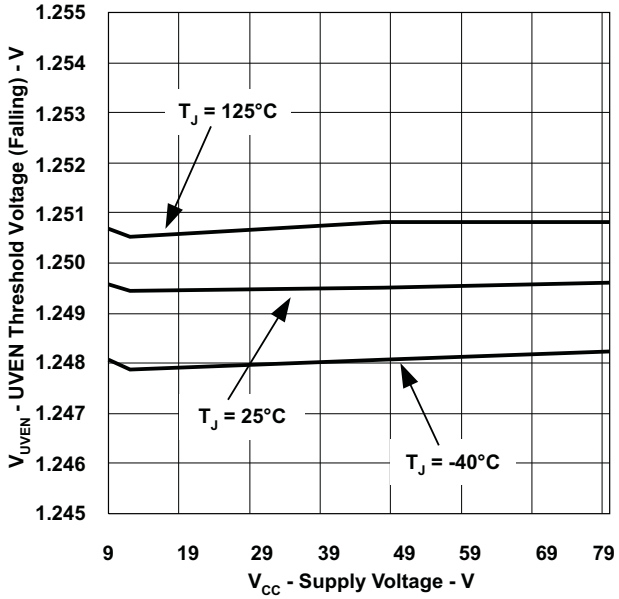


Figure 10.

UVEN AND OV THRESHOLD VOLTAGE (rising)
vs
SUPPLY VOLTAGE

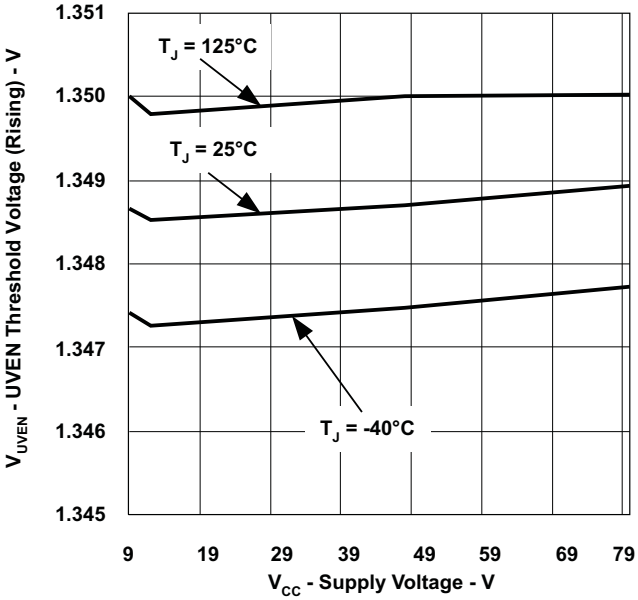


Figure 11.

LINEARITY
vs
SUPPLY VOLTAGE

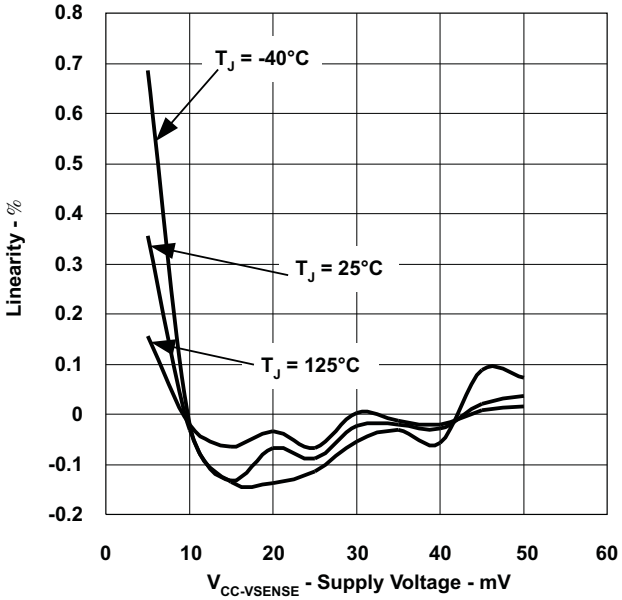


Figure 12.

APPLICATION INFORMATION

Basic Operation

The TPS2492/93 features include:

1. Adjustable under-voltage and over-voltage lockout;
2. Turn-on inrush limit;
3. High-side gate drive for an external N-channel FET;
4. FET protection (power limit and current limit);
5. Adjustable overload timeout;
6. Output current monitor;
7. Status output;
8. Charge-complete indicator for downstream converter sequencing; and
9. Optional automatic restart mode.

The TPS2492/93 features power-limiting FET protection that allows independent control of current limit (to set maximum full-load current), power limit (to keep FET in its safe operating area), and overload time (to control temperature rise). The power limiting feature controls the V and I across the FET to protect it, and does not control load power. This protection is a specialized form of foldback output limiting. Given a constant power dissipation, computation of peak junction temperature is straight forward. The TPS2393 provides a small operating duty cycle into a short, reducing the average temperature rise of the FET to levels similar to normal operation in many systems. This prevents overheating and failure with prolonged exposure to an output short. The typical application circuit, and oscilloscope plots of Figure 13 and Figure 17 demonstrate many of the functions described above.

Board Plug-In (Figure 13)

Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in as seen in Figure 13. The TPS2492/93 is held inactive with GATE, PROG, and TIMER held low, and with $\overline{PG}$ and $\overline{FLT}$ open drain, for less than 1 ms while internal voltages stabilize. Then GATE, PROG, TIMER, $\overline{FLT}$ and $\overline{PG}$ are released and the part begins sourcing current to the GATE pin because UVEN is high and OV is low. The external FET begins to turn on while the voltage across it, $V_{(SENSE-OUT)}$, and current through it, $V_{(VCC-SENSE)}/R_{SENSE}$, are monitored. Current initially rises to the value which satisfies the power limit engine (P_{LIM}/ V_{VCC}) since the output capacitor was discharged. The shape of the input current waveform shows the operation of the FET power limit. In this case, the 5-A current limit is never reached as the output reaches full charge. This is likely due to the limited gate slew rate.

TIMER and $\overline{PG}$ Operation (Figure 13)

The TIMER pin charges C_T as long as limiting action continues, and discharges at a 1/10 charge rate when limiting stops. If the voltage on C_T reaches 4 V before the output is charged, the external FET is turned off and either a latch-off or restart cycle commences, depending on the part type. The open-drain $\overline{PG}$ output provides a deglitched end-of-charge indication which is based on the voltage across the external FET. $\overline{PG}$ is useful for preventing a downstream DC-to-DC converter from starting while C_O is still charging. $\overline{PG}$ goes active (low) about 9 ms after C_O is charged. This delay allows the external FET to fully turn on and any transients in the power circuits to end before the converter starts up. The resistor pull-up shown on pin $\overline{PG}$ in the Typical Application Circuit only demonstrates operation; the actual connection to the converter depends on the application. Timing can appear to terminate early in some designs if operation transitions out of the power limit mode into a gate charge-rate limited mode at low V_{DS} values. This effect sometimes occurs because gate capacitances, C_{GD} and C_{GS}, are nonlinear with applied voltage, getting larger at smaller voltage. This can be seen in Figure 13.

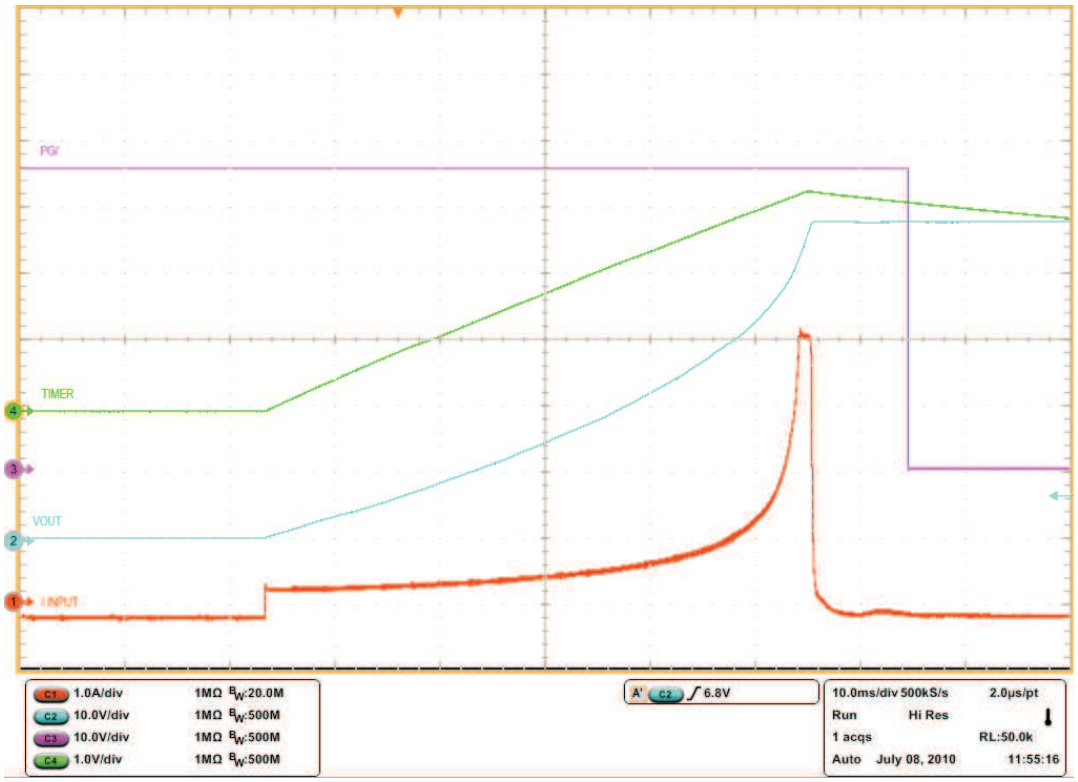


Figure 13. Basic Board Insertion

Action of the Constant Power Engine (Figure 14)

The calculated power dissipated in the external FET, V_{DS} x I_D, is computed under the same startup conditions as Figure 13. The current of the external FET, labeled I_{IN}, initially rises to the value that satisfies the constant power engine; in this case it is 25 W / 48 V = 0.52 A. The 25-W value is programmed into the engine by setting the PROG voltage using R4 and R5. V_{DS} of the external FET, which is calculated as $V_{(SENSE-OUT)}$, falls as C_O charges, thus allowing the external FET drain current to increase. This is the result of the internal constant power engine adjusting the current limit reference to the GATE amplifier as C_O charges and V_{DS} falls. The calculated device power in Figure 14, labeled POWER, is seen to be reasonably constant within the limitations of circuit tolerance and acquisition noise. A fixed current limit is implemented by clamping the constant power engine output to 50 mV when V_{DS} is low. This protection technique can be viewed as a specialized form of foldback limiting; the benefit over linear foldback is that it yields the maximum output current from a device over the full range of V_{DS} while still protecting the device.

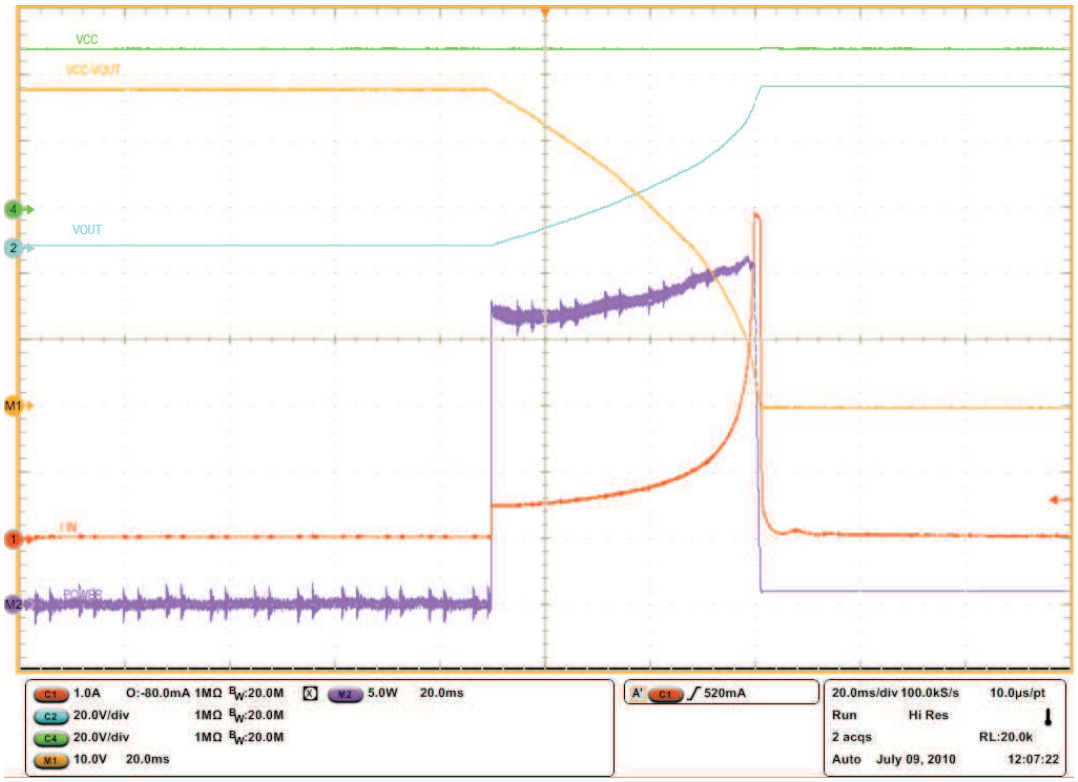


Figure 14. Computation of the External FET Stress During Startup

Response to a Hard Output Short (Figure 15, Figure 16, and Figure 17)

Figure 15 shows the short circuit response over the full time-out period. An output short is applied, causing the voltage to fall, limiter action begin, and the fault timer to start. The external FET current is actively controlled by the power limiting engine and gate amplifier circuit while the TIMER pin charges C_T to the 4-V threshold. Once this threshold is reached, the TPS2492/93 turns off the external FET. The TPS2492 latches off until either the input voltage drops below the UVLO threshold or UVEN cycles through the false (low) state. The TPS2493 will attempt a restart after going through a timing cycle. Figure 16 demonstrates the operation of $\overline{FLT}$ during a short circuit. $\overline{FLT}$ remains false (open drain) until the TIMER has expired.

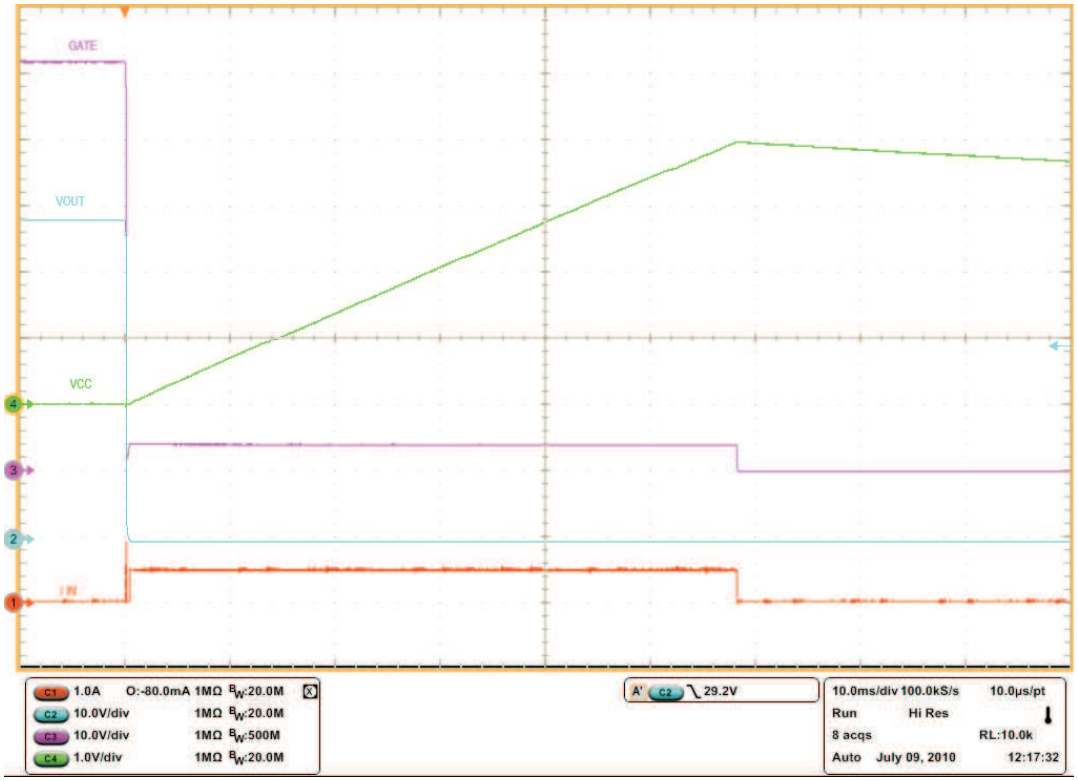


Figure 15. Current Limit Overview

Figure 16. $\overline{\text{FLT}}$ Operation

The TPS2492/93 responds rapidly to a short circuit as seen in Figure 17. The falling OUT voltage is the result of the external FET and C_O currents through the short circuit impedance. The internal GATE clamp causes the GATE voltage to follow the output voltage down and subsequently limits the negative V_{GS}. The I_{IN} waveform includes current into an input 47 µF capacitor. M1 drain current has a peak value in excess of the waveform, and terminates when V_{GATE} approaches V_{OUT}. The rapidly rising fault current overdrives the GATE amplifier causing it to overshoot and rapidly turn the external FET off by sinking current to ground. At a time beyond the extent of Figure 17, but within the scope of Figure 15, the FET will be slowly turned back on as the GATE amplifier recovers. The operating point will settle to the current or power limit, and finally the TIMER will expire and the FET will turn off.

Limited input voltage overshoot appears in Figure 17 because a local 47-µF bypass capacitor and 1000 µF distribution capacitor were used. The input voltage overshoots as the input current abruptly drops due to the stored energy in the input wiring inductance. The exact waveforms seen in an application depend upon many factors including parasitics of the voltage distribution, circuit layout, and the short itself.

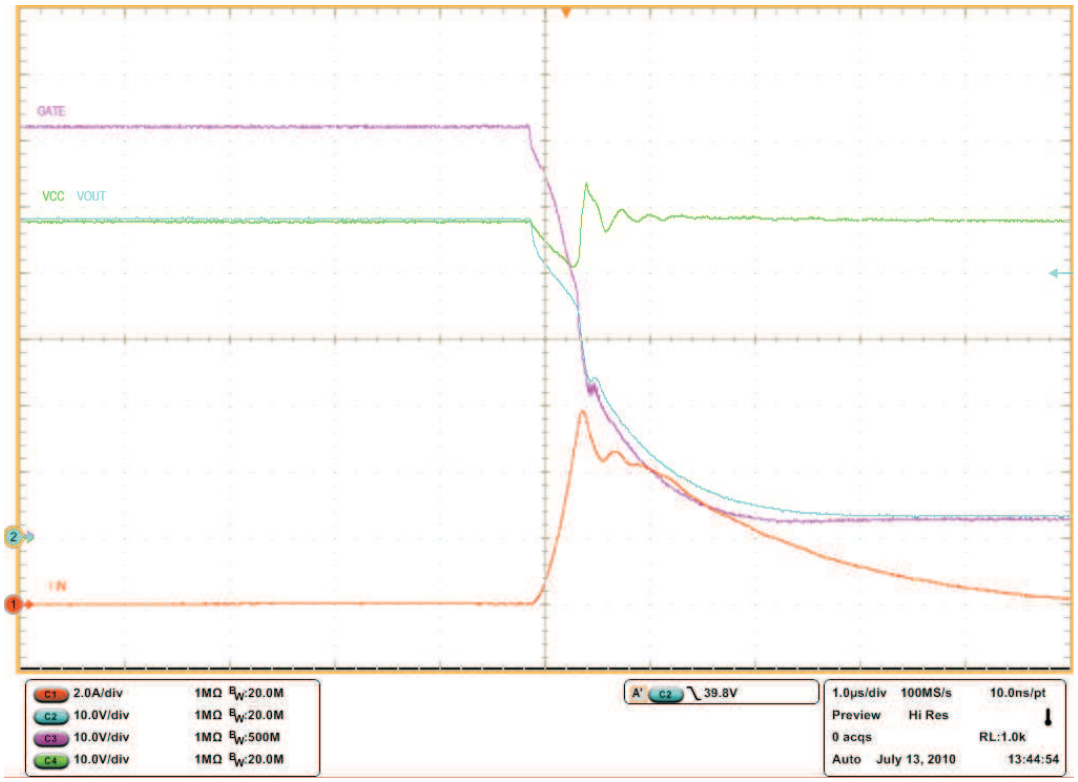


Figure 17. Current Limit Onset

Automatic Restart (Figure 18)

The TPS2493 automatically initiates a restart after a fault has caused it to turn off the external FET. Internal control circuits use C_T to count 16 cycles before re-enabling the external FET. This sequence repeats if the fault persists. TIMER has a 1:10 charge-to-discharge current ratio, and uses a 1-V lower threshold. The fault-retry duty cycle specification in the Electrical Characteristics Table quantifies this behavior. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and reduces the need for additional measures such as oversized heatsinking. Figure 18 demonstrates that the initial timing cycle starts with V_{TIMER} at zero V, subsequent cycles start with V_{TIMER} at 1 V, and a succesful restart occurs after a 16 cycle delay.

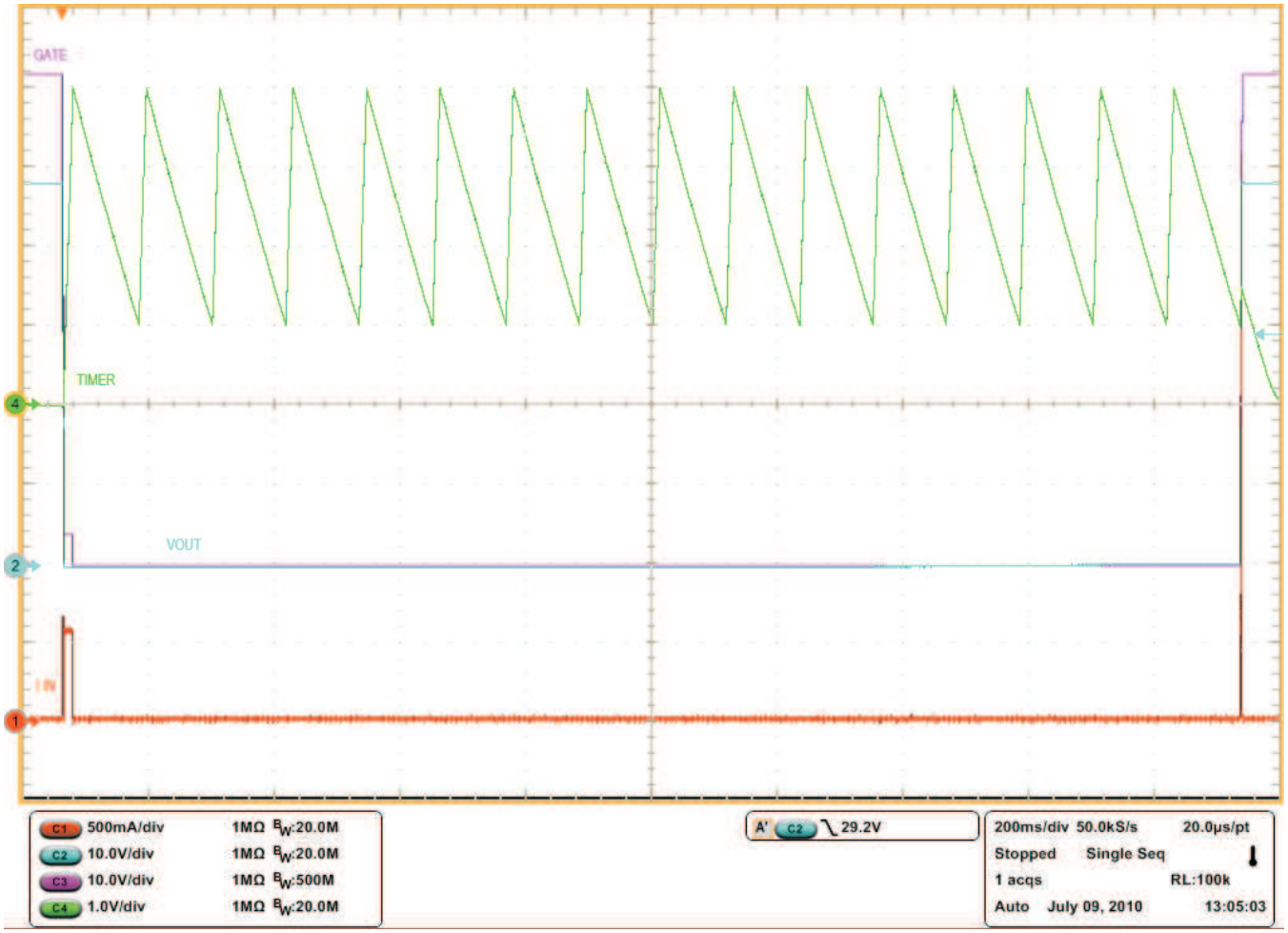


Figure 18. TPS2492/93 Restart Cycle Timing

Application Design Example

The following example illustrates the design and component selection process for a TPS2492/93 application. Figure 19 shows the application circuit for this design example. The requirements of this design are:

- Nominal System Voltage: 12 V
- Maximum Operating System Voltage: 13.5 V
- Overvoltage Threshold: 14.5 V
- Undervoltage Threshold: 9.5 V
- Steady-state Load Current: 40 A
- Load Capacitance: 1000 µF
- Maximum Ambient Temperature: 50°C
- Maximum Static Junction Temperature 125°C
- Maximum Transient Junction Temperature: 150°C

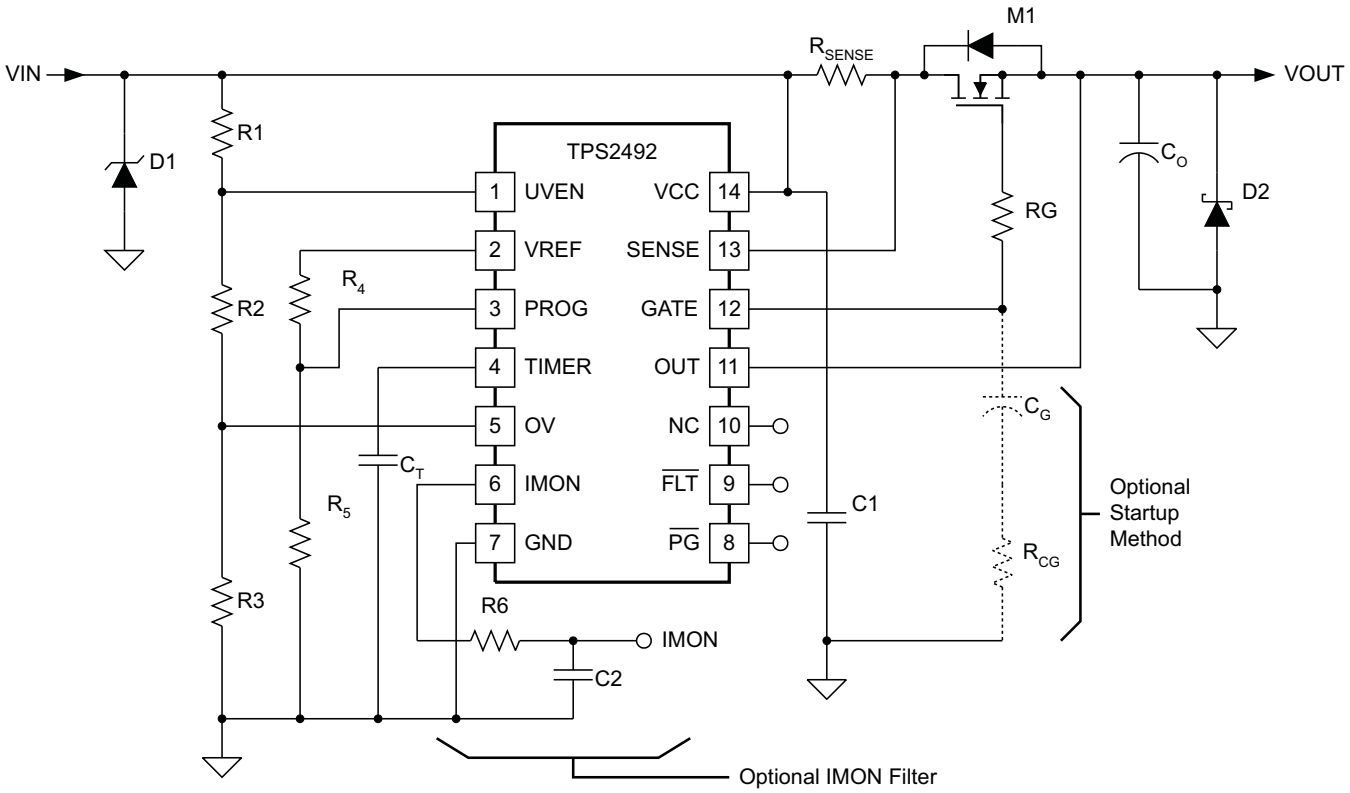


Figure 19. TPS2492/93 Design Example Schematic

1. Choose R_{SENSE}

Calculate R_{SENSE} using a multiplier factor of 1.2 (20%) for V_{SENSE} and R_{SENSE} tolerance along with some additional margin.

$$R_{SENSE} = \frac{V_{SENSE}}{1.2 \times I_{LIMIT}} = \frac{50mV}{1.2 \times 40A} = 1.042m\Omega \quad (5)$$

Choose R_{SENSE} = 1 mΩ, resulting in a nominal 50 A current limit.

$$I_{LIMIT(MAX)} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} = \frac{55mV}{1m\Omega} = 55A \quad (6)$$

$$P_{RSENSE} = I^2_{LIMIT(MAX)} \times R_{SENSE} = 55A^2 \times 1m\Omega = 3.025W \quad (7)$$

Multiple sense resistors in parallel should be considered.

2. Choose M1

Select the M1 V_{DS} rating allowing for maximum input voltage and transients. Then select an operating R_{DSON}, package, and cooling to control the operating temperature. Most manufacturers list $R_{DSON(MAX)}$ at 25°C and provide a typical characteristics curve from which values at other temperatures can be derived. The next equation can be used to estimate desired $R_{DSON(MAX)}$ at the maximum operating junction temperature of $T_{J(MAX)}$. (usually 125°C). $T_{A(MAX)}$ is the maximum expected ambient temperature. Assume that a thermal resistance, $R_{\theta JA}$ of 10 °C/W can be achieved by reinforcing the typical 40°C/W for a 1^2 inch copper pad with copper on multiple layers and some airflow.

$$R_{DSON(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JA} \times I^2_{LIMIT(NOM)}} = \frac{125°C - 50°C}{10\frac{°C}{W} \times (50A)^2} = 3m\Omega \text{ at } T_J = 125°C \quad (8)$$

Assume that we are able to find a suitable FET with an R_{DSON} of 0.74 mΩ at 25°C and 1.18 mΩ at 125°C. These devices are in a package such as a D2PAK with a large copper base and very low $R_{\theta JC}$.

The junction-to-ambient thermal resistance, $R_{\theta JA}$, depends upon the package style chosen and the details of heat-sinking and cooling including the PCB layout. Actual “in-system” temperature measurements will be required to validate thermal performance.

3. Choose the Power Limit P_{LIM} and the PROG Resistors, R_4 and R_5

M1 dissipates large amounts of power during power-up or output short circuit. Power limit, P_{LIM} should be set to prevent the M1 die temperature from exceeding a short term maximum temperature, $T_{J(MAX2)}$. Short term $T_{J(MAX2)}$ may be set as high as 150°C (specified on FET datasheet) while still leaving ample margin for the typical manufacturer's rating of 175°C. The R4 and R5 resistors set V_{PROG}, programming the FET power dissipation. Assume that $R_{\theta JA}$ is 10 °C/W, $R_{\theta JC}$ is 0.2 °C/W, and $R_{\theta CA}$ is 9.8 °C/W for the device we chose above. P_{LIM} can be estimated as follows:

$$P_{LIM} = \frac{0.7 \times \left[T_{J(MAX2)} - \left(R_{\theta CA} \times I^2_{LIMIT(NOM)} \times R_{DSON} \right) - T_{A(MAX)} \right]}{R_{\theta JC}} = 249W \tag{9}$$

Where $R_{\theta CA}$ is the M1 plus PCB case-to-ambient thermal resistance, $R_{\theta JC}$ is M1 junction-to-case thermal resistance, R_{DSON} is M1 channel resistance at the maximum operating temperature, and the factor of 0.7 accounts for the tolerance of the constant power engine. In this case we know that power limit is less than I_{LIMIT} x V_{IN} and that power limit will control operation during a short circuit.

It is often advantageous to use a transient value of $R_{\theta JC}$ to get a usable solution, that is a V_{PROG} within the recommended range. If a current/power limited startup is used, transient $R_{\theta JC}$ should be based on the TIMER period (see below). FET manufacturers typically provide transient thermal resistance in graphic format on their datasheet. Additional information can be found in SLVA158.

The following equations calculate V_{PROG} and R4 using an assumed R_5 = 20 kΩ.

$$V_{PROG} = \frac{P_{LIM}}{10 \times I_{LIM}} = \frac{249}{10 \times 50} = 0.498V \tag{10}$$

$$R_4 = R_5 \times \left(\frac{V_{REF}}{V_{PROG}} - 1 \right) = 140.6k\Omega \tag{11}$$

Choose R_4 = 140 kΩ. The recommended minimum V_{PROG} is 0.4 V. This is based on tolerance and accuracy of the constant power engine making very low power-limited designs highly variable. Some suggestions to get larger P_{LIM} values are to start with a low static operating junction temperature, and to utilize the transient thermal impedance (energy absorbing nature) of the package.

The output I vs. V_{OUT} curve for this configuration is shown in Figure 20.

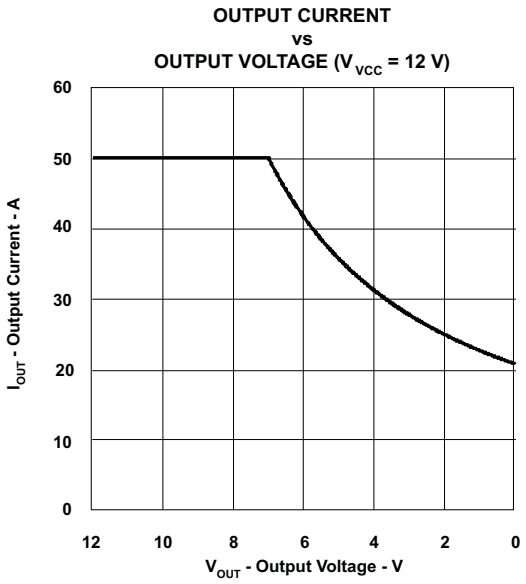


Figure 20. TPS2492/93 Power and Current Limit Curve

4. Choose the TIMER Capacitor, C_T and Turn-On Time

The turn on time t_{ON}, represents the time it takes the circuit to charge up the output capacitance C_O and load. C_T programs the fault time and should be chosen so that the fault timer does not terminate prior to completion of start up. The turn on time is a function of the type of control; current limit, power limit, or dV/dt control. The following equations calculates t_{ON} for the power limit and current limit cases, and assume that only C_O draws current during startup.

$$\text{For } P_{LIM} < V_{VCC(MAX)} \times I_{LIMIT(NOM)} : t_{ON} = \frac{C_O \times P_{LIM(ACT)}}{2 \times I^2_{LIMIT(NOM)}} + \frac{C_O \times V^2_{VCC(MAX)}}{2 \times P_{LIM(ACT)}} \left(Power\ Limit\right) \tag{12}$$

$$\text{For } P_{LIM} \geq V_{VCC(MAX)} \times I_{LIMIT(NOM)} : t_{ON} = \frac{C_O \times V_{VCC(MAX)}}{I_{LIMIT(NOM)}} \left(Current\ Limit\ Only\right) \tag{13}$$

$$t_{ON} = \frac{C_O \times P_{LIM}}{2 \times I^2_{LIMIT(NOM)}} + \frac{C_O \times V^2_{VCC(MAX)}}{2 \times P_{LIM}} = \frac{1000\mu F \times 249W}{2 \times 50^2 A} + \frac{1000\mu F \times 13.5V^2}{2 \times 249W} = 416\mu s \tag{14}$$

The next equation computes C_T for a TPS2492 application. TPS2492/93 TIMER current source and capacitor tolerances are accounted for.

$$C_T = \frac{I_{SOURCE(MAX)}}{V_{TMR\text{-}TH(MAX)}} \times t_{ON} \times (1 + C_{O\text{-}TOL} + C_{T\text{-}TOL}) \tag{15}$$

$$C_T = \frac{36\mu A}{4.1V} \times 416\mu s \times (1 + 0.2 + 0.1) = 4.75nF \tag{16}$$

Choose C_T = 6.8 nF assuming a 20% output capacitor tolerance and a 10% timing capacitor tolerance. Equation 16 is written around startup for a TPS2492, however during a restart (after a fault) of a TPS2493, C_T charges from 1 V to 4.1 V, requiring a $V_{TMR\text{-}TH(MAX)}$ value of 3.1V.

The maximum TIMER period may be calculated using the minimum TIMER charge current and maximum value of C_T. Use this period to determine the transient $R_{\theta JC}$ in step 3. While this is beyond the scope of this example, it may lead to some iteration.

5. Choose the Turn-On and Over-voltage Divider, R_1 - R_3

Per our system design requirements above, both over-voltage shutdown and under-voltage shutdown are desired. Equations for calculating the thresholds are:

$$V_{OV\_H} = \frac{V_{OV} \times R3}{(R1+R2+R3)} \quad (17)$$

$$V_{UVEN\_H} = \frac{V_{UV} \times (R2+R3)}{(R1+R2+R3)} \quad (18)$$

Assume R3 is 1 kΩ and use the following procedure to determine R1 and R2.

$$R1+R2 = \frac{R3 \times (V_{OV}-V_{OV\_H})}{(V_{UV\_H})} = \frac{1k\Omega \times (14.5V - 1.35V)}{1.35V} = 9.7407k\Omega \quad (19)$$

$$R2+R3 = \frac{V_{UVEN\_H} \times ((R1+R2)+R3)}{(V_{UV})} = \frac{1.25V \times (9.7407k\Omega + 1k\Omega)}{9.5V} = 1.4133k\Omega \quad (20)$$

$$R2=(R2+R3) - R3 = 1.4133k\Omega - 1k\Omega = 0.4133k\Omega \quad (21)$$

$$R1=(R1+R2) - R2 = 9.7407k\Omega - 0.4133k\Omega = 9.3275k\Omega \quad (22)$$

Selecting standard 1% values and scaling up by a factor of 10 to reduce power loss results in (R1 = 93.1 kΩ), (R2 = 4.12 kΩ), and (R3 = 10 kΩ).

Alternative Inrush Designs

Gate Capacitor (dV/dt) Control

The TPS2492/93 can be used with applications that require constant turn-on currents. The current is controlled by a single capacitor from the GATE terminal to ground with a series resistor. M1 appears to operate as a source follower (following the gate voltage) in this implementation. Again assuming that the output capacitor charges without additional loading, choose a time to charge, t_{ON}, based on the load capacitor, C_O input voltage V_I, and desired charge current I_{CHARGE}. When power limiting is used ($V_{PROG} < V_{REF}$) choose I_{CHARGE} to be less than P_{LIM}/V_{VCC} to prevent the fault timer from starting. The fault timer starts only if power or current limit is invoked.

$$t_{ON} = \frac{C_O \times V_{VCC}}{I_{CHARGE}} \quad (23)$$

Use the following equation to select the gate capacitance, C_G. It has been assumed that the external added (linear) capacitor is much larger than the FET capacitance. C_{GD} is the gate capacitance of M1, and I_{GATE} is the TPS2492/93 nominal gate charge current. C_{GD} is non-linear with applied V_{DG}. An averaged estimate may be made using the FET V_{GS} vs Q_G curve. Divide the charge accumulated during the plateau region by the plateau V_{GS} to get C_{GD}. As shown in Figure 19, a series resistor of about 1 kΩ should be used in series with C_G to avoid slowing the turnoff.

$$C_G = \frac{I_{GATE} \times t_{ON}}{V_{VCC}} - C_{GD} \quad (24)$$

If neither power nor current limit faults are invoked during turn on, C_T can be chosen for fast transient turnoff response. Considerations are junction temperature rise (as above), anticipated system noise, and possible peak overloads due to input voltage or load transients. Generally the period should be much less than the t_{ON} of step 4 above.

Additional Design Considerations

Calculation Tool SLVC033

The calculation tool for the TPS2490/91, SLVC033, may be used with the TPS2492/93. For accurate results, the timer current constants need to be updated. This may be accomplished using the Excel Tools / Protection command along with the password provided in the tool (spreadsheet).

Use of $\overline{PG}$ to Control Downstream Converters

Use the $\overline{PG}$ pin to control and sequence a downstream DC/DC converter. If this is not done a long time delay may be needed to allow C_O to fully charge before the converter starts. This practice will avoid having the converter attempt to operate at a low input voltage, drawing large currents. This mode of converter operation has the potential to form a stable operating point with the hotswap output I-V characteristic, preventing the system from starting.

IMON Filtering

The internal monitoring circuits leave a small amount of residual noise at about 2.5 kHz on the IMON output. While this does not contribute significant error at output voltages on the order of 1 V, better accuracy at low outputs will benefit from an R-C filter. Figure 19 demonstrates this filtering with elements R6 and C2. An example solution is a 1 kΩ resistor and a 1.5 nF capacitor. A buffer (e.g. unity-gain opamp) may be required if the output is used by a circuit that draws significant current.

Output Clamp Diode

Inductive loads or wiring inductance on the output may drive the OUT pin below GND when the circuit is unplugged or during current limit. The OUT pin can be protected by D2 (see Figure 19) between the TPS2492/93 OUT to GND pins. The OUT pin can withstand a short transient to -1 V.

Input Clamp TVS

Energy stored in the inductance of input wiring has the capability to drive the input voltage up if the (load) current is abruptly decreased. An example is a hard short on OUT rapidly raising the input current above the current limit threshold, which is then abruptly driven to zero when the current limit gains control after several microseconds. Combinations of input capacitance and transient voltage suppressor diodes (TVS - a type of Zener Diode) can aid in controlling the voltage overshoot. This is demonstrated by D1 and C1 of Figure 19. While a small bypass capacitor is recommended, the TVS is better able to control the voltage without the drawback of large input capacitance.

Gate Clamp Diode

The TPS2492/93 has a relatively well-regulated gate voltage of 12 V to 16 V, even at low supply voltages. A small clamp Zener from gate to source of M1, such as a BZX84C7V5, is recommended if V_{GS} of M1 is rated below this.

Input Bypass Capacitance

The input bypass capacitor, C1 per Figure 19 should be used to provide a low impedance local source of current and control the supply dv/dt on the VCC pin.

Adding External GATE-OUT Capacitance

Avoid directly placing ceramic capacitors directly across M1 gate to source when bypassing for ESD or noise is desired. Add some small resistance in series with the capacitor if absolutely required. If the resistance is not present, the added phase shift may encourage high frequency oscillation of the combined input and output L-C circuits during startup conditions.

High Gate Capacitance Applications

If OUT falls very rapidly during a fault, the FET V_{GS} can be driven high by the C_{GD} - C_{GS} voltage divider of (V_{SENSE} - V_{OUT}). Given enough capacitance and dv/dt, the internal 14-V GATE to OUT clamp may not have the capability to fully control the voltage. An external gate clamp Zener diode may be required to protect the FET if this is the case.

When gate capacitor dV/dT control is used, a 1-kΩ resistor in series with C_G is recommended, as shown in Figure 19.

Output Short Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to varying results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet since every setup differs.

Applications Using the Retry Feature (TPS2493)

Applications using the retry feature may want to estimate fault retry time. The TPS2493 will retry (enable M1 to attempt turn on) once for every 16 timer charge/discharge cycles (15 cycles between 1 V and 4 V, 1 cycle between 0 V and 4 V).

$$T_{RETRY} = C_T \times 19.6 \times 10^6 \quad (25)$$

M1 Selection

Use of a power FET in the linear region places large, long term stresses on the distributed junction. FETs whose safe operating area (SOA) curves display multiple slopes on the same line (e.g. a line whose time parameter is a constant) in the region of high voltage and low current generally are susceptible to secondary breakdown and are not strong candidates for this application. An example of a good choice is found in the Typical Application Circuit where the line at 10 ms shows no breaks in slope. The best device for the application is not always the lowest R_{DSON} device.

Layout Considerations

Good layout practice places the power devices D1, R_{SENSE}, M1, and C_O so power flows in a sequential, linear fashion. A ground plane under the power and the TPS2492/93 is desirable. The TPS2492/93 should be placed close to the sense resistor and FET using a Kelvin type connection to achieve accurate current sensing across R_{SENSE}. A low-impedance GND connection is required because the TPS2492/93 can momentarily sink upwards of 100 mA from the gate of M1. The GATE amplifier has high bandwidth while active, so keep the GATE trace length short. The PROG, TIMER, OV, and UVEN pins have high input impedances, therefore keep their input leads short. Oversize power traces and power device connections to assure low voltage drop and good thermal performance.

REVISION HISTORY

Changes from Original (July 2010) to Revision A	Page
• Changed marketing status	1

Changes from Revision A (#IMPLIED) to Revision B	Page
• Changed temperature rating from 80°C to 125°C in the product Information section to match the rest of the datasheet.	2

Changes from Revision B (October 2011) to Revision C	Page
• Added design calculator hyperlink.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2492PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2492	Samples
TPS2492PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2492	Samples
TPS2493PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2493	Samples
TPS2493PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2493	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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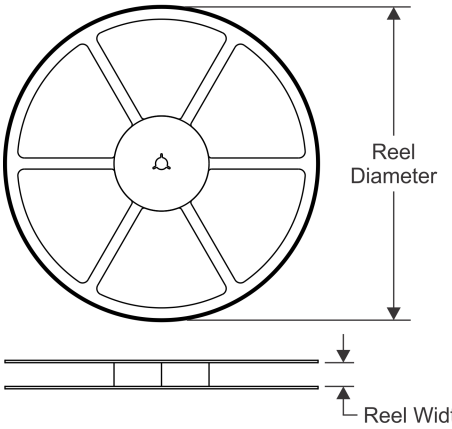
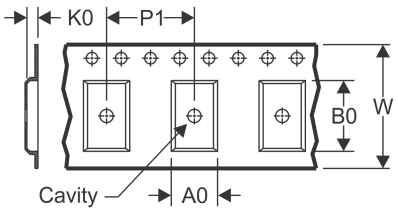
TAPE AND REEL INFORMATION

REEL DIMENSIONS

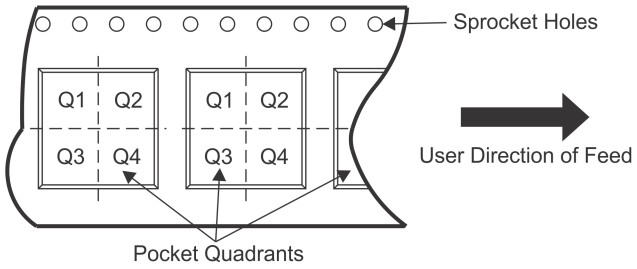


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

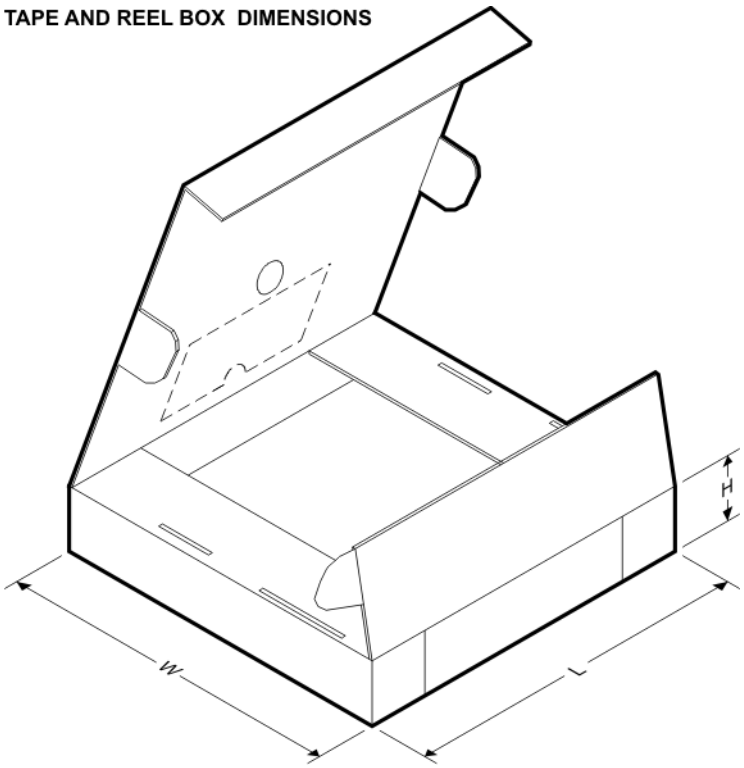
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2492PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2493PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

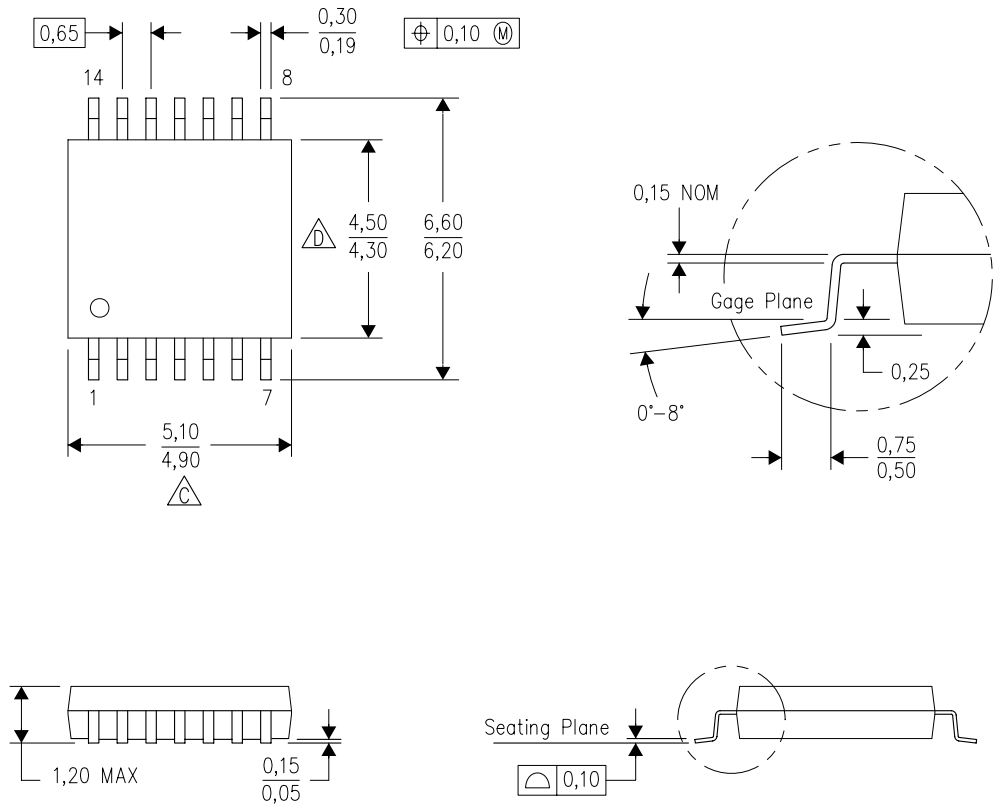
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2492PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TPS2493PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

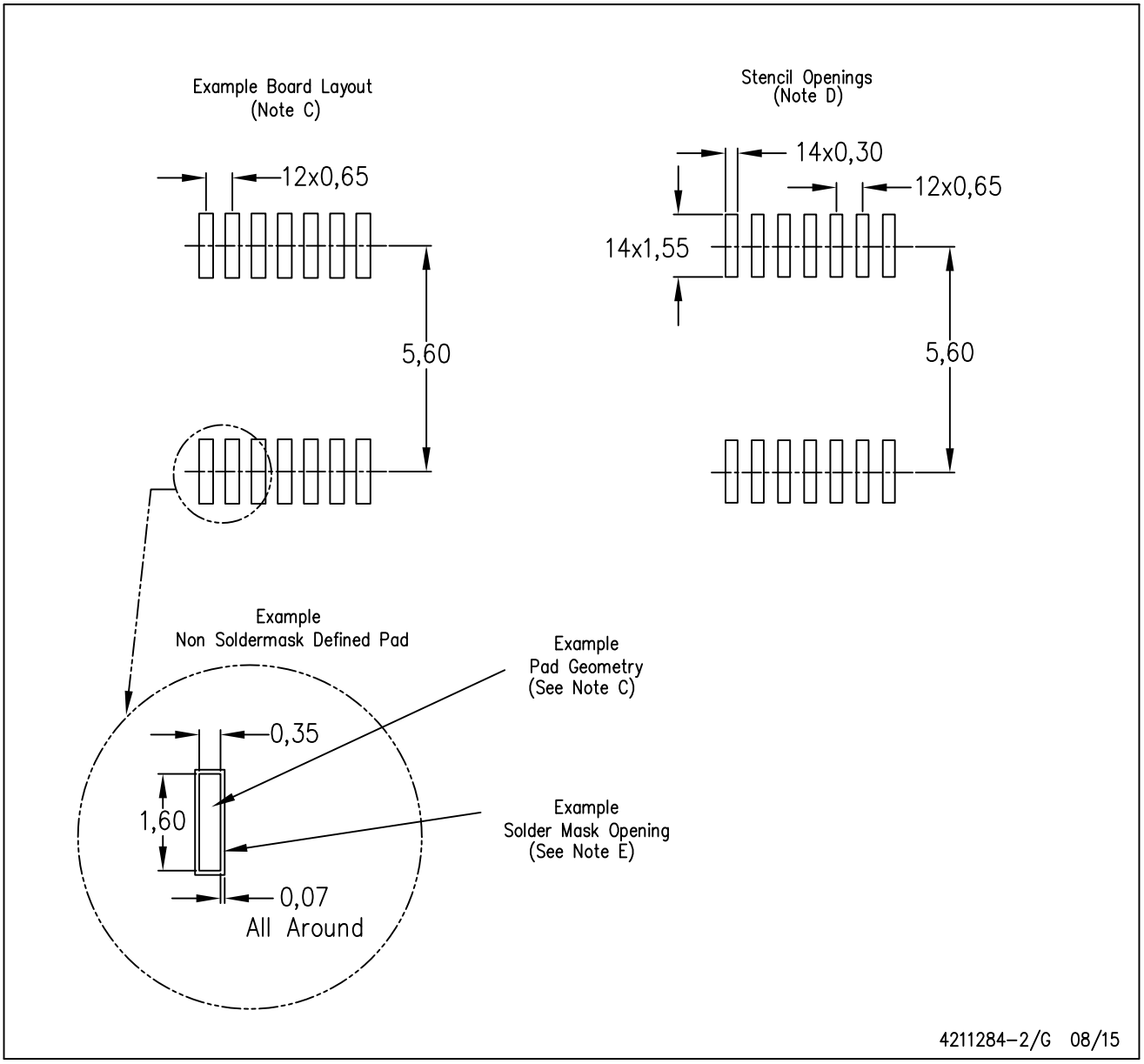
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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