CY7C1480V33

72-Mbit (2M × 36) Pipelined Sync SRAM

Features

- Supports bus operation up to 200 MHz
- Available speed grades are 200 and 167 MHz
- Registered inputs and outputs for pipelined operation
- 3.3 V core power supply
- 2.5 V/3.3 V I/O operation
- Fast clock-to-output times
  - 3.0 ns (for 200 MHz device)
- Provide high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1480V33 available in JEDEC-standard Pb-free 100-pin TQFP package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- “ZZ” Sleep Mode option

Functional Description

The CY7C1480V33 SRAM integrates 2M × 36 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable (CE_1), depth-expansion Chip Enables (CE_2 and CE_3), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables (BW_X, and BWE), and Global Write (GW). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at the rising edge of the clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle.This part supports byte write operations (see "Pin Definitions" on page 5 and "Truth Table" on page 8 for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. GW when active LOW causes all bytes to be written.

The CY7C1480V33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

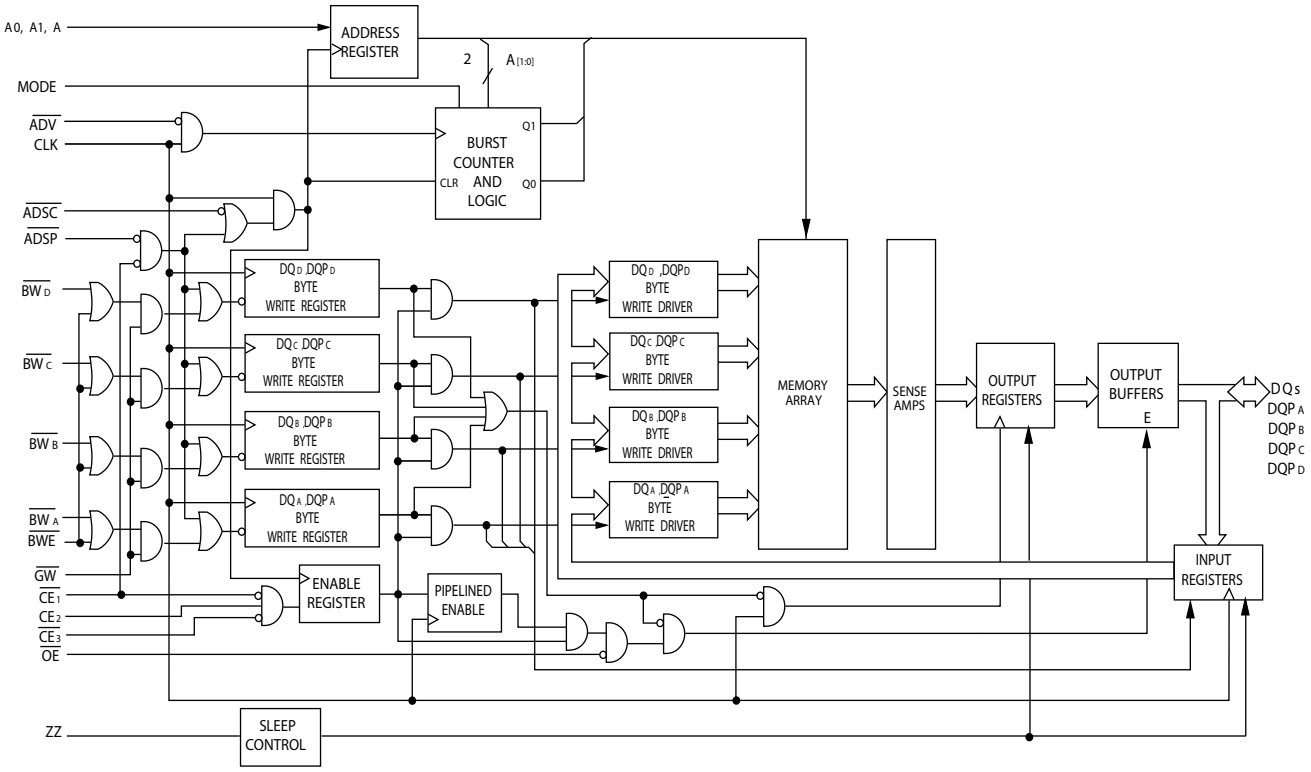
For a complete list of related documentation, click here.

Selection Guide

Description	200 MHz	167 MHz	Unit
Maximum Access Time	3.0	3.4	ns
Maximum Operating Current	500	450	mA
Maximum CMOS Standby Current	120	120	mA

Errata: For information on silicon errata, see "Errata" on page 21. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram – CY7C1480V33



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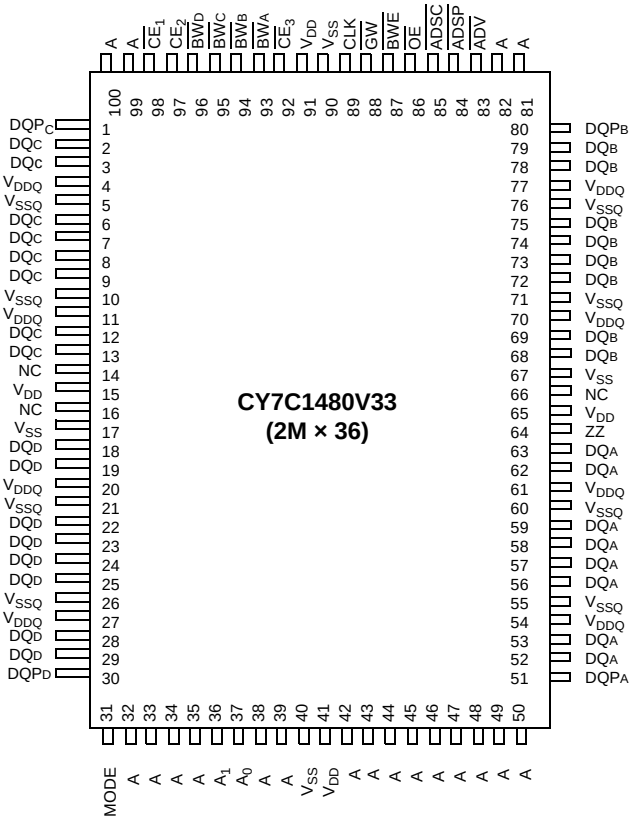
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout [1]



Note

1. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see"Errata" on page 21.This issue is fixed in the CY7C1480BV33 device.

Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A1:A0 are fed to the two-bit counter.
$\overline{BW}_A$,$\overline{BW}_B$, $\overline{BW}_C$,$\overline{BW}_D$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on BW_X and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal, Sampled on the Rising Edge of CLK, Active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ[2]	Input-Asynchronous	**ZZ "Sleep" Input, Active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQPs	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}[3]	I/O Ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.

Notes
2. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see"Errata" on page 21.This issue is fixed in the CY7C1480BV33 device.
3. Applicable for TQFP package.

Pin Definitions (continued)

Pin Name	I/O	Description
MODE	Input Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up.
TDO	JTAG Serial Output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG Serial Input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG Serial Input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.0 ns (200 MHz device).

The CY7C1480V33 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW_X}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, CE_3 are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.0 ns (250-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. After the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tri-states immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE_1}$, CE_2, CE_3 are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW_X}$ signals.

The CY7C1480V33 provides byte write capability that is described in the "Truth Table for Read/Write" on page 9. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW_X}$) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because CY7C1480V33 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ Write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) ADSP is deasserted HIGH, (3) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (4) the appropriate combination of the Write inputs (GW, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a Write to the desired byte(s). $\overline{ADSC}$-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The $\overline{ADV}$ input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because CY7C1480V33 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1480V33 provides a two-bit wraparound counter, fed by A1:A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, ADSP, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2$ V	–	120	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to Sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit Sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for CY7C1480V33 follows. [4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-State
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-State
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
WRITE Cycle,Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
WRITE Cycle,Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

4. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
5. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
6. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
7. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of $\overline{ADSC}$. As a result, OE must be driven HIGH before the start of the write cycle to allow the outputs to tri-state. OE is a "don't care" for the remainder of the write cycle.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The following is a Truth Table for Read/Write for the CY7C1480V33. [9]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Note
9. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND ..... –0.3 V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [10, 11]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	For 3.3 V I/O		3.135	V_{DD}	V
		For 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	For 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		For 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	For 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		For 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage[10]	For 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		For 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage[10]	For 3.3 V I/O		–0.3	0.8	V
		For 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	5.0-ns cycle, 200 MHz	–	500	mA
			6.0-ns cycle, 167 MHz	–	450	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	5.0-ns cycle, 200 MHz	–	245	mA
			6.0-ns cycle, 167 MHz	–	245	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	All speeds	–	120	mA

Notes

10. Overshoot: $V_{IH(AC)}$ < V_{DD} +1.5 V (Pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL(AC)}$ > –2V (Pulse width less than $t_{CYC}/2$).
11. Power up: Assumes a linear ramp from 0 V to $V_{DD(min.)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [10, 11]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$	5.0-ns cycle, 200 MHz	–	245	mA
			6.0-ns cycle, 167 MHz	–	245	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	All speeds	–	135	mA

Capacitance

Parameter [12]	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{ADDRESS}$	Address input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6	pF
C_{DATA}	Data input capacitance		5	pF
C_{CTRL}	Control input capacitance		8	pF
C_{CLK}	Clock input capacitance		6	pF
$C_{I/O}$	Input/Output capacitance		5	pF

Thermal Resistance

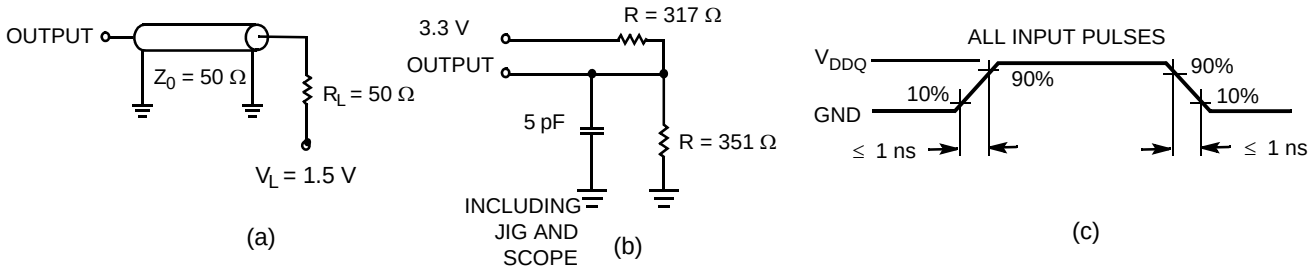
Parameter [12]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	24.63	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

Note
12. Tested initially and after any design or process change that may affect these parameters.

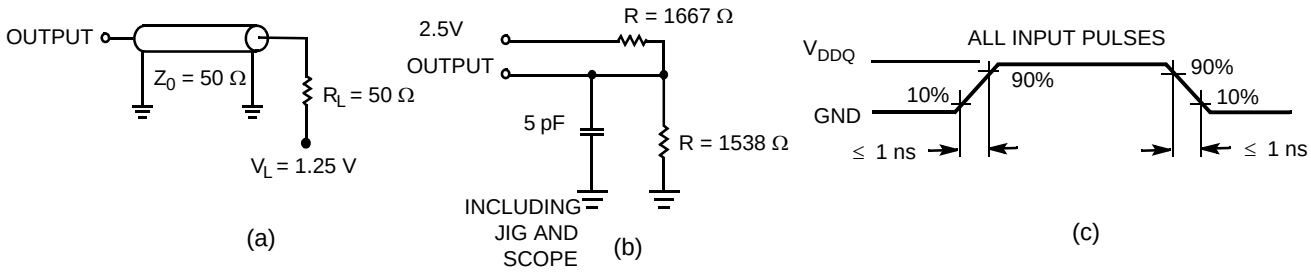
AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Switching Characteristics

Over the Operating Range

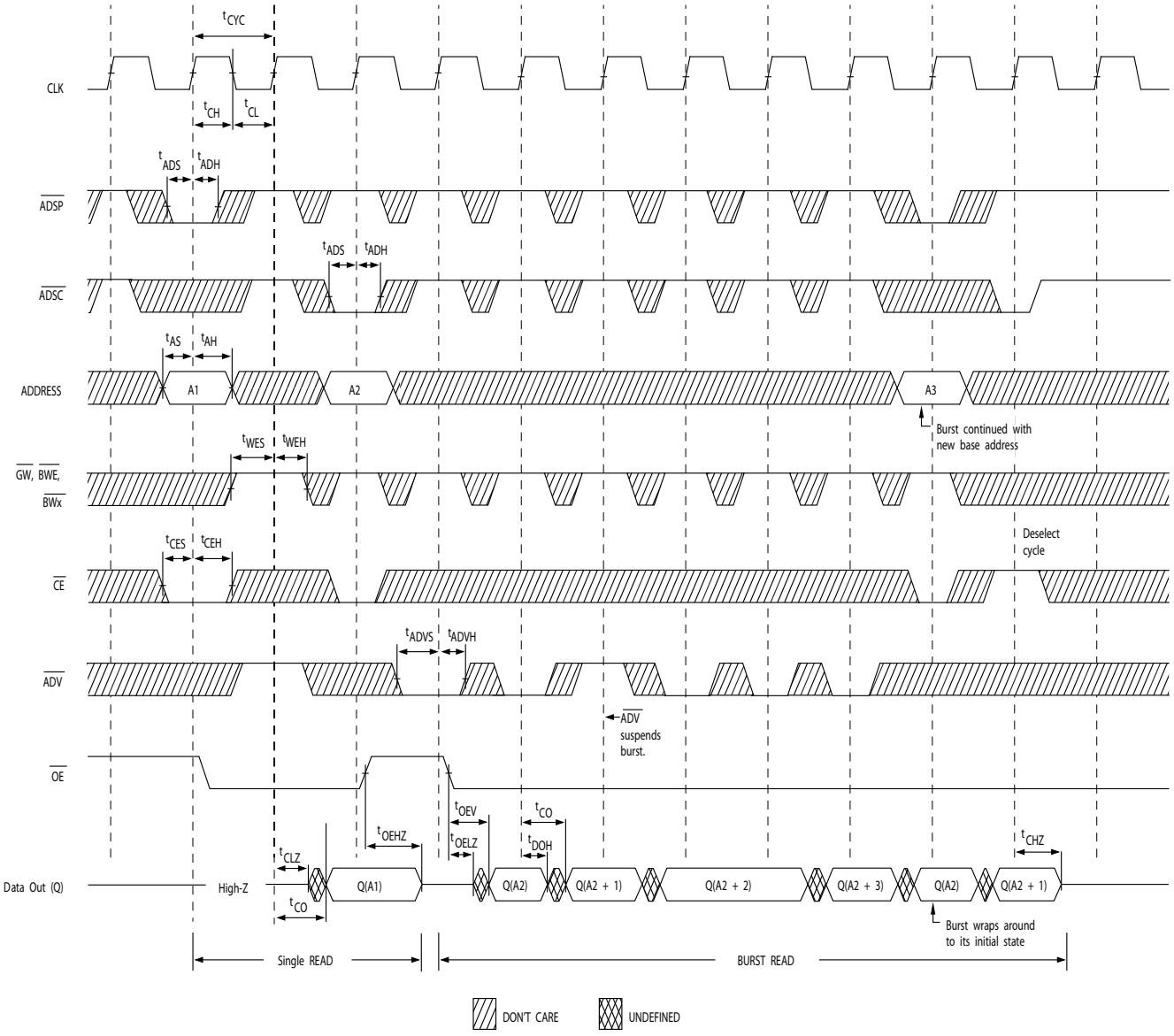
Parameter [13, 14]	Description	200 MHz		167 MHz		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the First Access [15]	1	–	1	–	ms
Clock						
t_{CYC}	Clock Cycle Time	5.0	–	6.0	–	ns
t_{CH}	Clock HIGH	2.0	–	2.4	–	ns
t_{CL}	Clock LOW	2.0	–	2.4	–	ns
Output Times						
t_{CO}	Data Output Valid After CLK Rise	–	3.0	–	3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3	–	1.5	–	ns
t_{CLZ}	Clock to Low Z [16, 17, 18]	1.3	–	1.5	–	ns
t_{CHZ}	Clock to High Z [16, 17, 18]	–	3.0	–	3.4	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	–	3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [16, 17, 18]	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [16, 17, 18]	–	3.0	–	3.4	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.4	–	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise	1.4	–	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.4	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.4	–	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.4	–	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.4	–	1.5	–	ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.4	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.4	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.4	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.4	–	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.4	–	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4	–	0.5	–	ns

Notes

13. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
14. Test conditions shown in (a) of Figure 2 on page 12 unless otherwise noted.
15. This part has an internal voltage regulator; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 12. Transition is measured ±200 mV from steady-state voltage.
17. At any possible voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z before Low-Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms

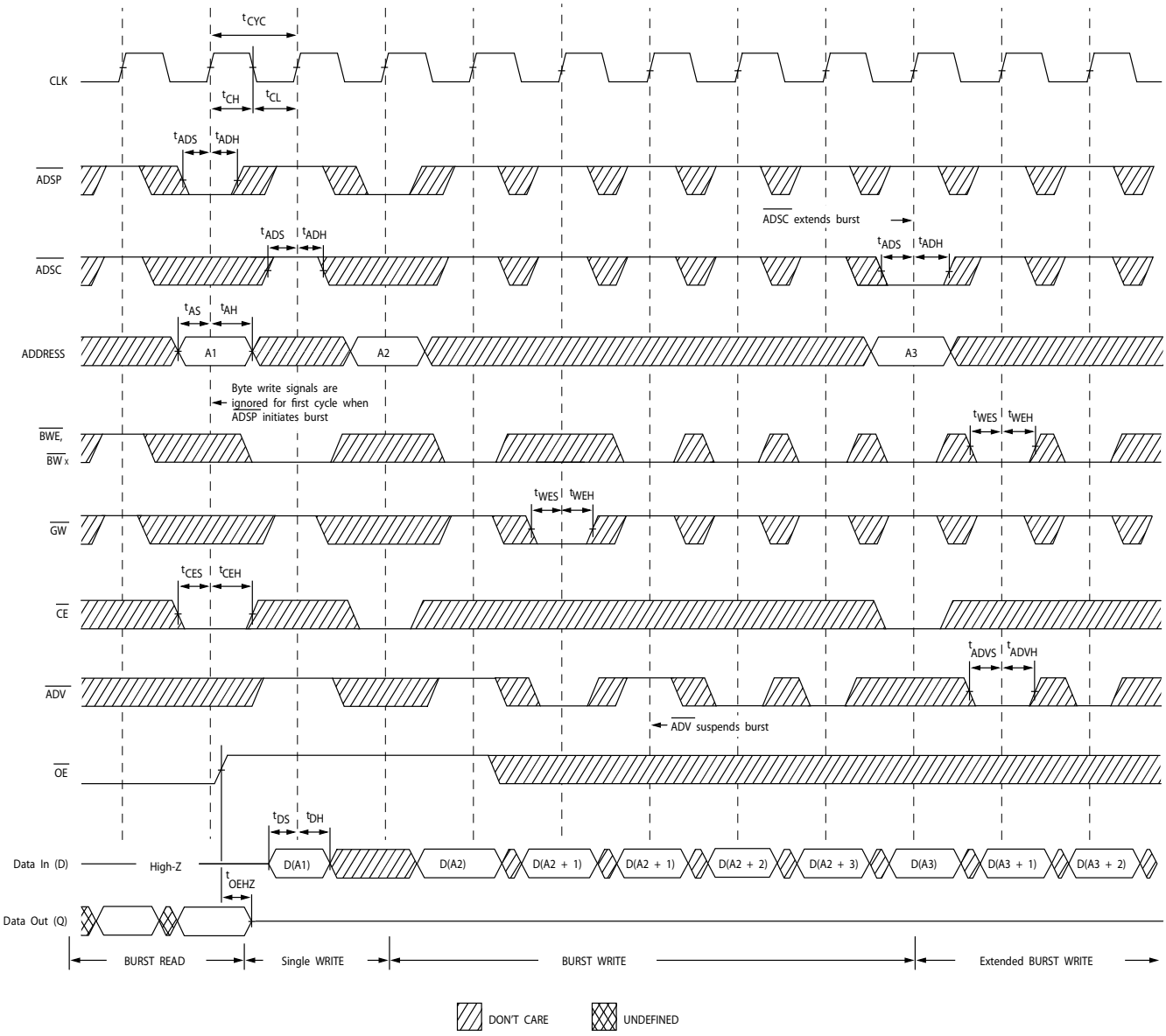
Figure 3. Read Cycle Timing [19]



Note
19. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Figure 4. Write Cycle Timing [20, 21]

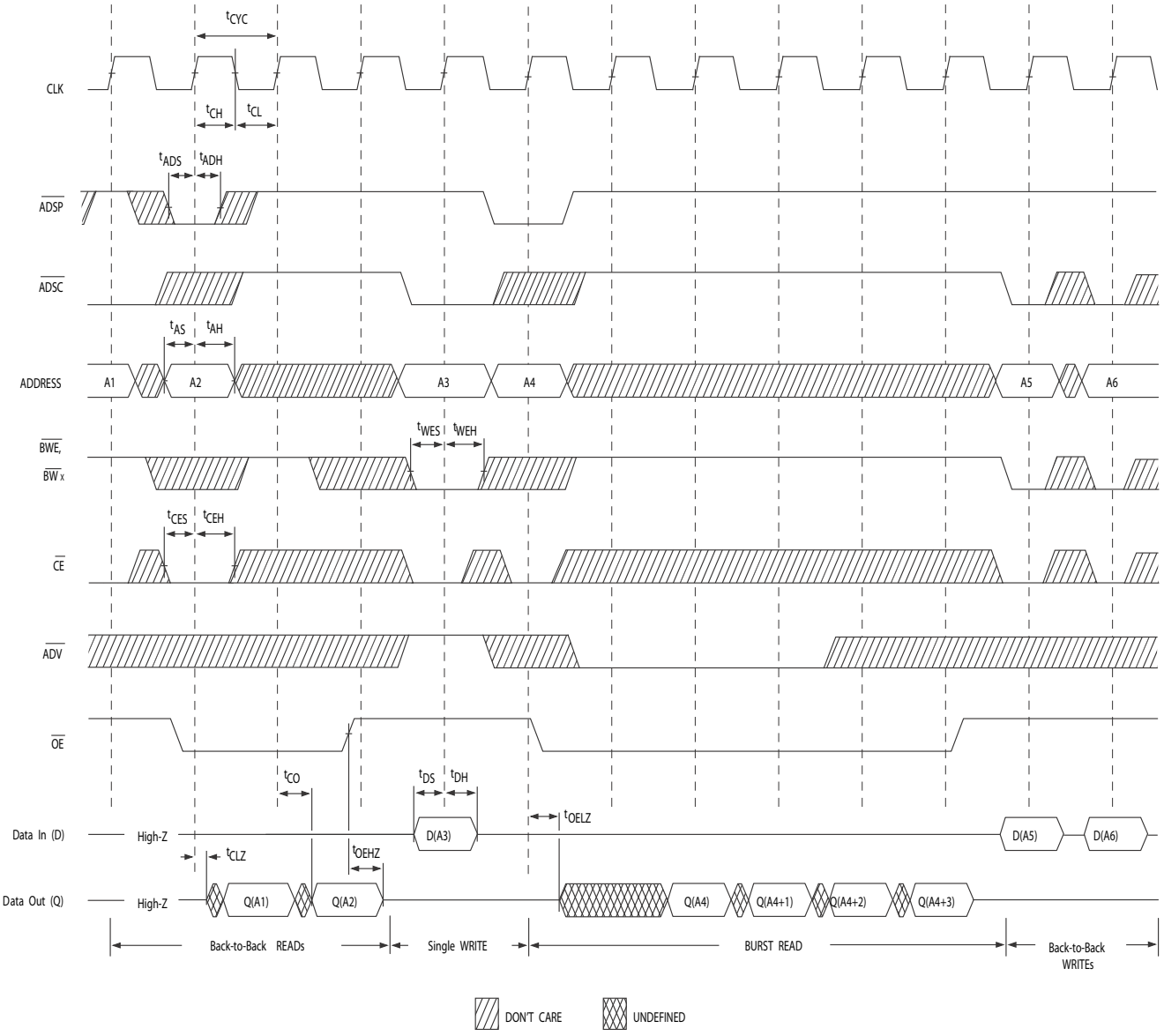


Notes

20. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
21. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

Switching Waveforms (continued)

Figure 5. Read/Write Cycle Timing [22, 23, 24]

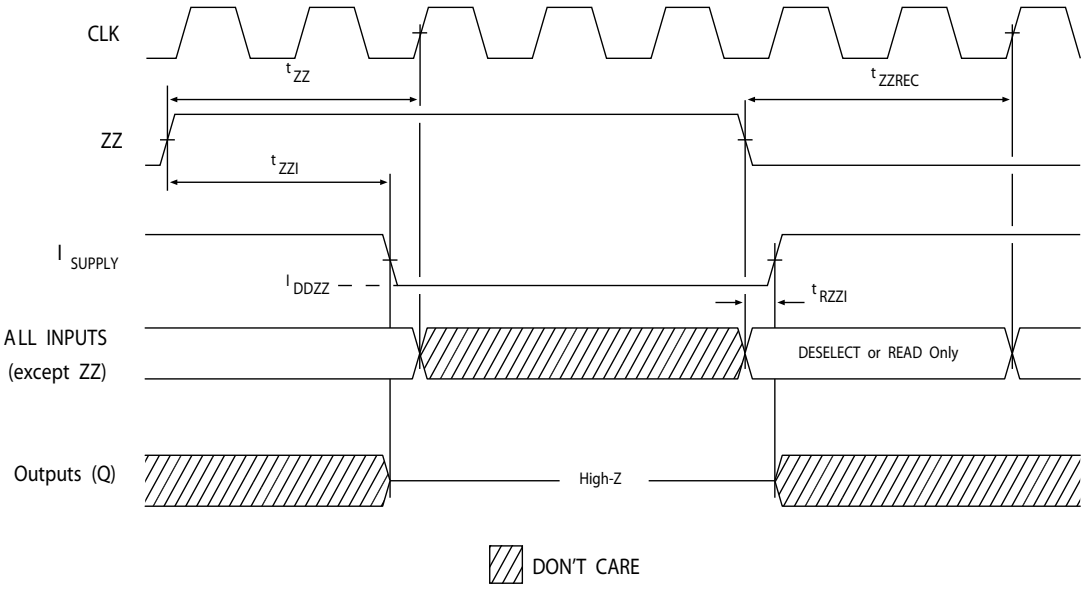


Notes

22. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
23. The data bus (Q) remains in high Z following a write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
24. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)

Figure 6. ZZ Mode Timing [25, 26]

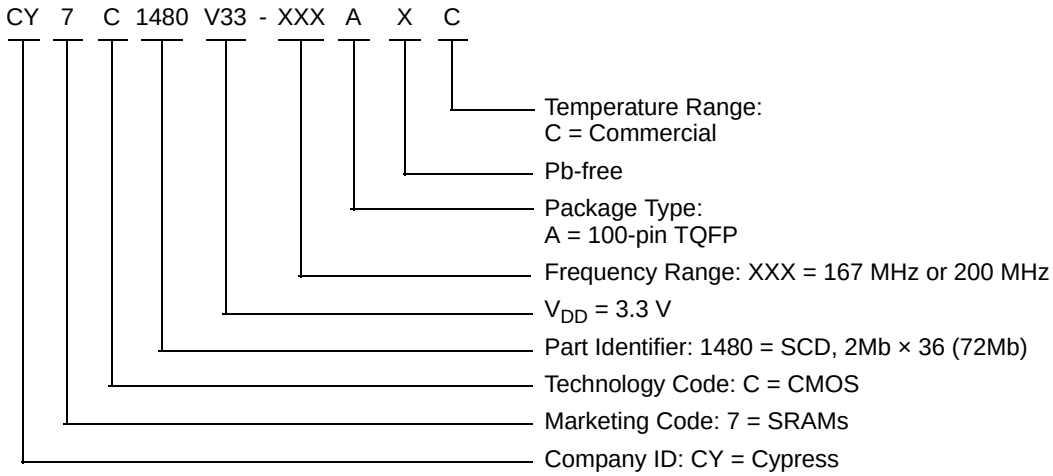


Notes
25. Device must be deselected when entering ZZ mode. See "Truth Table" on page 8 for all possible signal conditions to deselect the device.
26. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

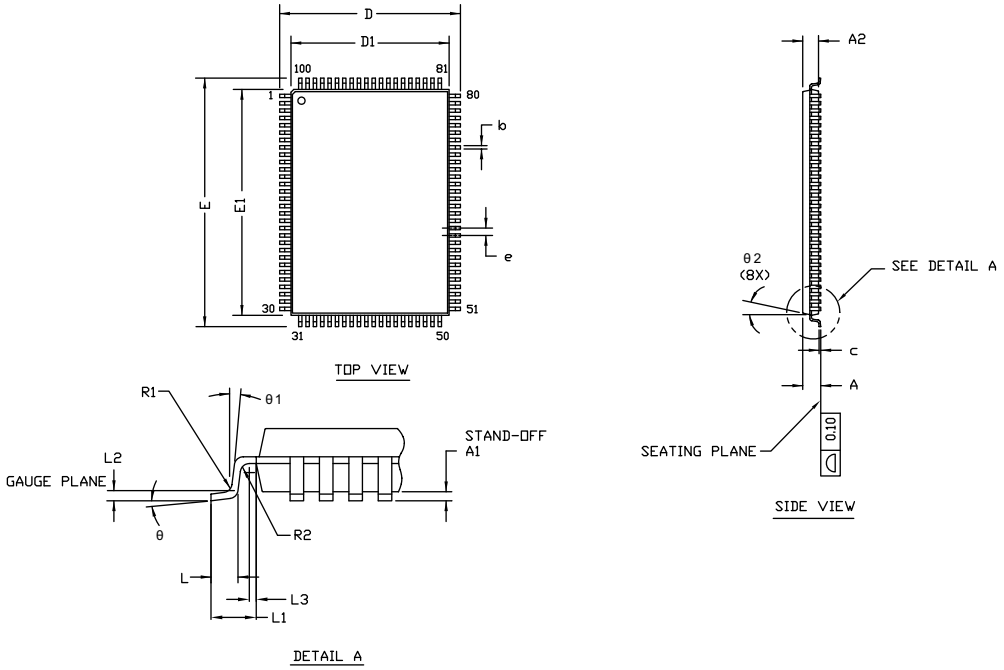
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1480V33-167AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
200	CY7C1480V33-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

Acronyms

Acronym	Description
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the Ram9 Sync/NoBL ZZ pin, JTAG, and Chip Enable issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

Part Numbers Affected

Density & Revision	Package Type	Operating Range
72Mb-Ram9 Synchronous SRAMs: CY7C148*V33	All packages	Commercial/Industrial

Product Status

All of the devices in the Ram9 72Mb Sync/NoBL family are qualified and available in production quantities.

Ram9 Sync/NoBL ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 72Mb Sync/NoBL family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	72M-Ram9 (90nm)	For the 72M Ram9 (90 nm) devices, this issue was fixed in the new revision. Please contact your local sales rep for availability.

1. ZZ Pin Issue

- PROBLEM DEFINITION

  The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS

  Device operated with ZZ pin left floating.

- SCOPE OF IMPACT

  When the ZZ pin is left floating, the device delivers incorrect data.

- WORKAROUND

  Tie the ZZ pin externally to ground.

- FIX STATUS

  Fix was done for the 72Mb RAM9 Synchronous SRAMs and 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

Table 1. List of Affected Devices and the new revision

Revision before the Fix	New Revision after the Fix
CY7C148*V33	CY7C148*BV33

Document History Page

Document Title: CY7C1480V33, 72-Mbit (2M × 36) Pipelined Sync SRAM Document Number: 38-05283				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	114670	PKS	08/06/02	New data sheet.
*A	118281	HGK	01/21/03	Changed status from Advanced Information to Preliminary. Updated Features (Removed 300 MHz frequency related information, updated package offering). Updated Selection Guide (Removed 300 MHz frequency related information). Updated Electrical Characteristics (Removed 300 MHz frequency related information). Updated Switching Characteristics (Removed 300 MHz frequency related information, changed maximum value of t_{CO} parameter from 2.4 ns to 2.6 ns for 250 MHz). Updated Ordering Information (Updated part numbers).
*B	233368	NJY	See ECN	Updated Features (Removed 250 MHz frequency related information and included 225 MHz frequency related information). Updated Functional Description. Updated Logic Block Diagrams (Corresponding to CY7C1480V33, CY7C1482V33, CY7C1486V33). Updated Selection Guide (Removed 250 MHz frequency related information and included 225 MHz frequency related information). Updated Functional Overview. Added Boundary Scan Exit Order (For all packages (Corresponding to CY7C1480V33, CY7C1482V33, CY7C1486V33)). Updated Electrical Characteristics (Removed 250 MHz frequency related information and included 225 MHz frequency related information, replaced the TBD's with their respective values for I_{DD}, I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} parameters). Updated Capacitance (Replaced values for all parameters for all Packages). Updated Thermal Resistance (Replaced values of Θ_{JA} and Θ_{JC} parameters from TBD to respective Thermal Values for all Packages). Updated Switching Characteristics (Removed 250 MHz frequency related information and included 225 MHz frequency related information). Updated Switching Waveforms. Updated Package Diagrams (Changed package outline for 165-ball FBGA package and 209-ball BGA package, removed 119-BGA package offering).
*C	299452	SYT	See ECN	Updated Features (Removed 225 MHz frequency related information and included 250 MHz frequency related information). Updated Selection Guide (Removed 225 MHz frequency related information and included 250 MHz frequency related information). Updated Electrical Characteristics (Removed 225 MHz frequency related information and included 250 MHz frequency related information). Updated Thermal Resistance (Changed values of Θ_{JA} parameter from 16.8 °C/W to 24.63 °C/W and Θ_{JC} parameter from 3.3 °C/W to 2.28 °C/W for 100-pin TQFP Package). Updated Switching Characteristics (Removed 225 MHz frequency related information and included 250 MHz frequency related information, changed minimum value of t_{CYC} parameter from 4.4 ns to 4.0 ns for 250 MHz frequency). Updated Ordering Information (Updated part numbers (Added Pb-free information for 100-pin TQFP, 165-ball FBGA and 209-ball BGA Packages), added 'Pb-free BG packages availability' comment below the Ordering Information).

Document History Page (continued)

Document Title: CY7C1480V33, 72-Mbit (2M × 36) Pipelined Sync SRAM Document Number: 38-05283				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	323080	PCI	See ECN	Updated Selection Guide (Unshaded 200 MHz and 167 MHz frequency related information). Updated Pin Configurations (Modified Address expansion pins/balls in the pinouts for all packages as per JEDEC standard). Updated Pin Definitions. Added Truth Table for Read/Write (Corresponding to CY7C1486V33). Added Note "BWx represents any byte write signal BW[0..7].To enable any byte write BWx, a Logic LOW signal should be applied at clock rise. Any number of bye writes can be enabled at the same time for any given write." and referred the same note in that table). Updated Operating Range (Added Industrial Operating Range). Updated Electrical Characteristics (Unshaded 200 MHz and 167 MHz frequency related information, Updated test conditions for $V_{OL,}$ V_{OH} parameters). Updated Switching Characteristics (Unshaded 200 MHz and 167 MHz frequency related information). Updated Ordering Information (Updated part numbers, removed 'Pb-free BG packages availability' comment below the Ordering Information).
*E	416193	NXR	See ECN	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court". Updated Electrical Characteristics (Updated Note 11 (Changed test condition from $V_{IH} \le V_{DD}$ to $V_{IH} < V_{DD}$), changed "Input Load Current except ZZ and MODE" to "Input Leakage Current except ZZ and MODE", changed minimum value of I_X parameter (corresponding to Input current of MODE (Input = V_{SS})) from –5 μA to –30 μA, changed maximum value of I_X parameter (corresponding to Input current of MODE (Input = V_{DD})) from 30 μA to 5 μA respectively, changed minimum value of I_X parameter (corresponding to Input current of ZZ (Input = V_{SS})) from –30 μA to –5 μA, changed maximum value of I_X parameter (corresponding to Input current of ZZ (Input = V_{DD})) from 5 μA to 30 μA respectively). Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table).
*F	470723	VKN	See ECN	Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated TAP AC Switching Characteristics (Changed minimum value of t_{TH} and t_{TL} parameters from 25 ns to 20 ns, changed maximum value of t_{TDOV} parameter from 5 ns to 10 ns). Updated Ordering Information (Updated part numbers).
*G	486690	VKN	See ECN	Updated Pin Configurations (Corrected the typo in the figure 209-ball FBGA pinout (Corrected the ball name H9 to V_{SS} from V_{SSQ})).
*H	1026720	VKN	See ECN	Updated Pin Definitions (Added Note 3 and referred the same note in V_{SSQ} pin).
*I	2898501	NJY	03/24/2010	Updated Ordering Information (Removed inactive parts from Ordering Information table) Updated Package Diagrams.
*J	3067398	NJY	10/20/10	Updated Ordering Information (The part CY7C1480V33-250AXC found to be in "EOL Prune" state in Oracle PLM is removed from the ordering information table) and added Ordering Code Definitions.
*K	3257192	NJY	05/14/2011	Updated Package Diagrams. Added Acronyms and Units of Measure. Updated to new template.

Document History Page (continued)

Document Title: CY7C1480V33, 72-Mbit (2M × 36) Pipelined Sync SRAM Document Number: 38-05283				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	3596931	NJY	04/23/2012	Updated Features (Removed 250 MHz frequency related information, removed CY7C1482V33, CY7C1486V33 related information, removed 165-ball FBGA package, 209-ball FBGA package related information). Updated Functional Description (Removed CY7C1482V33, CY7C1486V33 related information, removed the Note “For best practices recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines.” and its reference). Updated Selection Guide (Removed 250 MHz frequency related information). Removed Logic Block Diagram – CY7C1482V33. Removed Logic Block Diagram – CY7C1486V33. Updated Pin Configurations (Removed CY7C1482V33, CY7C1486V33 related information, removed 165-ball FBGA pakcage, 209-ball FBGA package related information). Updated Functional Overview (Removed CY7C1482V33, CY7C1486V33 related information). Updated Truth Table (Removed CY7C1482V33, CY7C1486V33 related information). Removed Truth Table for Read/Write (Corresponding to CY7C1482V33, CY7C1486V33). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed TAP Controller State Diagram. Removed TAP Controller Block Diagram. Removed TAP Timing. Removed TAP AC Switching Characteristics. Removed 3.3 V TAP AC Test Conditions. Removed 3.3 V TAP AC Output Load Equivalent. Removed 2.5 V TAP AC Test Conditions. Removed 2.5 V TAP AC Output Load Equivalent. Removed TAP DC Electrical Characteristics and Operating Conditions. Removed Identification Register Definitions. Removed Scan Register Sizes. Removed Identification Codes. Removed Boundary Scan Exit Order (Corresponding to CY7C1480V33, CY7C1482V33, CY7C1486V33). Updated Operating Range (Removed Industrial Temperature Range). Updated Electrical Characteristics (Removed 250 MHz frequency related information). Updated Capacitance (Removed 165-ball FBGA pakcage, 209-ball FBGA package related information). Updated Thermal Resistance (Removed 165-ball FBGA pakcage, 209-ball FBGA package related information). Updated Switching Characteristics (Removed 250 MHz frequency related information). Updated Package Diagrams (Removed 165-ball FBGA pakcage (spec 51-85165), 209-ball FBGA package (spec 51-85167) related information). Replaced all instances of IO with I/O across the document.
*M	3971185	NJY	04/23/2013	Added Errata. Completing Sunset Review.
*N	4033875	NJY	06/19/2013	Added Errata Footnotes. Updated to new template.
*O	4397427	PRIT	06/03/2014	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Completing Sunset Review.

Document History Page (continued)

Document Title: CY7C1480V33, 72-Mbit (2M × 36) Pipelined Sync SRAM Document Number: 38-05283				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	4572829	PRIT	11/18/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*Q	5857616	AJU	08/18/2017	Updated Package Diagrams: spec 51-85050 – Changed revision from *E to *G. Updated to new template. Completing Sunset Review.

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