

TLV6208x 1.2-A and 2-A High-Efficiency Step-Down Converter in 2-mm × 2-mm WSON Package

1 Features

- DCS-Control™ Architecture for Fast Transient Regulation
- 2.5 to 6-V Input Voltage Range (TLV62080)
- 2.7 to 6-V Input Voltage Range (TLV62084, TLV62084A)
- 100% Duty Cycle for Lowest Dropout
- Power Save Mode for Light Load Efficiency
- Output Discharge Function
- Power Good Output
- Thermal Shutdown
- Available in 2 mm × 2 mm 8-Terminal WSON Package
- For Improved Features Set, see the [TPS62080](#)
- Create a Custom Design Using the TLV6208x With the [WEBENCH® Power Designer](#)

2 Applications

- Battery-Powered Portable Devices
- Point-of-Load Regulators
- PC, Notebook, Server
- Set Top Box
- Solid State Drive (SSD), Memory Supply

3 Description

The TLV6208x family devices are small buck converters with few external components, enabling cost effective solutions. They are synchronous step-down converters with an input voltage range of 2.5 and 2.7 (2.5 V for TLV62080, 2.7 V for TLV62084x) to 6 V. The TLV6208x devices focus on high-efficiency step-down conversion over a wide output current range. At medium to heavy loads, the TLV6208x converters operate in PWM mode and automatically enter power save mode operation at light-load currents to maintain high efficiency over the entire load current range.

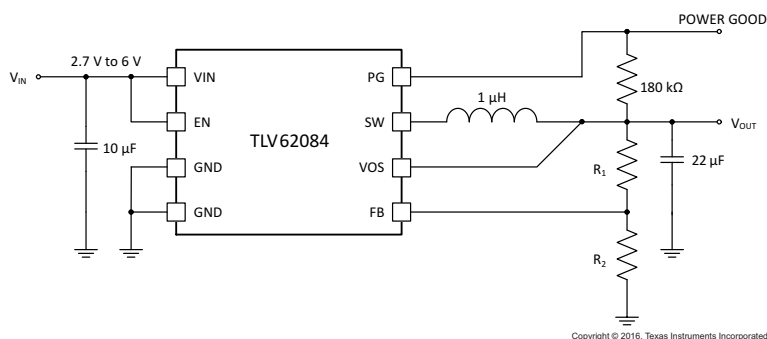
To address the requirements of system power rails, the internal compensation circuit allows a wide range of external output capacitor values. With the DCS-Control™ (Direct Control with Seamless transition into Power save mode) architecture excellent load transient performance and output voltage regulation accuracy are achieved. The devices are available in 2-mm × 2-mm WSON package with Thermal Pad.

Device Information⁽¹⁾

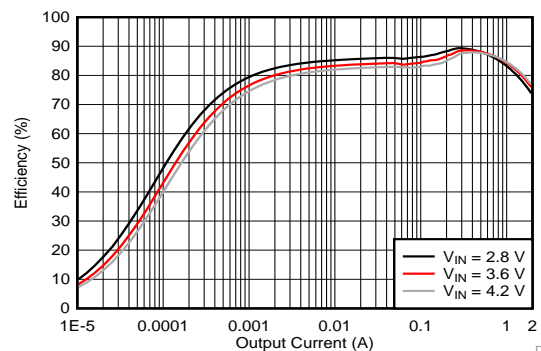
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------------|----------|-------------------|
| TLV62080 | WSON (8) | 2.00 mm × 2.00 mm |
| TLV62084, TLV62084A | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Efficiency vs Output Current, V_{OUT} = 1.2V



D002



Table of Contents

| | |
|---|--|
| 1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Device Comparison Table 4 6 Pin Configuration and Functions 4 7 Specifications 5 7.1 Absolute Maximum Ratings 5 7.2 ESD Ratings..... 5 7.3 Recommended Operating Conditions 5 7.4 Thermal Information 5 7.5 Electrical Characteristics..... 6 7.6 Typical Characteristics 7 8 Detailed Description 9 8.1 Overview 9 8.2 Functional Block Diagram 9 8.3 Feature Description..... 9 8.4 Device Functional Modes..... 11 | 9 Application and Implementation 12 9.1 Application Information..... 12 9.2 Typical Application 12 10 Power Supply Recommendations 18 11 Layout 18 11.1 Layout Guidelines 18 11.2 Layout Example 18 11.3 Thermal Considerations 19 12 Device and Documentation Support 20 12.1 Device Support..... 20 12.2 Documentation Support 20 12.3 Related Links 20 12.4 Trademarks 20 12.5 Electrostatic Discharge Caution..... 20 12.6 Receiving Notification of Documentation Updates 21 12.7 Community Resources..... 21 12.8 Glossary 21 13 Mechanical, Packaging, and Orderable Information 21 |
|---|--|

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (September 2016) to Revision H | Page |
|---|------|
| • Added WEBENCH® information to <i>Features</i> , <i>Detailed Design Procedure</i> , and <i>Device Support</i> sections..... | 1 |
| • Added SW (AC, less than 10 ns) to the <i>Absolute Maximum Rating</i> table | 5 |
| Changes from Revision F (January 2015) to Revision G | Page |
| • Added TLV62084A device and Applications | 1 |
| • Added Power Good Pin Logic Table (TLV62080/84) and Power Good Pin Logic Table (TLV62084A) | 10 |
| • Added scale factors in Figure 14 | 16 |
| • Changed PCB Layout Image | 18 |
| • Added Receiving Notification of Documentation Updates and Community Resources sections..... | 21 |
| Changes from Revision E (February 2014) to Revision F | Page |
| • Changed <i>Device Information</i> table. | 1 |
| • Renamed the Configuration and Functions section | 4 |
| • Added new TI-Legal note to Application and Implementation section. | 12 |
| • Renamed "Thermal Information" to Thermal Considerations | 19 |
| Changes from Revision D (June 2013) to Revision E | Page |
| • Added the <i>Device Information</i> table, <i>Power Supply Recommendations</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections | 1 |
| • Clarified the input voltage ranges of 2.5 V to 5.5 V for the TLV62080 device and 2.7 V to 5.5 V for the TLV62084 device | 1 |
| • Changed the Ordering Information table to the Device Comparison table and removed the Package Marking, T _A , and Package columns from the table | 4 |

| | |
|---|----|
| • Changed the word <i>pin</i> to <i>terminal</i> in most cases throughout the document | 4 |
| • Added the <i>Handling Ratings</i> table which now contains the storage temperature range and ESD ratings | 5 |
| • Added I _{LIM} range for TLV62084 in <i>Electrical Characteristics</i> table..... | 6 |
| • Added the higher output voltage graphs " <i>Output Voltage vs Load Current</i> ", <i>Figure 6</i> , <i>Figure 7</i> in the <i>Typical Characteristics</i> section..... | 7 |
| • Replaced the " <i>Switching Frequency vs Load Current</i> " graph to the new " <i>Switching Frequency vs Output Current</i> " graph in the <i>Typical Characteristics</i> section | 7 |
| • Replaced the TLV62080 typical application circuit with the circuit for the TLV62084..... | 12 |
| • Deleted the <i>Parameter Measurement Information</i> Section and moved image and list of components to <i>Typical Application</i> section..... | 12 |
| • Added <i>Table 4</i> to the <i>Design Requirements</i> section | 12 |
| • Added Moved Waveforms from the <i>Typical Characteristics</i> section into the <i>Application Curves</i> section. Changed L _{COIL} (coil inductance) to I _{COIL} (coil current) in the <i>Typical Application (PWM Mode and PFM Mode)</i> , <i>Load Transient</i> , <i>Line Transient</i> , and <i>Startup</i> waveforms..... | 15 |
| • Added the output capacitance and inductance conditions to the first (original) <i>Load Transient</i> graph..... | 16 |
| • Added the second <i>Load Transient</i> graph (<i>Figure 14</i>) | 16 |

| Changes from Revision C (May 2013) to Revision D | Page |
|---|-------------|
| • Deleted TLV62084 device number from datasheet..... | 19 |

| Changes from Revision B (July 2012) to Revision C | Page |
|---|-------------|
| • Changed the <i>Thermal Information</i> table values | 5 |

| Changes from Revision A (November 2011) to Revision B | Page |
|--|-------------|
| • Changed QFN to SON in <i>ORDERING INFORMATION</i> | 4 |
| • Changed QFN to SON in <i>DEVICE INFORMATION</i> | 4 |
| • Changed Thermal Pad description in <i>Pin Functions</i> | 4 |
| • Changed T _J in the <i>Absolute Maximum Ratings</i> ⁽¹⁾ From: –40 to 125°C To: -40 to 150°C | 5 |
| • Changed several instances of DSC to DCS in <i>DEVICE OPERATION</i> section..... | 9 |
| • Changed DSC to DCS in <i>Functional Block Diagram</i> | 9 |

| Changes from Original (October 2011) to Revision A | Page |
|---|-------------|
| • Changed pin VSNS to VOS in <i>Figure 9</i> | 12 |
| • Changed pin VSNS to VOS in <i>Figure 10</i> | 15 |

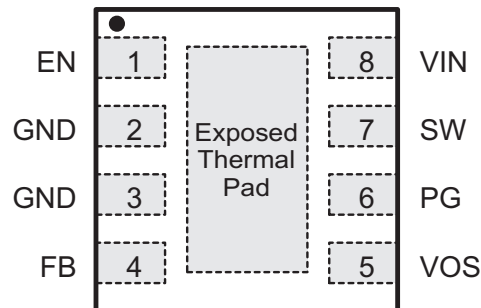
5 Device Comparison Table

| PART NUMBER ⁽¹⁾ | INPUT VOLTAGE | OUTPUT CURRENT | Power Good Logic Level (EN=Low) |
|----------------------------|---------------|----------------|---------------------------------|
| TLV62080 | 2.5 V to 6 V | 1.2 A | High Impedance |
| TLV62084 | 2.7 V to 6 V | 2 A | High Impedance |
| TLV62084A | 2.7 V to 6 V | 2 A | Low |

(1) For detailed ordering information please check the [Mechanical, Packaging, and Orderable Information](#) section at the end of this datasheet.

6 Pin Configuration and Functions

8-Pin WSON With Thermal Pad
DSG Package
(Top View)



Pin Functions

| PIN | | I/O | DESCRIPTION |
|---------------------|------|-----|--|
| NO. | NAME | | |
| 1 | EN | IN | Device enable logic input. Do not leave floating. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown. |
| 2, 3 | GND | PWR | Power and signal ground. |
| 4 | FB | IN | Feedback terminal for the internal control loop. Connect this terminal to the external feedback divider to program the output voltage. |
| 5 | VOS | IN | Output voltage sense terminal for the internal control loop. Must be connected to output. |
| 6 | PG | OUT | Power Good open drain output. This terminal is pulled to low if the output voltage is below regulation limits. This terminal can be left floating if not used. |
| 7 | SW | PWR | Switch terminal connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here. |
| 8 | VIN | PWR | Power supply voltage input. |
| Exposed Thermal Pad | | — | Must be connected to GND. Must be soldered to achieve appropriate power dissipation and mechanical reliability. |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---|------|-----------------------|------|
| Voltage range ⁽²⁾ | VIN, PG, VOS | -0.3 | 7 | V |
| | SW | -0.3 | V _{IN} + 0.3 | V |
| | SW (AC, less than 10 ns) ⁽³⁾ | -3.0 | 10 | V |
| | FB | -0.3 | 3.6 | V |
| | EN | -0.3 | V _{IN} + 0.3 | V |
| Power Good Sink Current | PG | | 1 | mA |
| Operating junction temperature range, T _J | | -40 | 150 | °C |
| Storage temperature range, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM) ESD stress voltage ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM) ESD stress voltage ⁽²⁾ | ±500 | V |

- (1) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

| | | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|------|
| V _{IN} | Input voltage range, TLV62080 | 2.5 | | 6 | V |
| V _{IN} | Input voltage range, TLV62084, TLV62084A | 2.7 | | 6 | V |
| T _J | Operating junction temperature | -40 | | 125 | °C |

- (1) Refer to the [Application Information](#) section for further information.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TLV6208x DSG (8 PINS) | UNITS |
|-------------------------------|--|-----------------------------|-------|
| θ _{JA} | Junction-to-ambient thermal resistance | 59.7 | °C/W |
| θ _{JCtop} | Junction-to-case (top) thermal resistance | 70.1 | °C/W |
| θ _{JB} | Junction-to-board thermal resistance | 30.9 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.4 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 31.5 | °C/W |
| θ _{JCbot} | Junction-to-case (bottom) thermal resistance | 8.6 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Over recommended free-air temperature range, $T_A = -40^{\circ}\text{C}$ to 85°C , typical values are at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted), $V_{IN} = 3.6\text{ V}$.

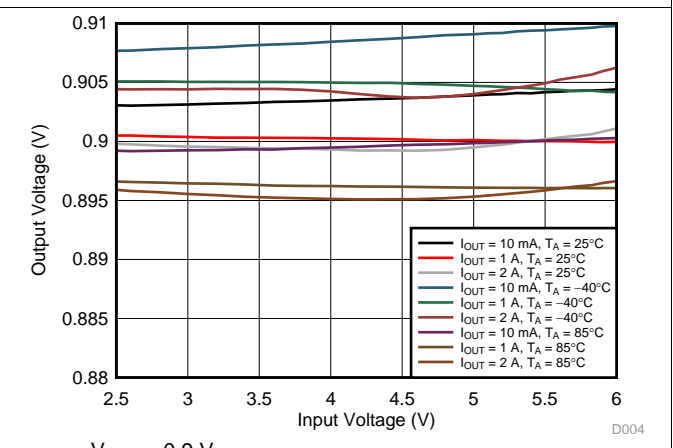
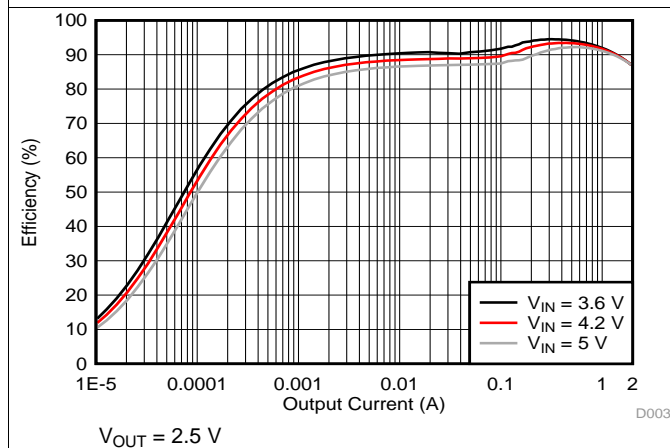
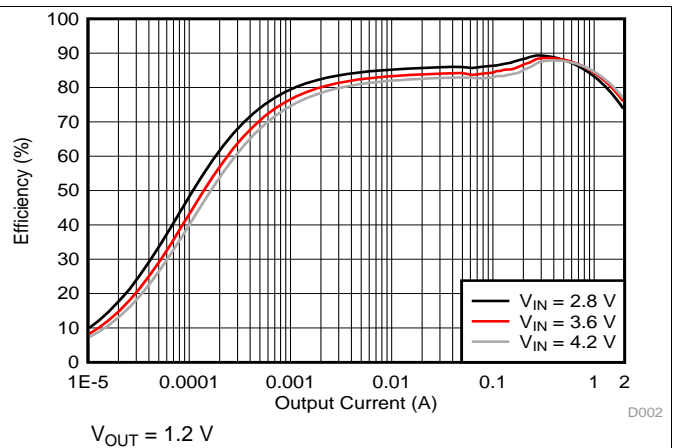
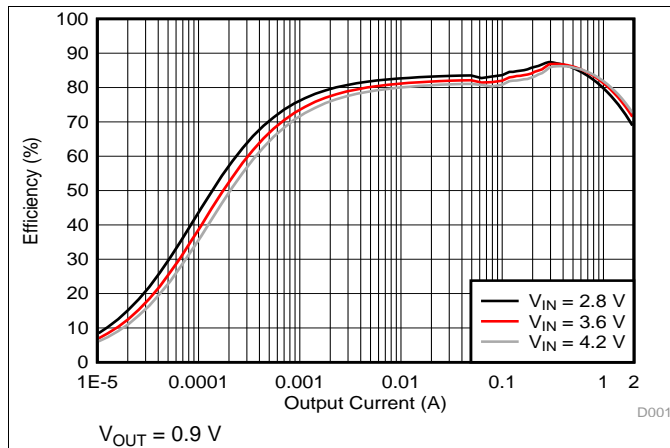
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|---|---|-------|------|-------|--------------------|
| SUPPLY | | | | | | |
| V_{IN} | Input voltage range, TLV62080 | | 2.5 | | 6 | V |
| V_{IN} | Input voltage range, TLV62084, TLV62084A | | 2.7 | | 6 | V |
| I_Q | Quiescent current into V_{IN} | $I_{OUT} = 0\text{ mA}$, Device not switching | | 30 | | μA |
| I_{SD} | Shutdown current into V_{IN} | EN = LOW | | | 1 | μA |
| V_{UVLO} | Under voltage lock out | Input voltage falling | | 1.8 | 2 | V |
| | Under voltage lock out hysteresis | Rising above V_{UVLO} | | 120 | | mV |
| T_{JSD} | Thermal shutdown | Temperature rising | | 150 | | $^{\circ}\text{C}$ |
| | Thermal shutdown hysteresis | Temperature falling below T_{JSD} | | 20 | | $^{\circ}\text{C}$ |
| LOGIC INTERFACE (EN) | | | | | | |
| V_{IH} | High level input voltage | $2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$ | 1 | | | V |
| V_{IL} | Low level input voltage | $2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$ | | | 0.4 | V |
| I_{LKG} | Input leakage current | | | 0.01 | 0.5 | μA |
| POWER GOOD | | | | | | |
| V_{PG} | Power good threshold | V_{OUT} falling referenced to V_{OUT} nominal | -15 | -10 | -5 | % |
| | Power good hysteresis | | | 5 | | % |
| V_{OL} | Low level voltage | $I_{sink} = 500\ \mu\text{A}$ | | | 0.3 | V |
| $I_{PG,LKG}$ | PG Leakage current | $V_{PG} = 5.0\text{ V}$ | | 0.01 | 0.1 | μA |
| OUTPUT | | | | | | |
| V_{OUT} | Output voltage range | | 0.5 | | 4 | V |
| V_{FB} | Feedback regulation voltage | $V_{IN} \geq 2.5\text{ V}$ and $V_{IN} \geq V_{OUT} + 1\text{ V}$ | 0.438 | 0.45 | 0.462 | V |
| I_{FB} | Feedback input bias current | $V_{FB} = 0.45\text{ V}$ | | 10 | 100 | nA |
| R_{DIS} | Output discharge resistor | EN = LOW, $V_{OUT} = 1.8\text{ V}$ | | 1 | | k Ω |
| $R_{DS(on)}$ | High side FET on-resistance | $I_{SW} = 500\text{ mA}$ | | 120 | | m Ω |
| | Low side FET on-resistance | $I_{SW} = 500\text{ mA}$ | | 90 | | m Ω |
| I_{LIM} | High side FET switch current-limit, TLV62080 | Rising inductor current | 1.6 | 2.8 | 4 | A |
| I_{LIM} | High side FET switch current-limit, TLV62084, TLV62084A | Rising inductor current | 2.3 | 2.8 | 4 | A |

7.6 Typical Characteristics

See [Typical Application](#) for characterization setup.

Table 1. Table of Graphs

| | | FIGURE |
|-------------------------|---|----------|
| Efficiency | Load current, $V_{OUT} = 0.9\text{ V}$ | Figure 1 |
| | Load current, $V_{OUT} = 1.2\text{ V}$ | Figure 2 |
| | Load current, $V_{OUT} = 2.5\text{ V}$ | Figure 3 |
| Output Voltage Accuracy | Input Voltage, $V_{OUT} = 0.9\text{ V}$ | Figure 4 |
| | Input Voltage, $V_{OUT} = 2.5\text{ V}$ | Figure 5 |
| | Load current, $V_{OUT} = 0.9\text{ V}$ | Figure 6 |
| | Load current, $V_{OUT} = 2.5\text{ V}$ | Figure 7 |
| Switching Frequency | Load current, $V_{OUT} = 2.5\text{ V}$ | Figure 8 |



TLV62080, TLV62084, TLV62084A

SLVSAK9H – OCTOBER 2011 – REVISED JANUARY 2017

www.ti.com

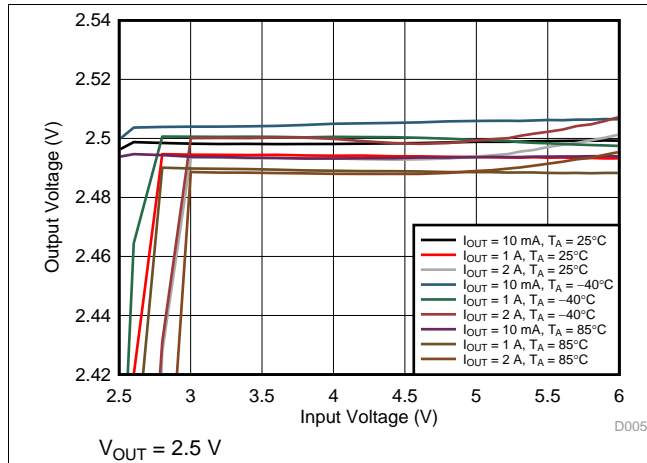


Figure 5. Output Voltage vs Input Voltage

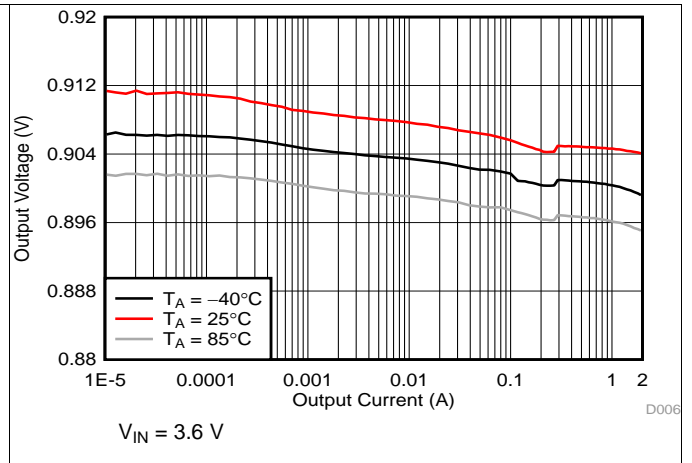


Figure 6. Output Voltage vs Load Current

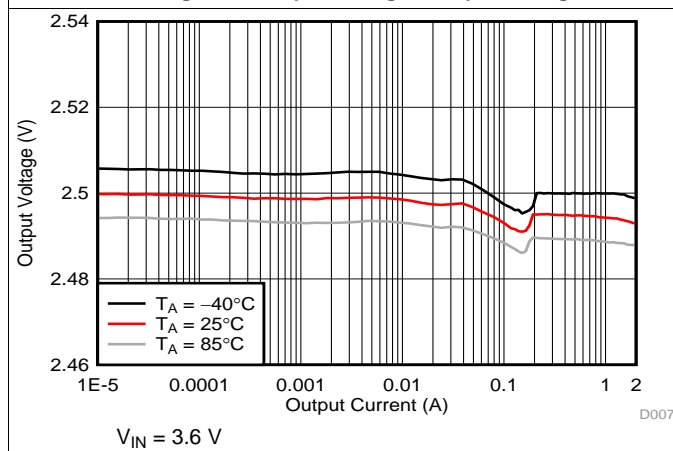


Figure 7. Output Voltage vs Load Current

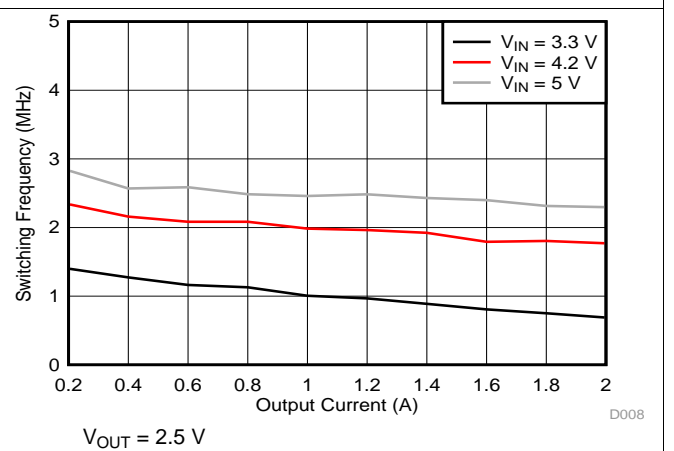


Figure 8. Switching Frequency vs Output Current

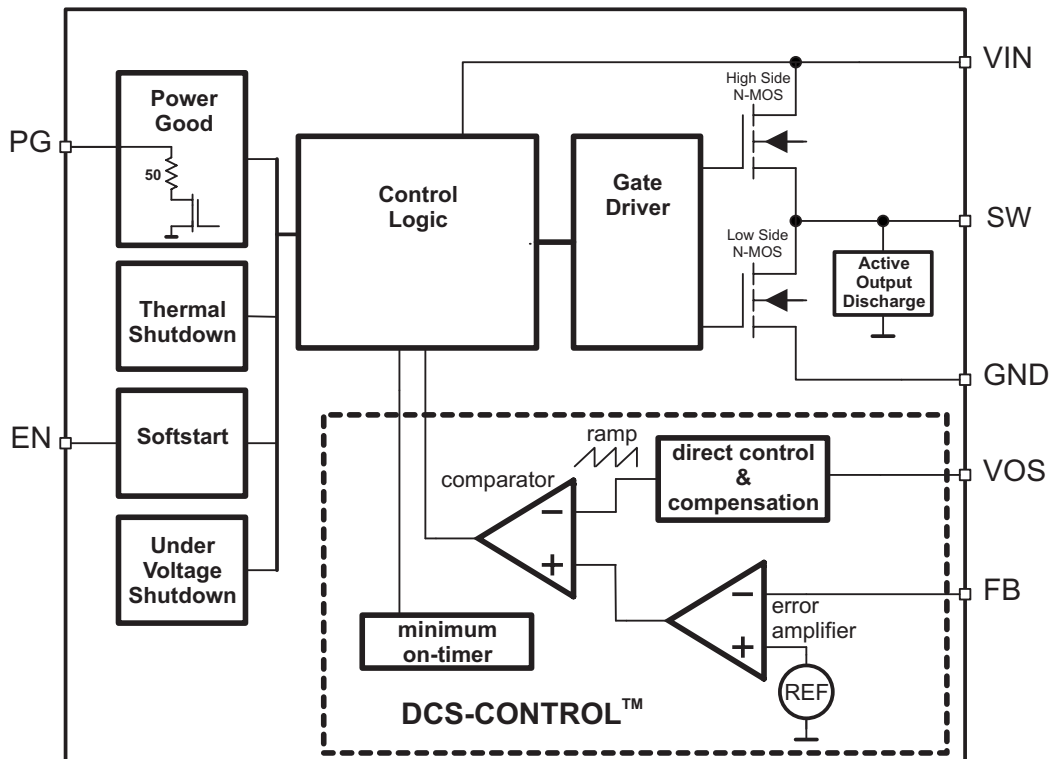
8 Detailed Description

8.1 Overview

The TLV62080 and TLV62084x synchronous switched-mode converters are based on DCS-Control™. DCS-Control™ is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode, the TLV6208x converter operates with the nominal switching frequency of 2 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes (PWM and PFM) using a single building block with a seamless transition from PWM to power save mode without effects on the output voltage. The TLV62080 and TLV62084x devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 100% Duty-Cycle Low-Dropout Operation

The devices offer low input-to-output voltage difference by entering the 100% duty-cycle mode. In this mode the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This mode is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. Equation 1 calculates the minimum input voltage to maintain regulation based on the load current and output voltage.

Feature Description (continued)

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L)$$

With:

- $V_{IN,MIN}$ = Minimum input voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance

(1)

8.3.2 Enabling and Disabling the Device

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the programmed threshold. The EN input must be terminated and not left floating.

8.3.3 Output Discharge

The output gets discharged through the SW terminal with a typical discharge resistor of R_{DIS} whenever the device shuts down (by disable, thermal shutdown or UVLO).

8.3.4 Soft Start

When EN is set to start device operation, the device starts switching after a delay of about 40 μ s and VOUT rises with a slope of about 10mV/ μ s (See [Figure 16](#) and [Figure 17](#) for typical startup operation). Soft start avoids excessive inrush current and creates a smooth output voltage rise slope. Soft start also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft start time, such as in the case of heavy load, the converter enters standard operation. Consequently, the inductor current limit operates as described in [Inductor Current-Limit](#). The TLV62080 and TLV62084x devices are able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

8.3.5 Power Good

The TLV62080 and TLV62084x devices have a power-good output going low when the output voltage is below the nominal value. The power good maintains high impedance once the output is above 95% of the regulated voltage, and is driven to low once the output voltage falls below typically 90% of the regulated voltage. The PG terminal is an open drain output and is specified to sink typically up to 0.5 mA. The power good output requires a pull-up resistor which is recommended connecting to the device output. When the device is off because of disable, UVLO, or thermal shutdown, the PG terminal is at high impedance. TLV62084A features PG=Low in these cases. [Table 2](#) and [Table 3](#) show the different PG operation for the TLV6208x and TLV62084A. The PG output can be left floating if unused.

Table 2. Power Good Pin Logic Table (TLV62080/84)

| Device Information | | PG Logic Status | |
|----------------------|----------------------------|-----------------|-----|
| | | High Z | Low |
| Enable (EN=High) | $V_{FB} \geq V_{PG}$ | √ | |
| | $V_{FB} \leq V_{PG}$ | | √ |
| Shutdown (EN=Low) | | √ | |
| UVLO | $0.7V < V_{IN} < V_{UVLO}$ | √ | |
| Thermal Shutdown | $T_J > T_{JSD}$ | √ | |
| Power Supply Removal | $V_{IN} < 0.7V$ | √ | |

Table 3. Power Good Pin Logic Table (TLV62084A)

| Device Information | | PG Logic Status | |
|----------------------|----------------------------|-----------------|-----|
| | | High Z | Low |
| Enable (EN=High) | $V_{FB} \geq V_{PG}$ | √ | |
| | $V_{FB} \leq V_{PG}$ | | √ |
| Shutdown (EN=Low) | | | √ |
| UVLO | $0.7V < V_{IN} < V_{UVLO}$ | | √ |
| Thermal Shutdown | $T_J > T_{JSD}$ | | √ |
| Power Supply Removal | $V_{IN} < 0.7V$ | √ | |

The PG signal can be used for sequencing of multiple rails by connecting to the EN terminal of other converters. Leave the PG terminal unconnected when not in use.

8.3.6 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout is implemented which shuts down the device at voltages lower than V_{UVLO} with a V_{HYS_UVLO} hysteresis.

8.3.7 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically T_{JSD} . Once the device temperature falls below the threshold, the device returns to normal operation automatically.

8.3.8 Inductor Current-Limit

The Inductor current-limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor, a heavy load, or shorted output circuit condition.

The incorporated inductor peak-current limit measures the current during the high-side and low-side power MOSFET on-phase. Once the high-side switch current-limit is tripped, the high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current. When the inductor current drops down to the low-side switch current-limit, the low-side MOSFET is turned off and the high-side switch is turned on again. This operation repeats until the inductor current does not reach the high-side switch current-limit. Because of an internal propagation delay, the real current-limit value exceeds the static-current limit in the [Electrical Characteristics](#) table.

8.4 Device Functional Modes

8.4.1 Power Save Mode

As the load current decreases, the TLV62080 and TLV62084x devices enter power save mode operation. During power save mode, the converter operates with a reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency. Power save mode occurs when the inductor current becomes discontinuous. Operation in power save mode is based on a fixed on time architecture. The typical on time is given by $t_{on} = 400 \text{ ns} \times (V_{OUT} / V_{IN})$. The switching frequency over the whole load current range is shown in [Figure 8](#).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are designed to operate from an input voltage supply range between 2.5 V (2.7 V for the TLV62084x devices) and 6 V with a maximum output current of 2 A (1.2 A for the TLV62080 device). The TLV6208x devices operate in PWM mode for medium to heavy load conditions and in power save mode at light load currents.

In PWM mode the TLV6208x converters operate with the nominal switching frequency of 2 MHz which provides a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range.

The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. See the [Documentation Support](#) section for additional documentation.

9.2 Typical Application

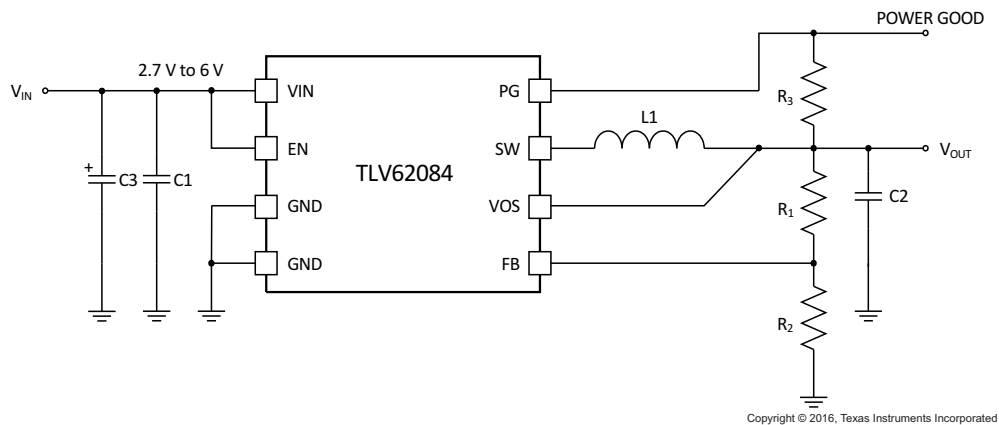


Figure 9. Typical Application Schematic

9.2.1 Design Requirements

Use the following typical application design procedure to select external components values for the TLV62084 device.

Table 4. Design Parameters

| DESIGN PARAMETERS | EXAMPLE VALUES |
|-----------------------|-------------------|
| Input Voltage Range | 2.8 V to 4.2 V |
| Output Voltage | 1.2 V |
| Transient Response | $\pm 5\% V_{OUT}$ |
| Input Voltage Ripple | 400 mV |
| Output Voltage Ripple | 30 mV |
| Output Current Rating | 2 A |
| Operating frequency | 2 MHz |

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62080 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Table 5. List of Components

| REFERENCE | DESCRIPTION | MANUFACTURER ⁽¹⁾ |
|-----------|---|-----------------------------|
| C1 | 10 μ F, Ceramic Capacitor, 6.3 V, X5R, size 0603 | Std |
| C2 | 22 μ F, Ceramic Capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L | Murata |
| C3 | 47 μ F, Tantalum Capacitor, 8 V, 35 m Ω , size 3528, T520B476M008ATE035 | Kemet |
| L1 | 1 μ H, Power Inductor, 2.2 A, size 3 mm \times 3 mm \times 1.2 mm, XFL3012-102MEB | Coilcraft |
| R1 | 65.3 k Ω , Chip Resistor, 1/16 W, 1%, size 0603 | Std |
| R2 | 39.2 k Ω , Chip Resistor, 1/16 W, 1%, size 0603 | Std |
| R3 | 178 k Ω , Chip Resistor, 1/16 W, 1%, size 0603 | Std |

(1) See [Third-party Products Disclaimer](#)

9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low pass frequency filter. To simplify this process [Table 6](#) outlines possible inductor and capacitor value combinations for the most application.

Table 6. Matrix of Output Capacitor and Inductor Combinations

| L [μ H] ⁽¹⁾ | C _{OUT} [μ F] ⁽¹⁾ | | | | |
|-----------------------------|--|---------------------|----|-----|-----|
| | 10 | 22 | 47 | 100 | 150 |
| 0.47 | | | | | |
| 1 | + | + ⁽²⁾⁽³⁾ | + | + | |
| 2.2 | + | + | + | + | |
| 4.7 | | | | | |

(1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.

(2) Plus signs (+) indicates recommended filter combinations.

(3) Filter combination in typical application.

9.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, [Equation 2](#) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

Where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

(2)

TI recommends choosing the saturation current for the inductor 20% to approximately 30% higher than the $I_{L,MAX}$, out of [Equation 2](#). A higher inductor value is also useful to lower ripple current, but increases the transient response time as well. The following inductors are recommended to be used in designs (see [Table 7](#)).

Table 7. List of Recommended Inductors

| INDUCTANCE [μH] | CURRENT RATING [mA] | DIMENSIONS L x W x H [mm ³] | DC RESISTANCE [mΩ typ] | TYPE | MANUFACTURER ⁽¹⁾ |
|--------------------|------------------------|--|---------------------------|---------------|-----------------------------|
| 1 | 2500 | 3 × 3 × 1.2 | 35 | XFL3012-102ME | Coilcraft |
| 1 | 1650 ⁽²⁾ | 3 × 3 × 1.2 | 40 | LQH3NPN1R0NJ0 | Murata |
| 2.2 | 2500 | 4 × 3.7 × 1.65 | 49 | LQH44PN2R2MP0 | Murata |
| 2.2 | 1600 ⁽²⁾ | 3 × 3 × 1.2 | 81 | XFL3012-222ME | Coilcraft |

(1) See [Third-party Products Disclaimer](#)

(2) Recommended for TLV62080 only due to limited current rating

9.2.2.4 Capacitor Selection

The input capacitor is the low impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those terminals. For most applications 10 μF is sufficient though a larger value reduces input current ripple.

The architecture of the TLV6208x device allows use of tiny ceramic-type output capacitors with low equivalent-series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends use of the X7R or X5R dielectric. The TLV62080 and TLV62084x devices are designed to operate with an output capacitance of 10 to 100 μF and beyond, as listed in [Table 6](#). Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

Table 8. List of Recommended Capacitors

| CAPACITANCE [μF] | TYPE | DIMENSIONS L x W x H [mm ³] | MANUFACTURER ⁽¹⁾ |
|---------------------|----------------|--|-----------------------------|
| 10 | GRM188R60J106M | 0603: 1.6 × 0.8 × 0.8 | Murata |
| 22 | GRM188R60G226M | 0603: 1.6 × 0.8 × 0.8 | Murata |
| 22 | GRM21BR60J226M | 0805: 2 × 1.2 × 1.25 | Murata |

(1) See [Third-party Products Disclaimer](#)

9.2.2.5 Setting the Output Voltage

By selecting R_1 and R_2 , the output voltage is programmed to the desired value. Use Equation 3 to calculate R_1 and R_2 .

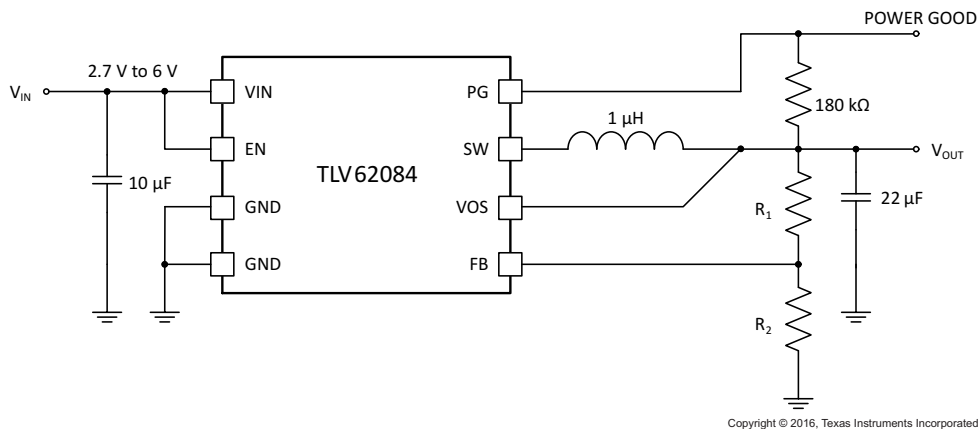


Figure 10. Typical Application Circuit

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

For best accuracy, R_2 must be kept smaller than 40 kΩ to ensure that the current flowing through R_2 is at least 100-times larger than I_{FB} . Changing the sum towards a lower value increases the robustness against noise injection. Changing the sum towards higher values reduces the current consumption.

9.2.3 Application Curves

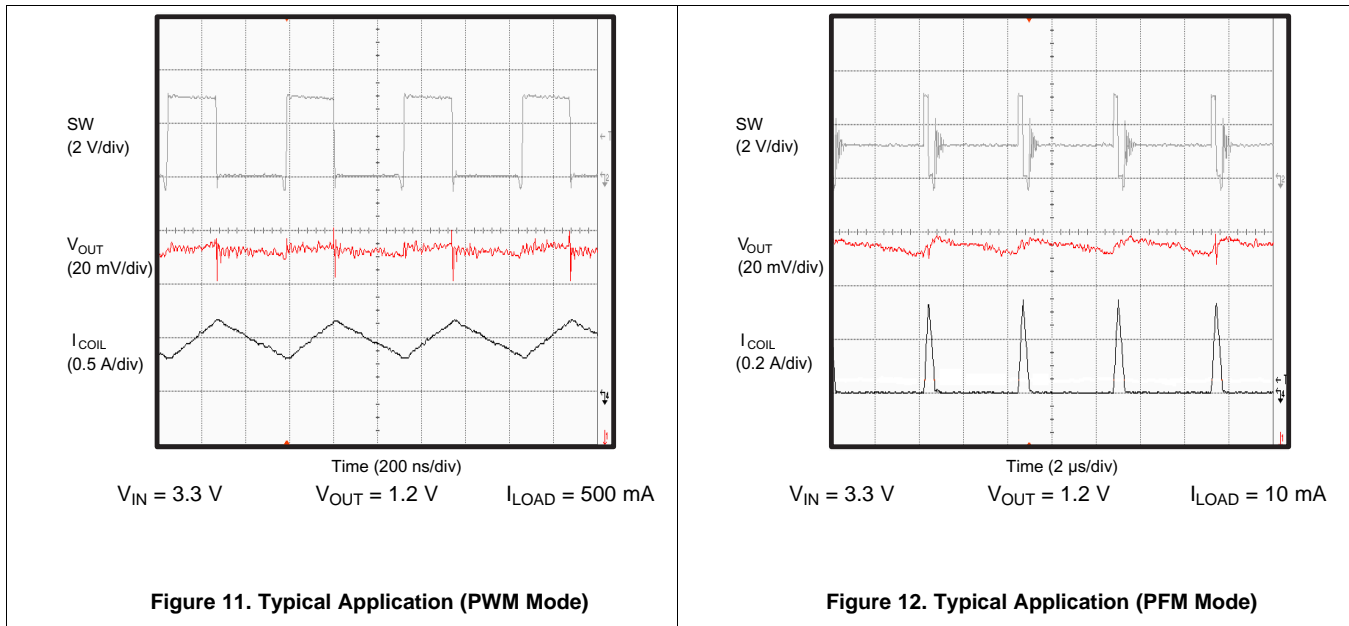
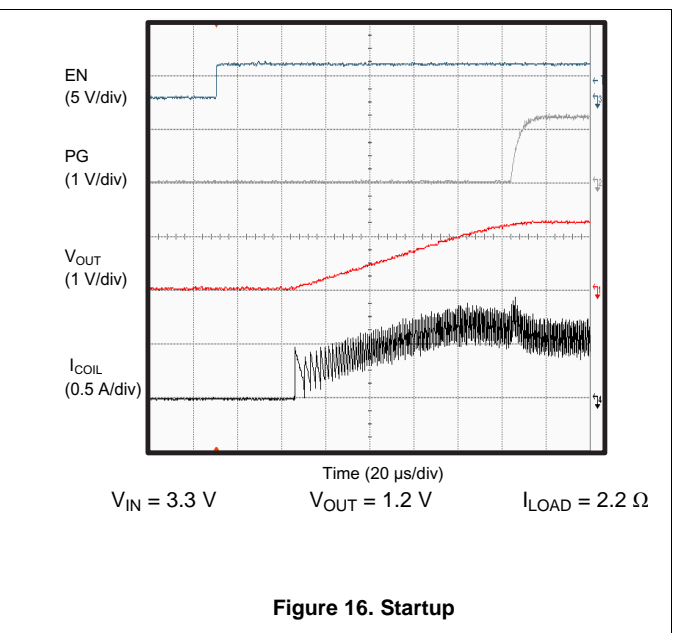
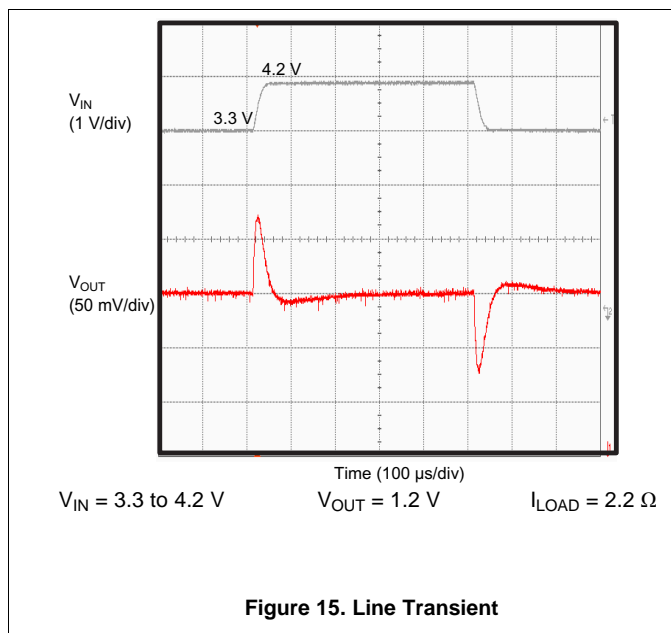
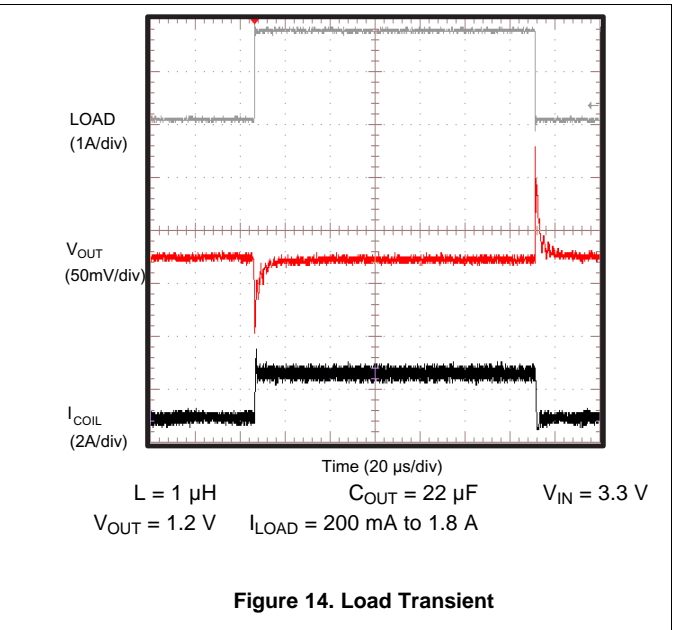
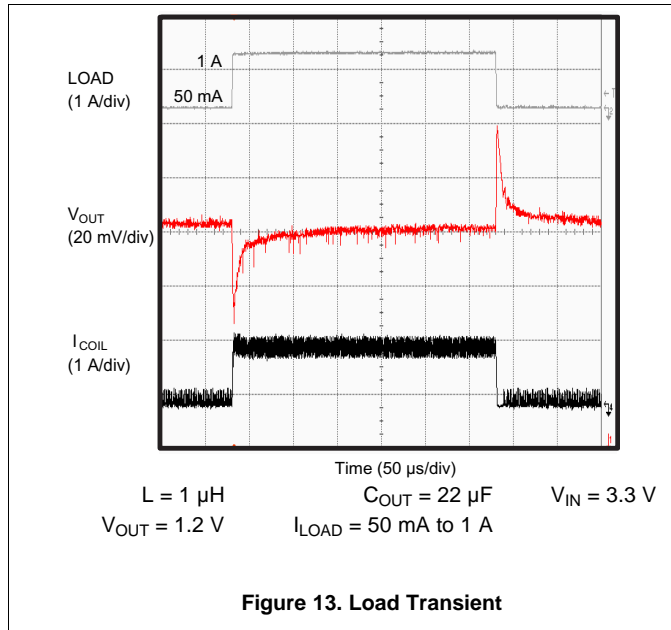
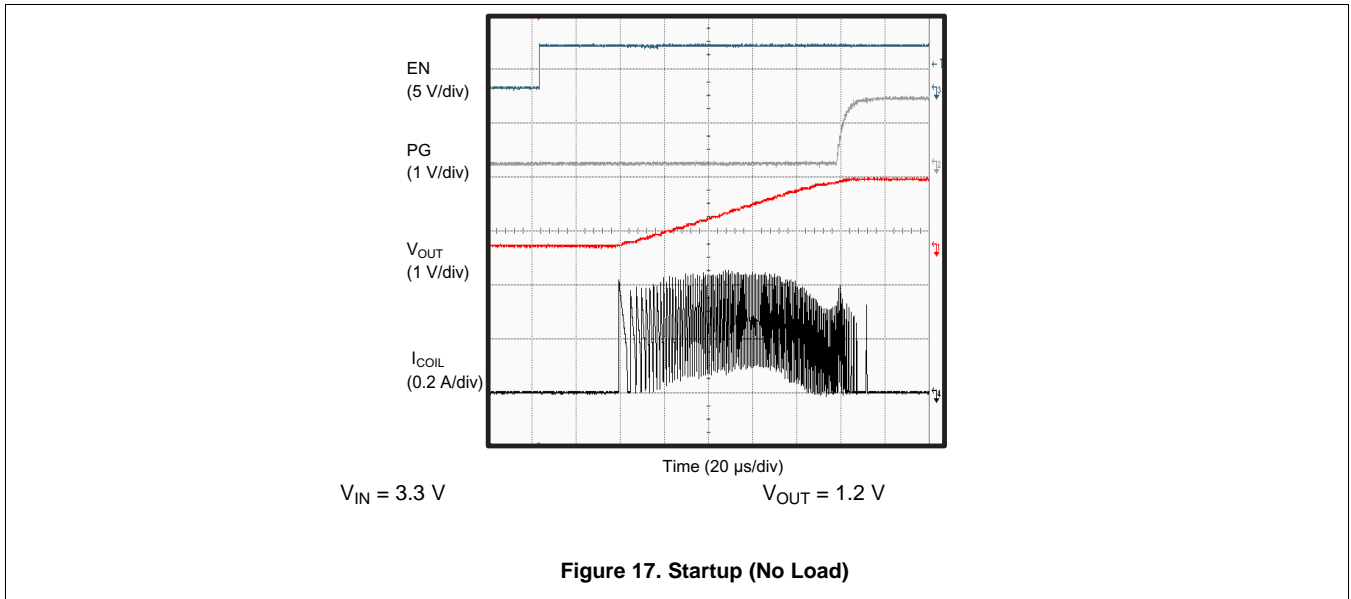


Figure 11. Typical Application (PWM Mode)

Figure 12. Typical Application (PFM Mode)





10 Power Supply Recommendations

The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TLV6208x.

11 Layout

11.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62080 and TLV62084x devices.

- Place input and output capacitors, along with the inductor, as close as possible to the IC which keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance.
- Use a common-power GND.
- Properly connect the low side of the input and output capacitors to the power GND to avoid a GND potential shift.
- The sense traces connected to FB and VOS terminals are signal traces. Keep these traces away from SW nodes.
- Use care to avoid noise induction. By a direct routing, parasitic inductance can be kept small.
- Use GND layers for shielding if needed.

11.2 Layout Example

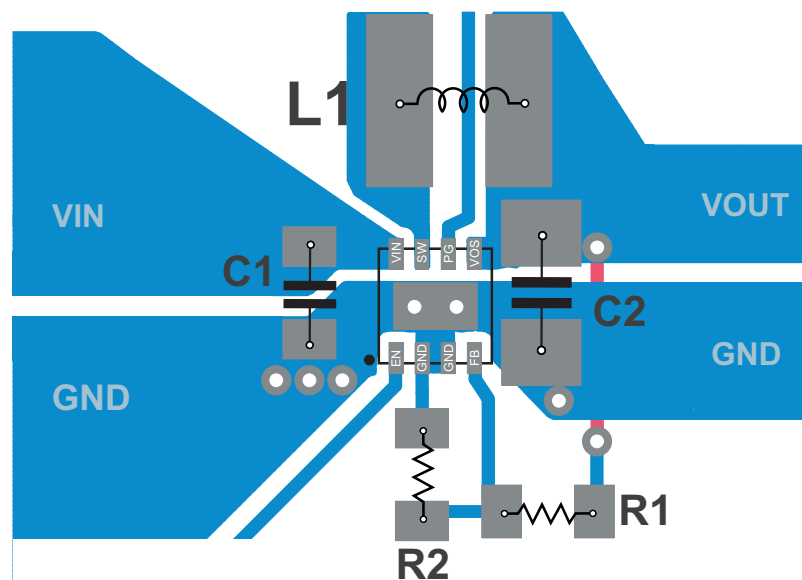


Figure 18. PCB Layout Suggestion

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB by soldering the Thermal Pad.
- Introducing airflow in the system.

For more details on how to use the thermal parameters, see the Thermal Characteristics application notes [SZZA017](#) and [SPRA953](#).

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the TLV62080 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

For related documentation see the following:

- TLV62080EVM-756 User's Guide, *TLV62080, 1.2-A, High-Efficiency, Step-Down Converter in 2-mm x 2-mm SON Package*, [SLVU640](#)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

| PARTS | PRODUCT FOLDER | BUY NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TLV62080 | Click here | Click here | Click here | Click here | Click here |
| TLV62084 | Click here | Click here | Click here | Click here | Click here |
| TLV62084A | Click here | Click here | Click here | Click here | Click here |

12.4 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
 WEBENCH is a registered trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.7 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV62080DSGR | ACTIVE | WSO | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAU | Samples |
| TLV62080DSGT | ACTIVE | WSO | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAU | Samples |
| TLV62084ADSGR | ACTIVE | WSO | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14M | Samples |
| TLV62084ADSGT | ACTIVE | WSO | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14M | Samples |
| TLV62084DSGR | ACTIVE | WSO | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SLO | Samples |
| TLV62084DSGT | ACTIVE | WSO | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SLO | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV62080DSGR | WSON | DSG | 8 | 3000 | 178.0 | 8.4 | 2.25 | 2.25 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV62080DSGT | WSON | DSG | 8 | 250 | 178.0 | 8.4 | 2.25 | 2.25 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV62084ADSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV62084ADSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV62084DSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV62084DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV62080DSGR | WSON | DSG | 8 | 3000 | 205.0 | 200.0 | 33.0 |
| TLV62080DSGT | WSON | DSG | 8 | 250 | 205.0 | 200.0 | 33.0 |
| TLV62084ADSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62084ADSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62084DSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62084DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

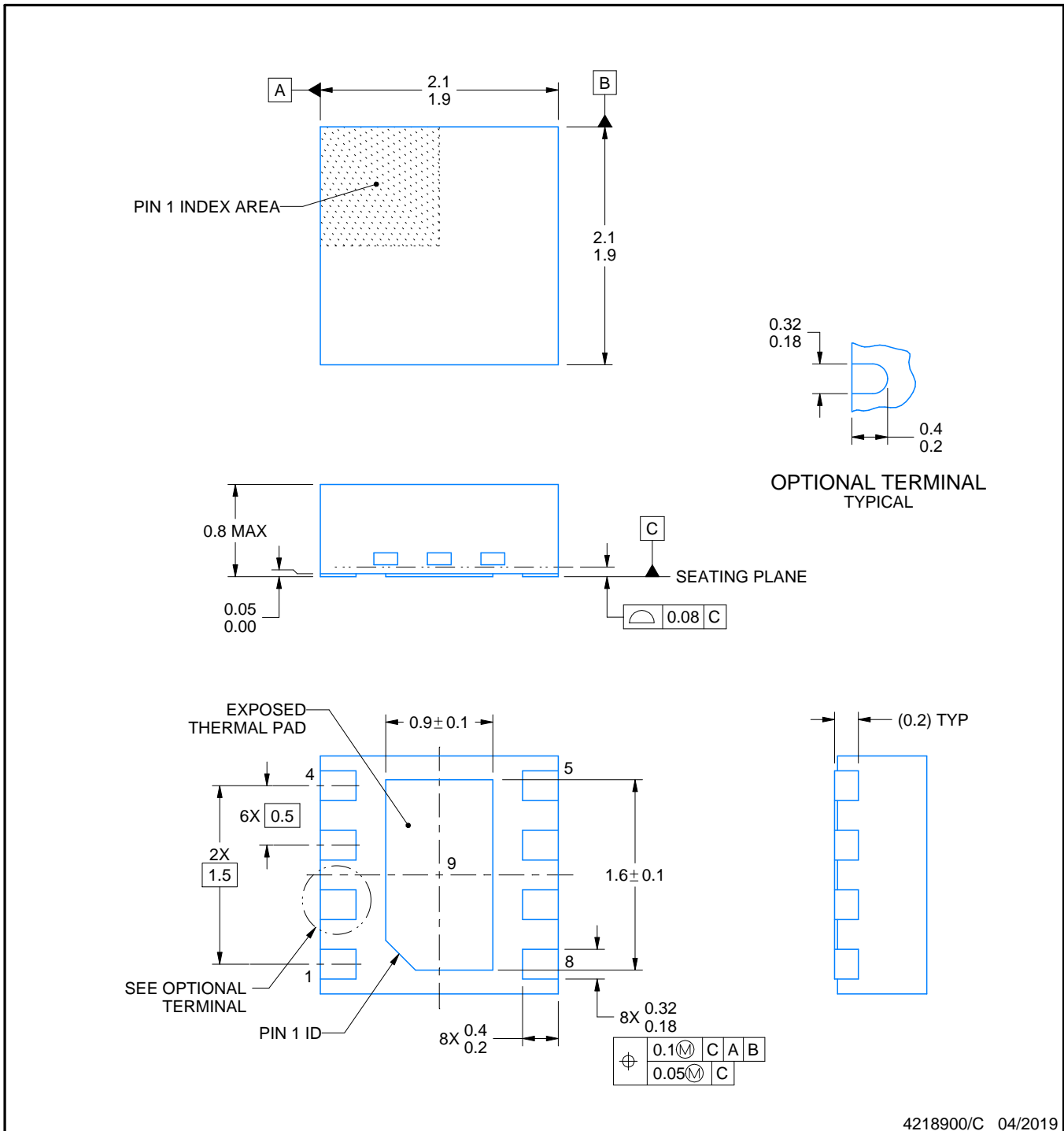
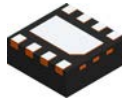
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



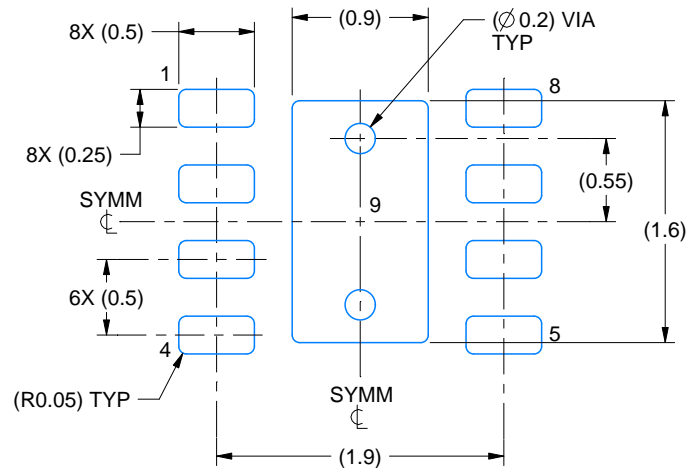
4218900/C 04/2019

EXAMPLE BOARD LAYOUT

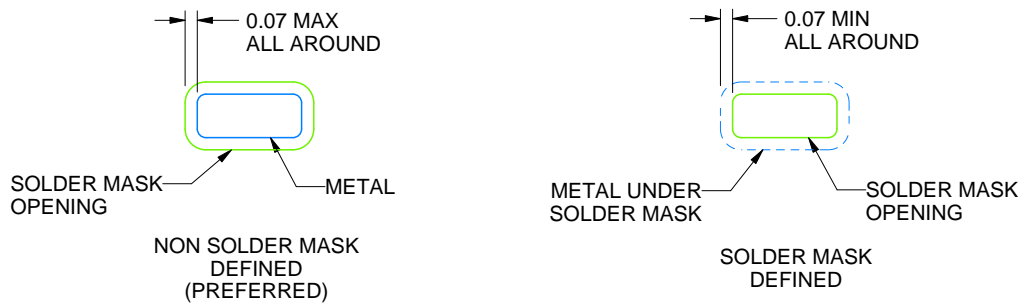
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

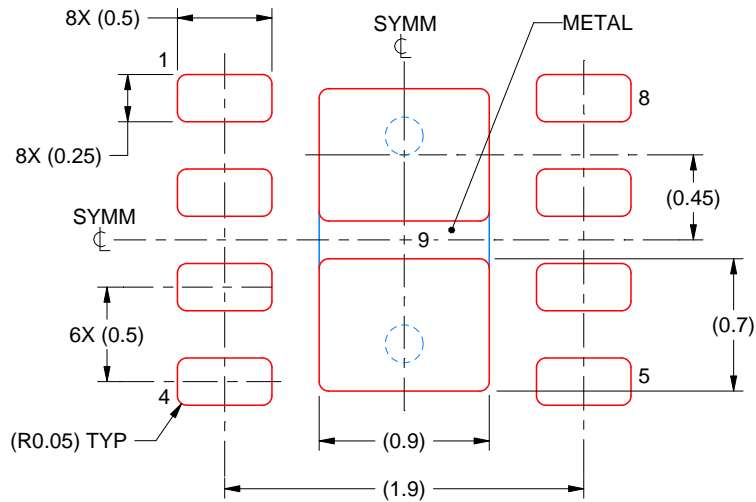
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated