

4.7 DC Operating Conditions

4.7.1 Digital Pins

Table 149: Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins ¹	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0			V
			VDDO = 2.5V	1.75			V
			VDDO = 1.8V	1.26		VDDO+0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V			0.8	V
			VDDO = 2.5V			0.75	V
			VDDO = 1.8V (88E1518/ 88E1512/ 88E1514)	-0.3		0.54	V
VOH	High level output voltage	All digital outputs		VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs				0.4	V
I _{ILK}	Input leakage current					10	uA
C _{IN}	Input capacitance	All pins				5	pF

1. VDDO supplies the CLK125, MDC, MDIO, RESETn, LED[2:0], CONFIG, TX_CLK, TX_CTRL, TXD[3:0], RX_CLK, RX_CTRL, and RXD[3:0].

4.7.2 IEEE DC Transceiver Parameters

Table 150: IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

-10BASE-T IEEE 802.3 Clause 14

-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V _{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585 ¹			mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T ²	0.67	0.75	0.82	V
	Overshoot ²	MDIP/N[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V _{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585 ³			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460 ⁴		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360 ⁵		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska[®] Quad will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.8 AC Electrical Specifications

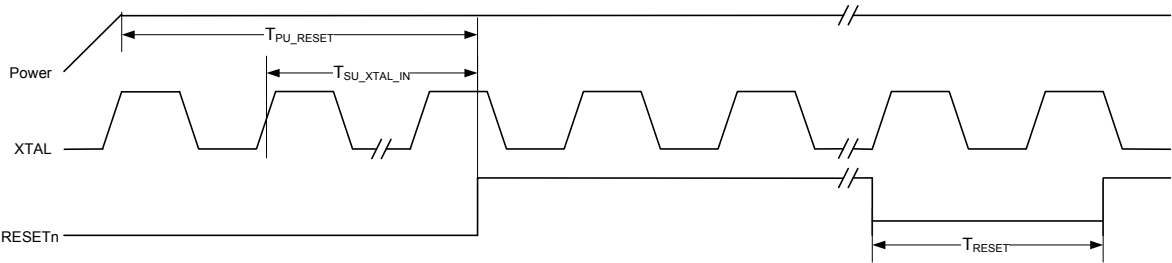
4.8.1 Reset Timing

Table 151: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted	10			ms
$T_{SU_XTAL_IN}$	Number of valid XTAL_IN cycles prior to RESETn de-asserted	10			clks
T_{RESET}	Minimum reset pulse width during normal operation	10			ms

Figure 24: Reset Timing



4.8.2 XTAL_IN/XTAL_OUT Timing¹

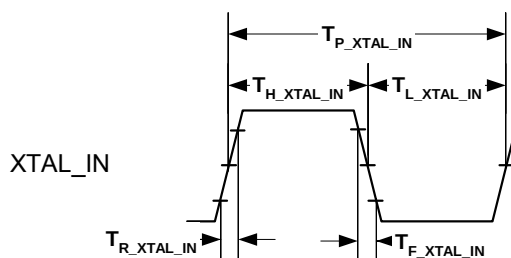
Table 152: XTAL_IN/XTAL_OUT Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P_XTAL_IN}$	XTAL_IN Period		40-50 ppm	40	40+50 ppm	ns
$T_{H_XTAL_IN}$	XTAL_IN High time		13	20	27	ns
$T_{L_XTAL_IN}$	XTAL_IN Low time		13	20	27	ns
$T_{R_XTAL_IN}$	XTAL_IN Rise	10% to 90%	-	3.0	-	ns
$T_{F_XTAL_IN}$	XTAL_IN Fall	90% to 10%	-	3.0	-	ns
$T_{J_XTAL_IN}$	XTAL_IN total jitter ¹		-	-	200	ps ²
XTAL_ESR	Crystal ESR ³		-	30	50	W

1. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
2. 12 kHz to 20 MHz rms jitter on XTAL_IN = 4 ps.
3. See "How to use Crystals as Clock Sources" application note for details.

Figure 25: XTAL_IN/XTAL_OUT Timing



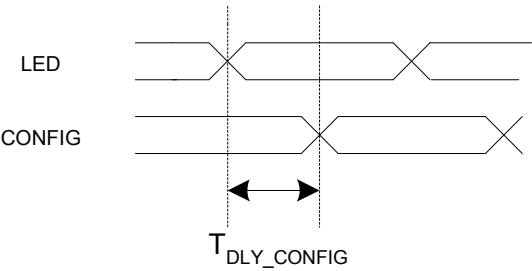
1. If the crystal option is used, ensure that the frequency is 25 MHz $\pm$ 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.

4.8.3 LED to CONFIG Timing

Table 153: LED to CONFIG Timing

Symbol	Parameter	Min	Typ	Max	Units
T _{DLY_CONFIG}	LED to CONFIG Delay	0		25	ns

Figure 27: LED to CONFIG Timing



4.9 SGMII Timing

4.9.1 SGMII Output AC Characteristics

Table 154: SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
T_{SKEW1}^1	Skew between two members of a differential pair			20	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.

4.9.2 SGMII Input AC Characteristics

Table 155: SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

4.10 RGMII Timing

4.10.1 RGMII AC Characteristics

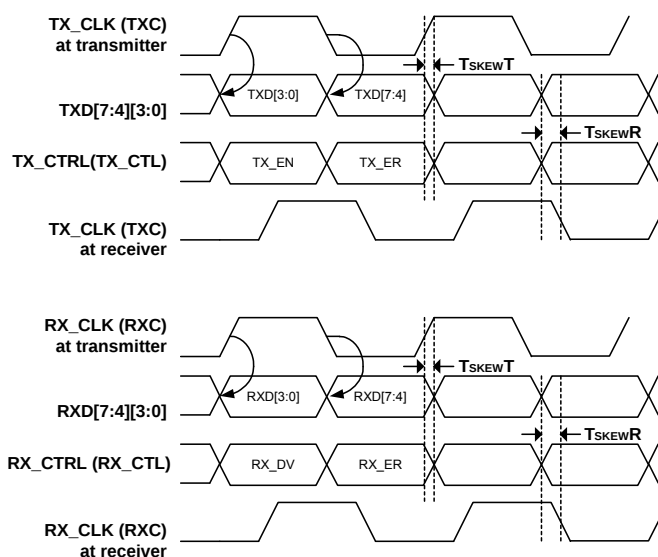
Table 156: RGMII AC Characteristics

(This table is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in [Section 4.10.2, RGMII Delay Timing for Different RGMII Modes, on page 136](#)).

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.8	ns
T _{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
T _{CYCLE_HIGH1000}	High Time for 1000BASE-T ¹	3.6	4.0	4.4	ns
T _{CYCLE_HIGH100}	High Time for 100BASE-T ¹	16	20	24	ns
T _{CYCLE_HIGH10}	High Time for 10BASE-T ¹	160	200	240	ns
T _{RISE} /T _{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{CYCLE} of the lowest speed transitioned between.

Figure 29: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in [Section 4.10.2, RGMII Delay Timing for Different RGMII Modes, on page 136](#)

4.10.2 RGMII Delay Timing for Different RGMII Modes

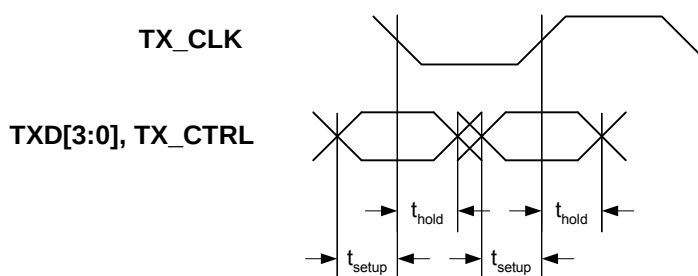
4.10.2.1 PHY Input - TX_CLK Delay when Register 21_2.4 = 0

Table 157: PHY Input - TX_CLK Delay when Register 21_2.4 = 0

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.4 = 0	1.0			ns
t_{hold}		0.8			ns

Figure 30: TX_CLK Delay Timing - Register 21_2.4 = 0



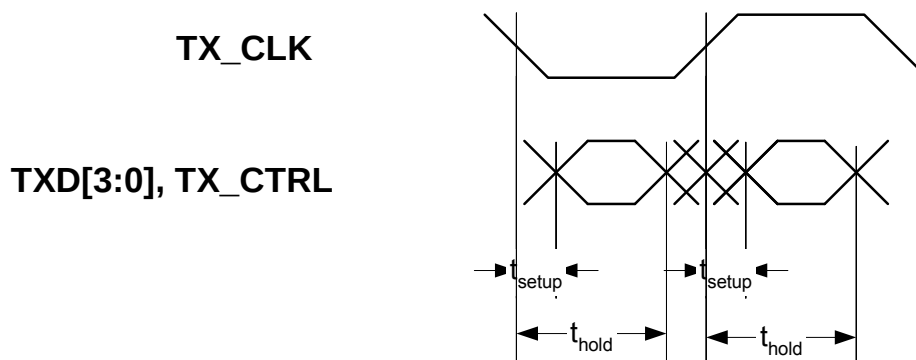
4.10.2.2 PHY Input - TX_CLK Delay when Register 21_2.4 = 1

Table 158: PHY Input - TX_CLK Delay when Register 21_2.4 = 1

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.4 = 1 (add delay)	-0.9			ns
t_{hold}		2.7			ns

Figure 31: TX_CLK Delay Timing - Register 21_2.4 = 1 (add delay)



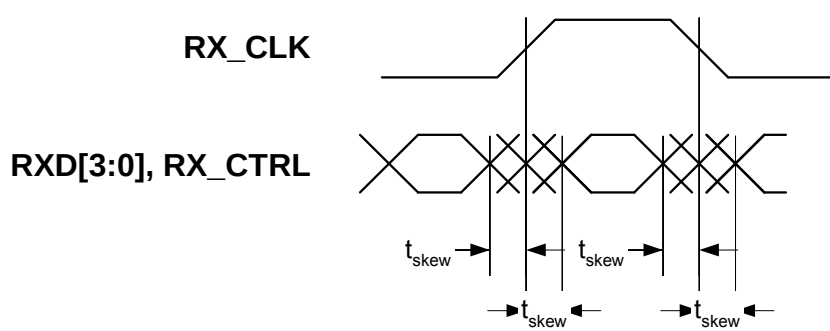
4.10.2.3 PHY Output - RX_CLK Delay

Table 159: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{skew}	Register 21_2.5 = 0	- 0.5		0.5	ns

Figure 32: RGMII RX_CLK Delay Timing - Register 21_2.5 = 0



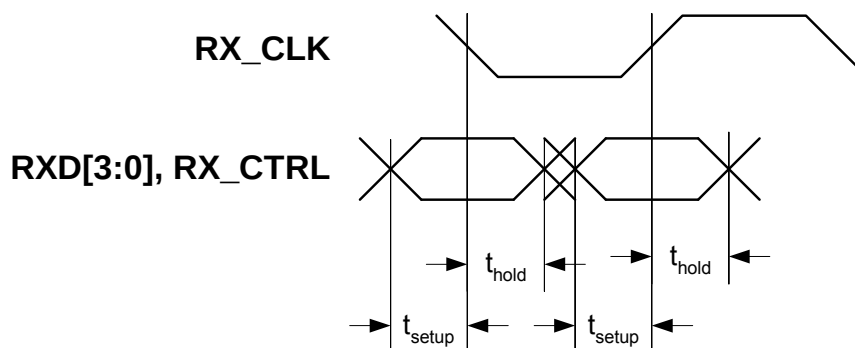
4.10.2.4 PHY Output - RX_CLK Delay

Table 160: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.5 = 1 (add delay)	1.2			ns
t_{hold}		1.2			ns

Figure 33: RGMII RX_CLK Delay Timing - Register 21_2.5 = 1 (add delay)



4.11 MDC/MDIO Timing

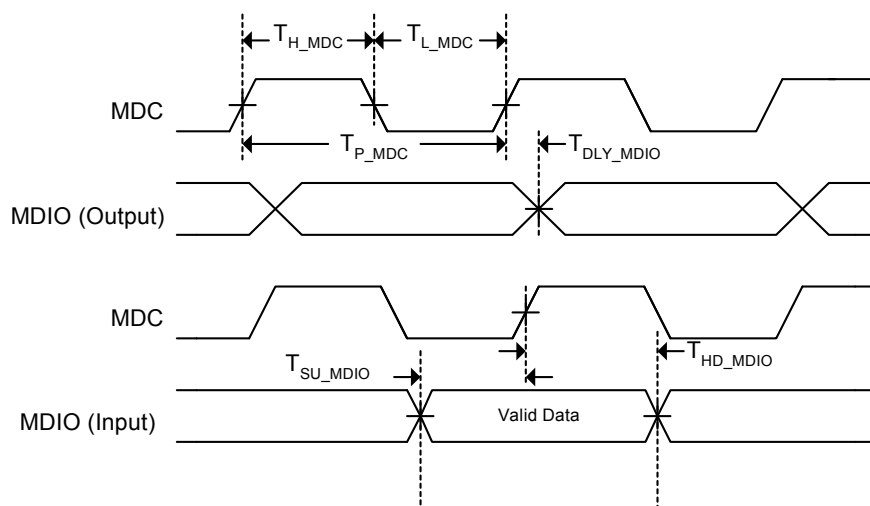
Table 161: MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	10			ns
T_{P_MDC}	MDC Period	83.3			ns ¹
T_{H_MDC}	MDC High	30			ns
T_{L_MDC}	MDC Low	30			ns

1. Maximum frequency = 12 MHz.

Figure 34: MDC/MDIO Timing



4.12 IEEE AC Transceiver Parameters

Table 162: IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

-10BASE-T IEEE 802.3 Clause 14-2000

-100BASE-TX ANSI X3.263-1995

-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T _{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T _{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T _{RISE} /T _{FALL} Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5 ¹	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

4.13 Latency Timing

4.13.1 RGMII to 1000BASE-T Transmit Latency Timing

Table 163: RGMII to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

Symbol	Parameter	Min	Typ	Max	Units
T _{AS_TXC_MDI_1000}	1000BASE-T TX_CTRL Asserted to MDI SSD1	141		153	ns

4.13.2 RGMII to 100BASE-TX Transmit Latency Timing

Table 164: RGMII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

Symbol	Parameter	Min	Typ	Max	Units
T _{AS_TXC_MDI_100}	100BASE-TX TX_CTRL Asserted to /J/	634		679	ns

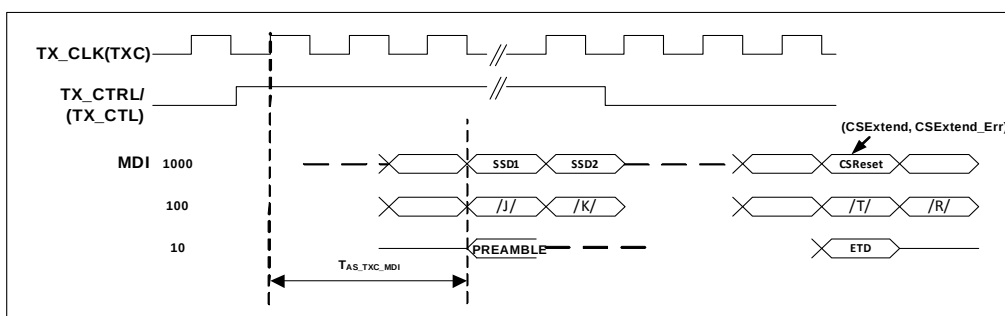
4.13.3 RGMII to 10BASE-T Transmit Latency Timing

Table 165: RGMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

Symbol	Parameter	Min	Typ	Max	Units
T _{AS_TXC_MDI_10}	10BASE-T TX_CTRL Asserted to Preamble	5.874		6.258	μs

Figure 36: RGMII/MII to 10/100/1000BASE-T Transmit Latency Timing



4.13.4 1000BASE-T to RGMII Receive Latency Timing

Table 166: 1000BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
$T_{AS_MDI_RXC_1000}$	1000BASE-T MDI start of Packet to RX_CTRL Asserted	227		235	ns

4.13.5 100BASE-TX to RGMII Receive Latency Timing

Table 167: 100BASE-TX to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
$T_{AS_MDI_RXC_100}$	100BASE-TX MDI start of Packet to RX_CTRL Asserted	362		362	ns

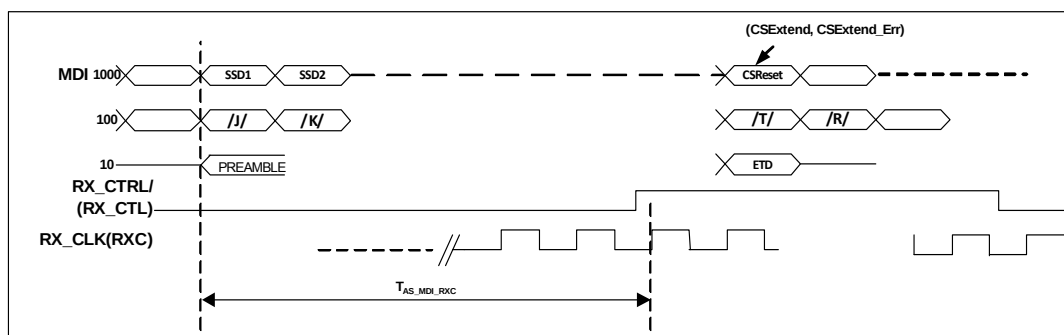
4.13.6 10BASE-T to RGMII Receive Latency Timing

Table 168: 10BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
$T_{AS_MDI_RXC_10}$	10BASE-T MDI start of Packet to RX_CTRL Asserted	2.082		2.178	μ s

Figure 37: 10/100/1000BASE-T to RGMII Receive Latency Timing



4.13.7 10/100/1000BASE-T to SGMII Latency Timing

Table 169: 10/100/1000BASE-T to SGMII Latency Timing

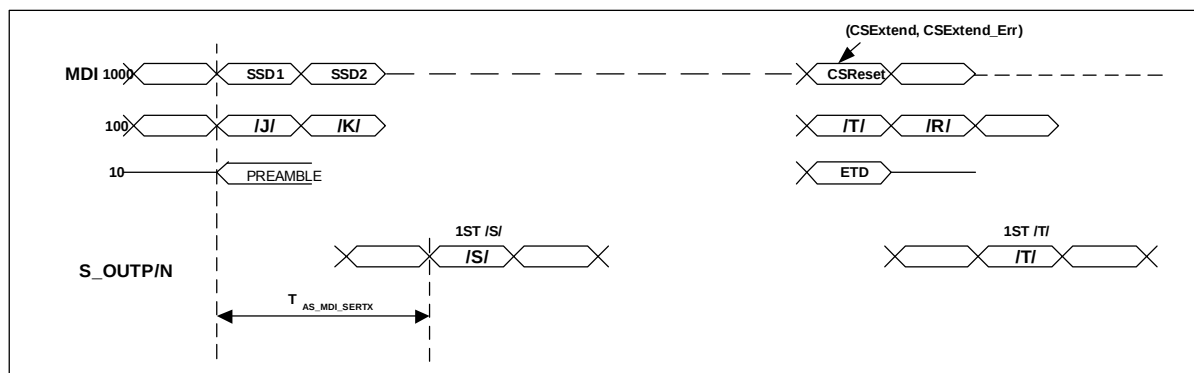
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
$T_{AS_MDI_SERTX_1000}^{1,2}$	MDI SSD1 to S_OUTP/N Start of Packet	326		361	ns
$T_{AS_MDI_SERTX_100}^2$	MDI /J/ to S_OUTP/N Start of Packet	776		866	ns
$T_{AS_MDI_SERTX_10}^{2,3}$	MDI Preamble to S_OUTP/N Start of Packet	5.702		6.103	us

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.

- Assumes Register 16_1.15:14 is set to 01, which is the default.
- Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 38: 10/100/1000BASE-T to SGMII Latency Timing



4.13.8 SGMII to 10/100/1000BASE-T Latency Timing

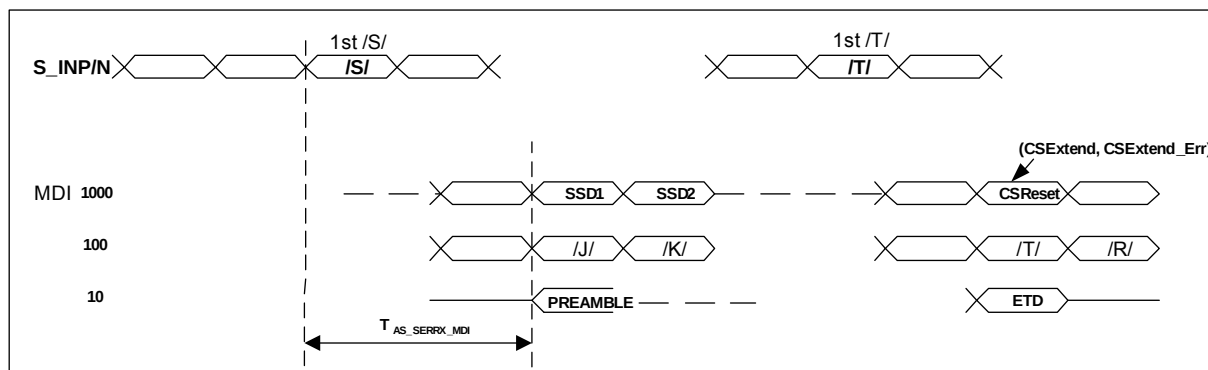
Table 170: SGMII to 10/100/1000BASE-T Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
$T_{AS_SERRX_MDI_1000}^1$	S_INP/N Start of Packet /S/ to MDI SSD1	206		232	ns
$T_{AS_SERRX_MDI_100}^1$	S_INP/N Start of Packet /S/ to MDI /J/	626		706	ns
$T_{AS_SERRX_MDI_10}^1$	S_INP/N Start of Packet /S/ to MDI Preamble	4.991		5.779	us

- Assumes register 16_2.15:14 is set to 01, which is the default.

Figure 39: SGMII to 10/100/1000BASE-T Latency Timing



5

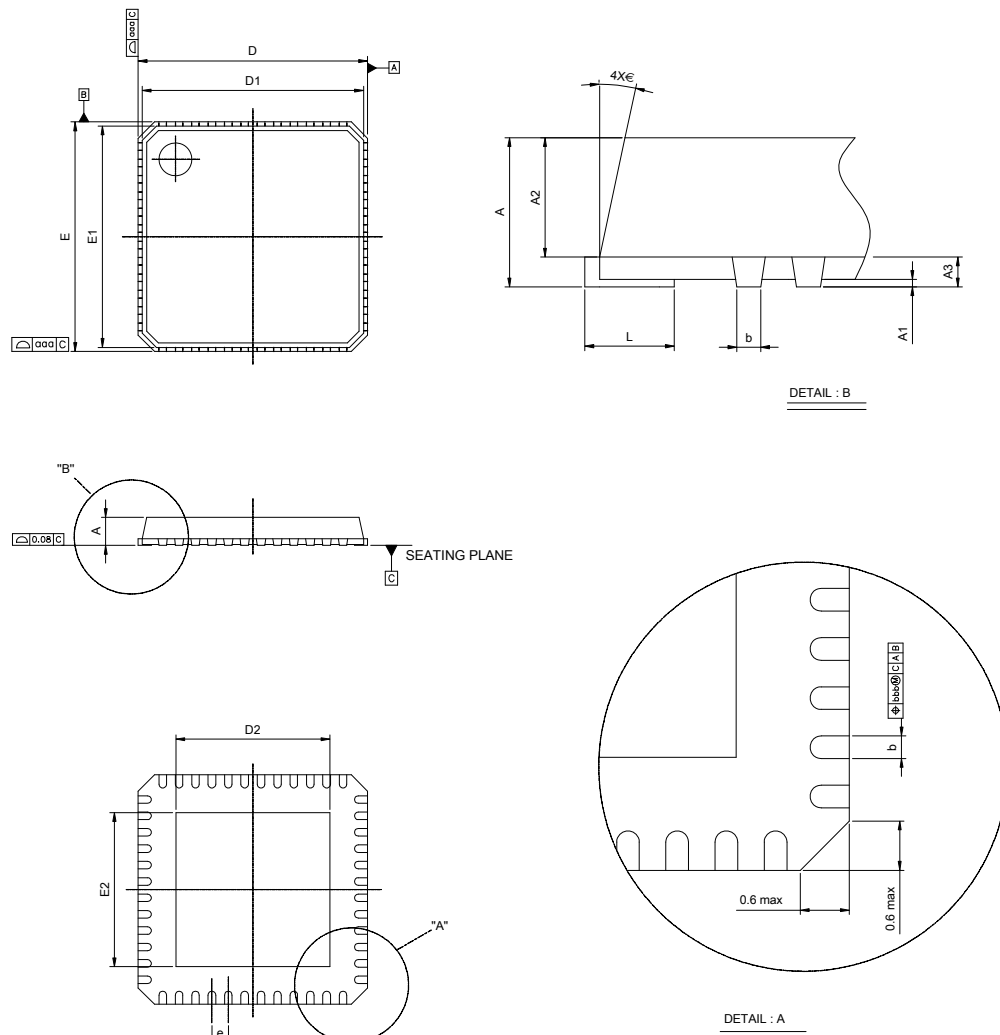
Package Mechanical Dimensions

This section includes information on the following topics:

- [Section 5.1, 48-Pin QFN Package](#)
- [Section 5.2, 56-Pin QFN Package](#)

5.1 48-Pin QFN Package

Figure 40: 88E1510/88E1518 48-pin QFN Package Mechanical Drawings



NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

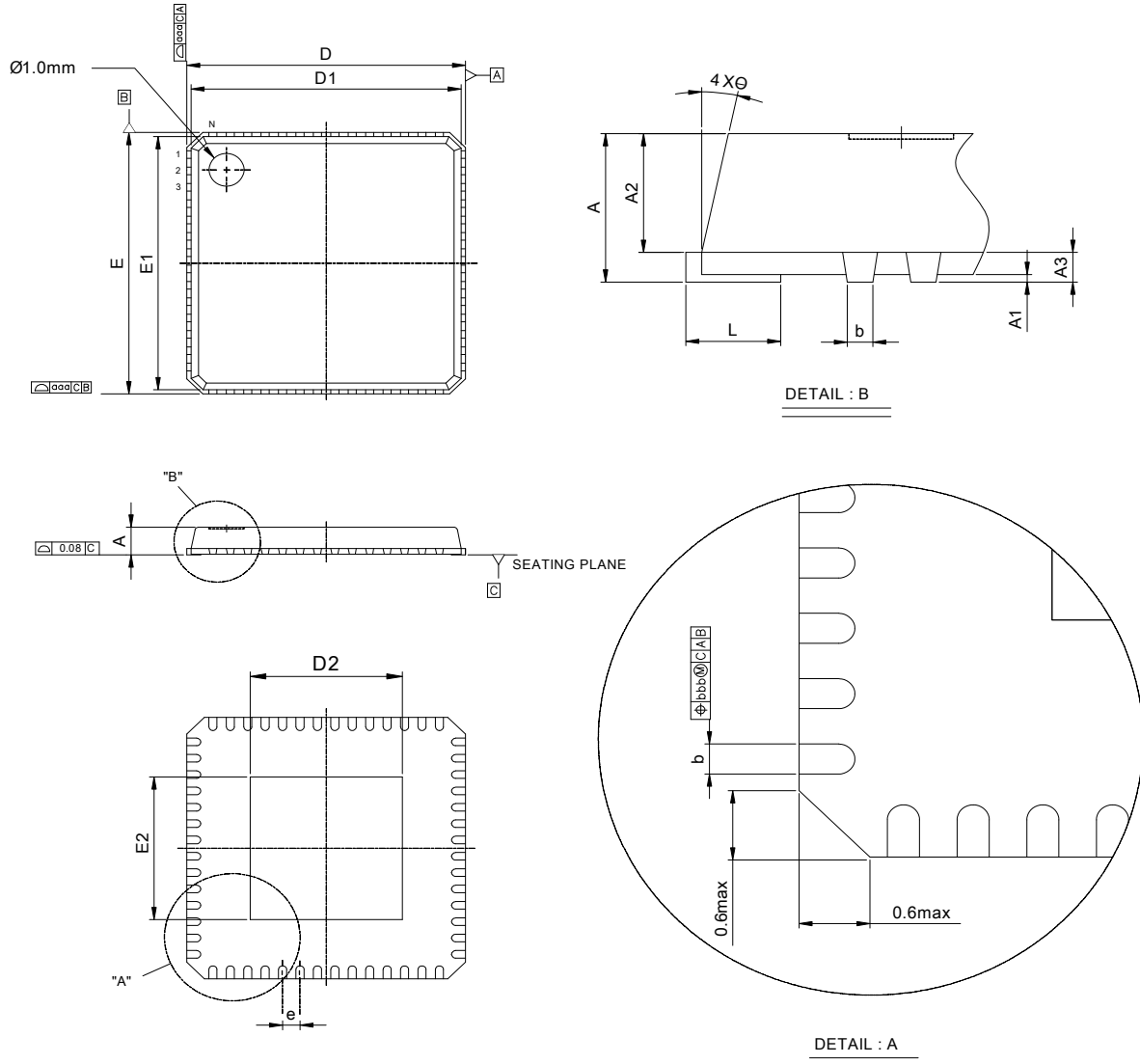
Table 171: 48-Pin QFN Mechanical Dimensions

Symbol	Dimensions in mm		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3	0.20 REF		
b	0.18	0.23	0.30
D	7.00 BSC		
D1	6.75 BSC		
E	7.00 BSC		
E1	6.75 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.25
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	Dimension in mm
D ₂	3.10
E ₂	3.10

5.2 56-Pin QFN Package

Figure 41: 88E1512/88E1514 56-pin QFN Package Mechanical Drawings



Note

All dimensions in mm.

Table 172: 56-Pin QFN Mechanical Dimensions

Symbol	Dimensions in mm		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3	0.20 REF		
b	0.18	0.23	0.30
D	8.00 BSC		
D1	7.75 BSC		
E	8.00 BSC		
E1	7.75 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.15
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	Dimension in mm
D ₂	4.37
E ₂	4.37

6 Part Order Numbering/Package Marking

This section includes information on the following topics:

- [Section 6.1, Part Order Numbering](#)
- [Section 6.2, Package Marking](#)

6.1 Part Order Numbering

[Figure 42](#) shows the part order numbering scheme for the 88E1510/88E1518/88E1512/88E1514. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 42: Sample Part Number

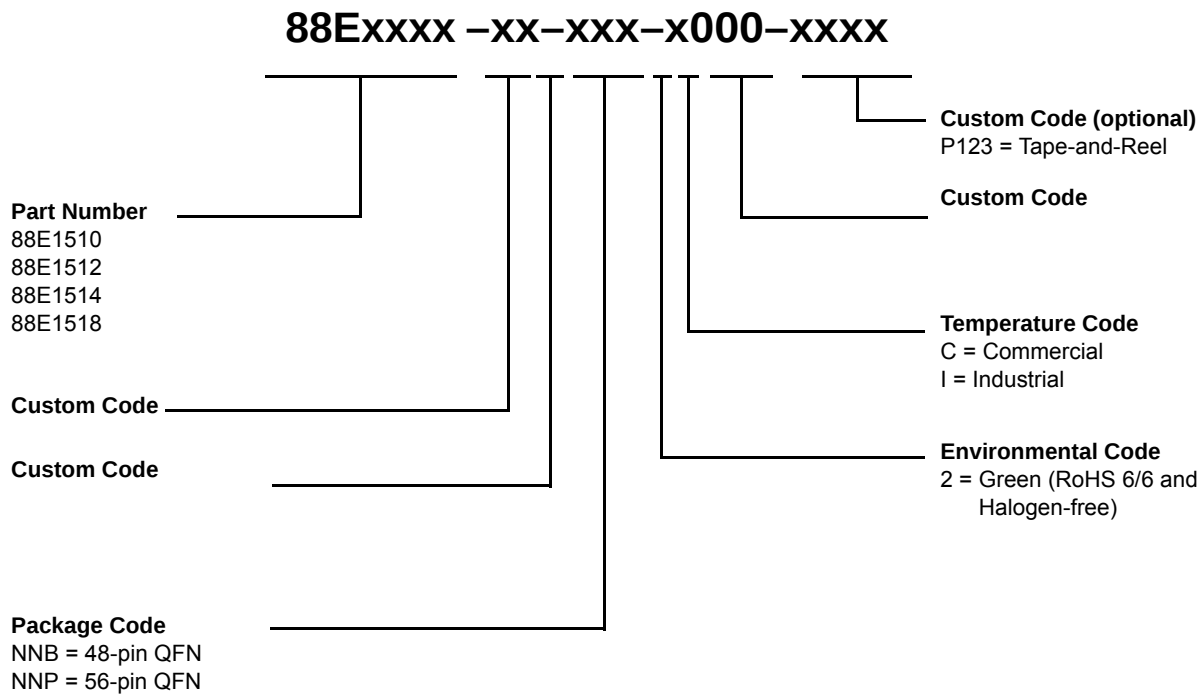


Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options

Package Type	Part Order Number
Commercial	
88E1510 48-pin QFN	88E1510-xx-NNB2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1510 48-pin QFN Tape-and-Reel	88E1510-xx-NNB2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1518 48-pin QFN	88E1518-xx-NNB2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)

Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options (Continued)

Package Type	Part Order Number
88E1518 48-pin QFN Tape-and-Reel	88E1518-xx-NNB2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1512 56-pin QFN	88E1512-xx-NNP2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1514 56-pin QFN	88E1514-xx-NNP2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1514 56-pin QFN Tape-and-Reel	88E1514-xx-NNP2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package)
Industrial	
88E1510 48-pin QFN	88E1510-xx-NNB2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package)
88E1512 56-pin QFN	88E1512-xx-NNP2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package)
88E1512 56-pin QFN Tape-and-Reel	88E1512-xx-NNP2I000-P123 (Industrial, Green, RoHS 6/6 and Halogen-free package)

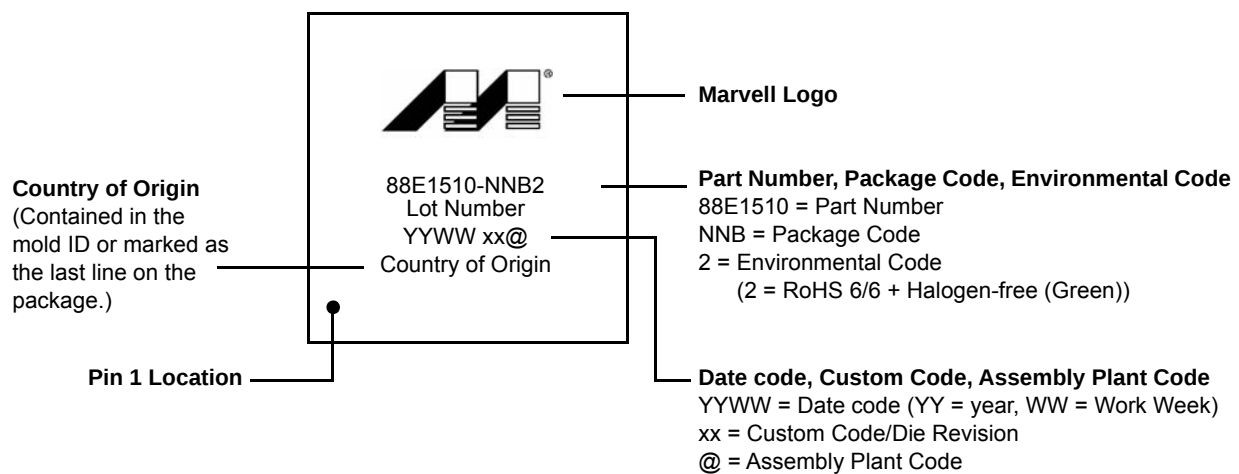
6.2 Package Marking

6.2.1 Commercial

The following figures show sample Commercial package markings and pin 1 location for the 88E1510/88E1518/88E1512/88E1514:

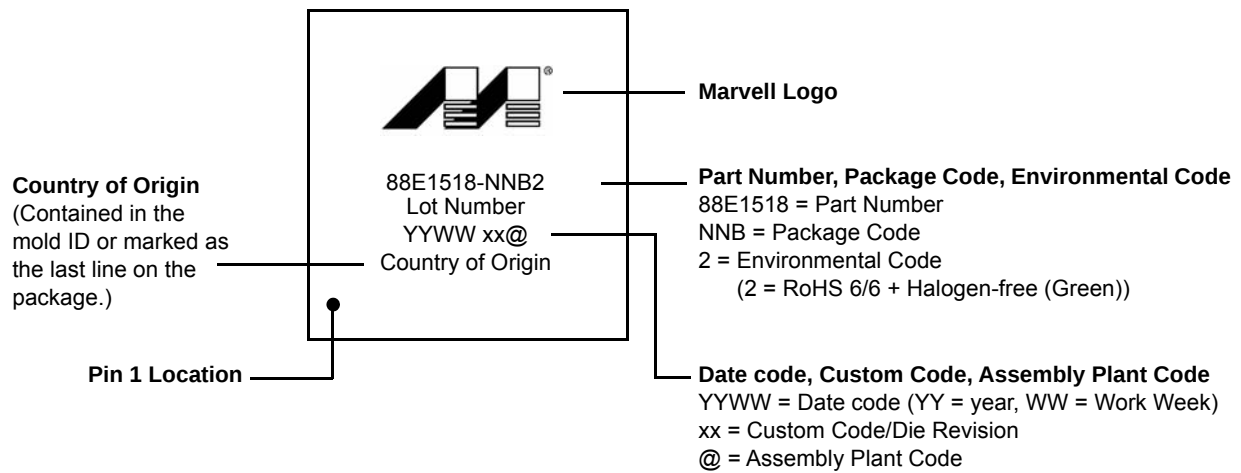
- [Figure 43](#) for 88E1510 48-pin QFN
- [Figure 44](#) for 88E1518 48-pin QFN
- [Figure 45](#) for 88E1512 56-pin QFN
- [Figure 46](#) for 88E1514 56-pin QFN

Figure 43: 88E1510 48-pin QFN Commercial Package Marking and Pin 1 Location



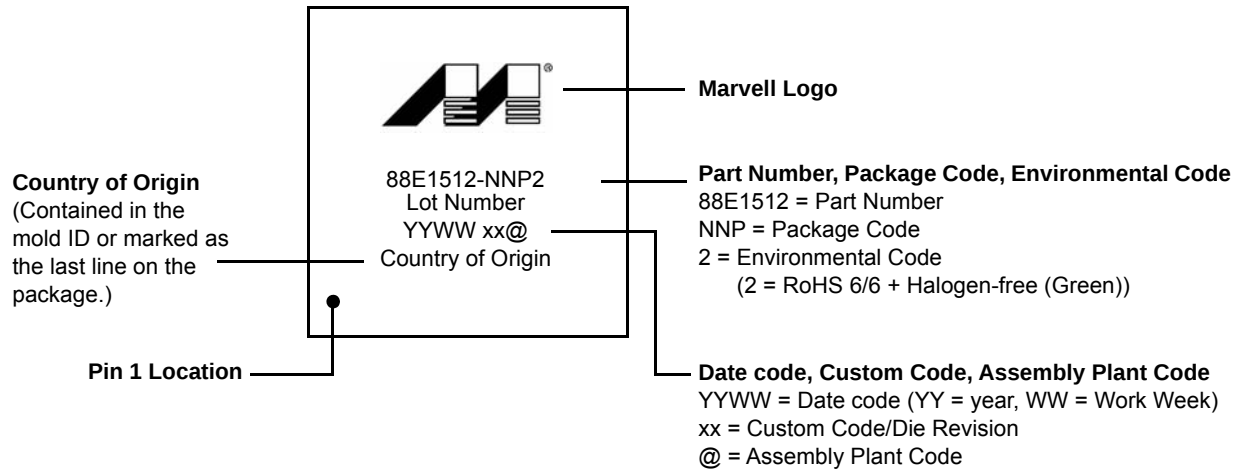
Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 44: 88E1518 48-pin QFN Commercial Package Marking and Pin 1 Location



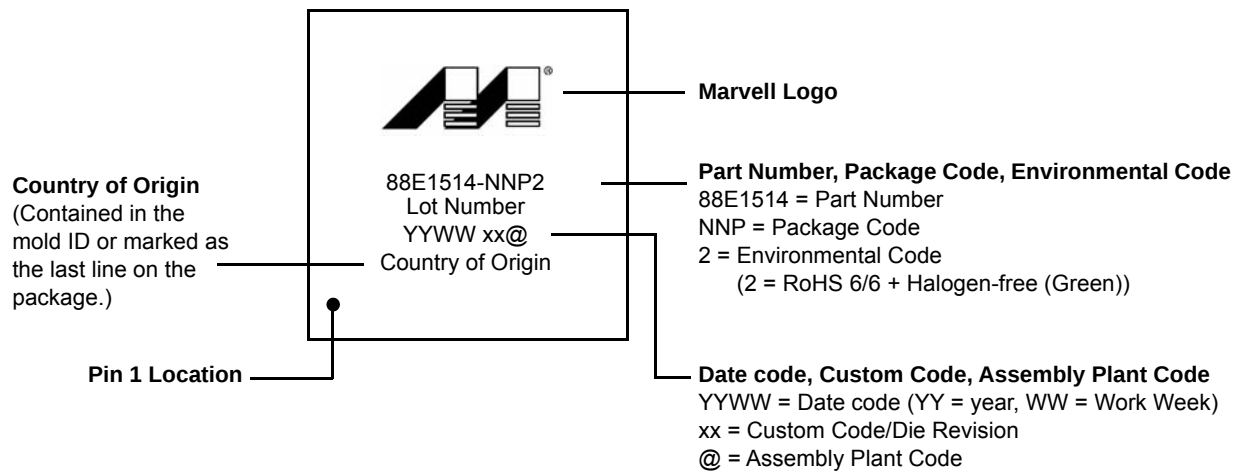
Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 45: 88E1512 56-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 46: 88E1514 56-pin QFN Commercial Package Marking and Pin 1 Location



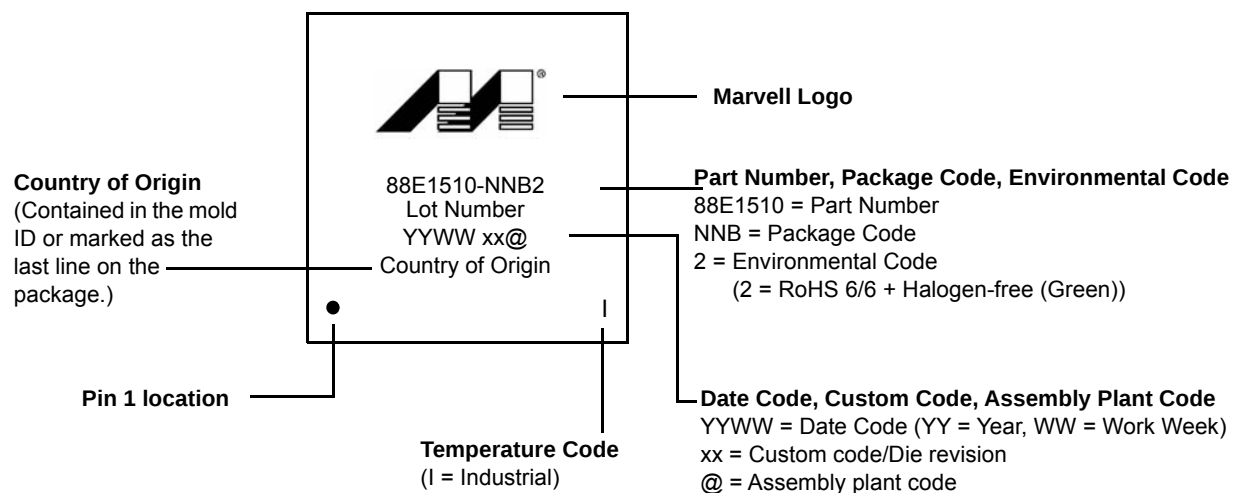
Note: The above drawing is not drawn to scale. Location of markings is approximate.

6.2.2 Industrial

The following figures show sample Industrial package markings and pin 1 location for the 88E1510/88E1518/88E1512/88E1514:

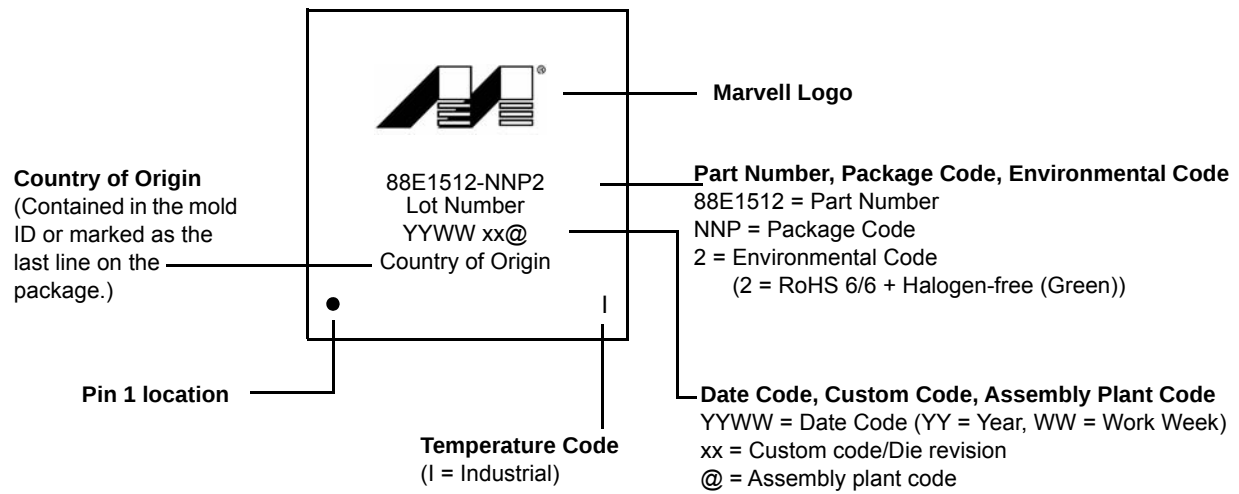
- [Figure 47](#) for 88E1510 48-pin QFN
- [Figure 48](#) for 88E1512 56-pin QFN

Figure 47: 88E1510 48-pin QFN Industrial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 48: 88E1512 56-pin QFN Industrial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A

Revision History

Table 174: Revision History

Revision	Date	Section	Detail
Rev. B	February 23, 2018	All applicable	Cosmetic enhancements
		Part Order Numbering/Package Marking	Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options: added part number for 88E1512 56-pin QFN Tape-and-Reel
Rev. A	January 4, 2018	—	Initial release



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