Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

Features

- Injection Current Cross–Coupling Less than 1 mV/mA (See Figure 10)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range $(V_{CC} GND) = 2.0 \text{ to } 6.0 \text{ V}$
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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www.onsemi.com





SOIC-16 D SUFFIX CASE 751B

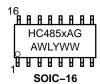


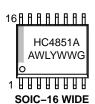


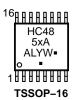


TSSOP-16 DT SUFFIX CASE 948F QFN16 MN SUFFIX CASE 485AW

MARKING DIAGRAMS









QFN16*
*V4851 marking used for NLV74HC4851AMN1TWG

x = 1 or 2

A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

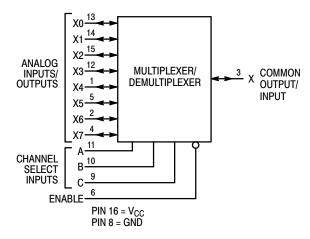


Figure 1. MC74HC4851A Logic Diagram Single-Pole, 8-Position Plus Common Off

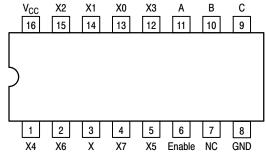


Figure 2. MC74HC4851A 16-Lead Pinout (Top View)

FUNCTION TABLE - MC74HC4851A

Control Inputs				
	Select			
Enable	С	В	Α	ON Channels
L	L	L	L	X0
L	L	L	Н	X1
L	L	Н	L	X2
L	L	Н	Н	X3
L	Н	L	L	X4
L	Н	L	Н	X5
L	Н	Н	L	X6
L	Н	Н	Н	X7
Н	X	Χ	Χ	NONE

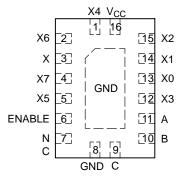


Figure 3. MC74HC4851A QFN Pinout

FUNCTION TABLE - MC74HC4852A

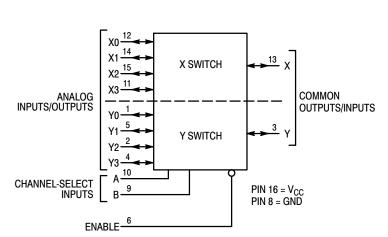
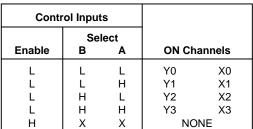


Figure 4. MC74HC4852A Logic Diagram Double-Pole, 4-Position Plus Common Off



X = Don't Care

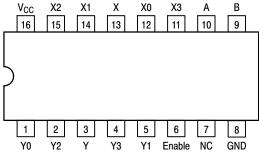


Figure 5. MC74HC4852A 16-Lead Pinout (Top View)

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Any Pin) (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	±25	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V _{in}	DC Input Voltage (Any Pin)	(Referenced to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch		0.0	1.2	V
T _A	Operating Temperature Range, All Package Types		- 55	+125	°C
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

			v _{cc}	Guarai		anteed Limit	
Symbol	Parameter	Condition	V	-55 to 25°C	≤85°C	≤125°C	Unit
V _{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R _{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V _{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R _{on} = Per Spec	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
l _{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)} = V_{CC}$ or GND $V_{in(analog)} = GND$	6.0	2	20	40	μΑ

^{*}For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Analog Section

				Guaranteed Limit			
Symbol	Parameter	Condition	v _{cc}	-55 to 25°C	≤85°C	≤125°C	Unit
R _{on}	Maximum "ON" Resistance	$V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}}; V_{\text{IS}} = V_{\text{CC}} \text{ to}$ GND (Note 1); $I_{\text{S}} \le 2.0 \text{ mA}$ (Note 2)	2.0 3.0 4.5 6.0	1700 1100 550 400	1750 1200 650 500	1800 1300 750 600	Ω
ΔR_{on}	Delta "ON" Resistance	$V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}}; V_{\text{IS}} = V_{\text{CC}}/2$ (Note 1); $I_{\text{S}} \le 2.0 \text{ mA}$ (Note 2)	2.0 3.0 4.5 6.0	300 160 80 60	400 200 100 80	500 240 120 100	Ω
l _{off}	Maximum Off-Channel Leakage Current, Any One Channel Common Channel	V _{in} = V _{CC} or GND	6.0	±0.1 ±0.1	±0.1 ±0.1	±0.1 ±0.1	μΑ
I _{on}	Maximum On-Channel Leakage Channel-to-Channel	V _{in} = V _{CC} or GND	6.0	±0.1	±0.1	±0.1	μΑ

AC CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V _{CC}	-55 to 25°C	≤85°C	≤125°C	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Analog Input to Analog Output		160 80 40 30	180 90 45 35	200 100 50 40	ns
t _{PHL} , t _{PHZ,PZH} t _{PLH} , t _{PLZ,PZL}	Maximum Propagation Delay, Enable or Channel-Select to Analog Output	2.0 3.0 4.5 6.0	260 160 80 78	280 180 90 80	300 200 100 80	ns
C _{in}	Maximum Input Capacitance Digital Pins (All Switches Off) Any Single Analog Pin (All Switches Off) Common Analog Pin		10 35 40	10 35 40	10 35 40	pF
C _{PD}	Power Dissipation Capacitance Typical	5.0	20			pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V $_{CC}$ = 5V, T_A = -55°C to +125°C)

Symbol	Parameter	Condition	Тур	Max	Unit
VΔ _{out}		$\begin{split} & I_{in}{}^{*} \leq 1 \text{ mA, } R_{S} \leq 3,9 \text{ k}\Omega \\ & I_{in}{}^{*} \leq 10 \text{ mA, } R_{S} \leq 3,9 \text{ k}\Omega \\ & I_{in}{}^{*} \leq 1 \text{ mA, } R_{S} \leq 20 \text{ k}\Omega \\ & I_{in}{}^{*} \leq 10 \text{ mA, } R_{S} \leq 20 \text{ k}\Omega \end{split}$	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV

^{*} I_{in} = Total current injected into all disabled channels.

V_{IS} is the input voltage of an analog I/O pin.
 I_S is the currebnt flowing in or out of analog I/O pin.

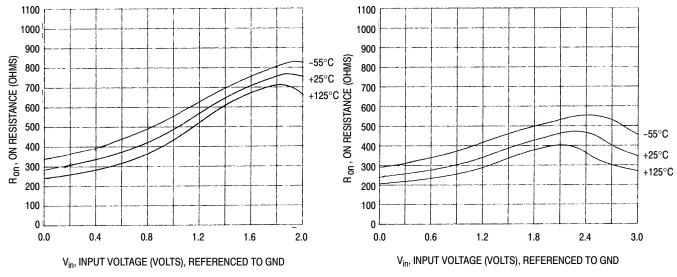


Figure 6. Typical On Resistance V_{CC} = 2V

Figure 7. Typical On Resistance $V_{CC} = 3V$

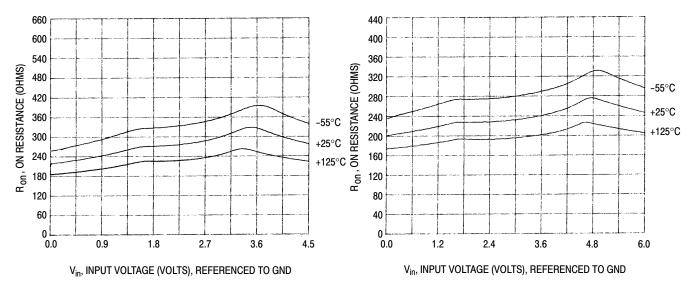


Figure 8. Typical On Resistance $V_{CC} = 4.5V$

Figure 9. Typical On Resistance $V_{CC} = 6V$

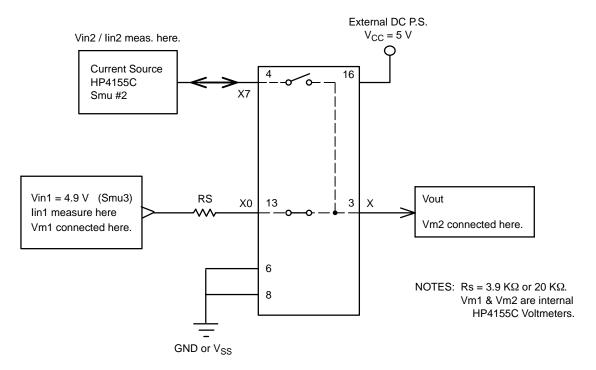


Figure 10. Injection Current Coupling Specification

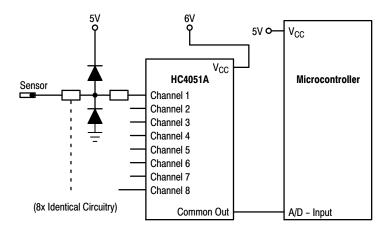


Figure 11. Actual Technology

Requires 32 passive components and one extra 6V regulator to suppress injection current into a standard HC4051 multiplexer

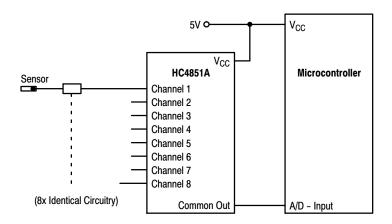


Figure 12. MC74HC4851A Solution Solution by applying the HC4851A multiplexer

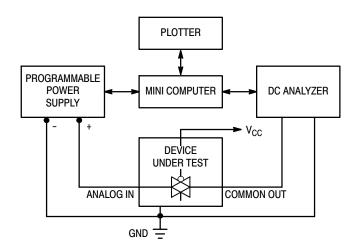


Figure 13. On Resistance Test Set-Up

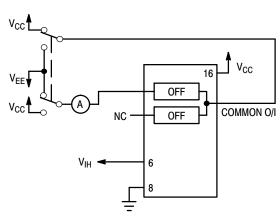


Figure 14. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

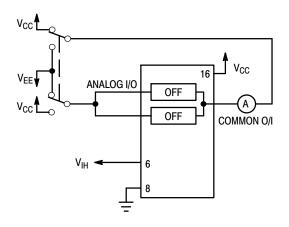


Figure 15. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

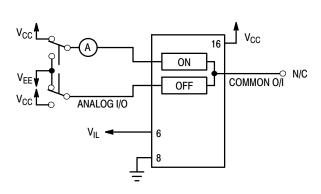


Figure 16. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

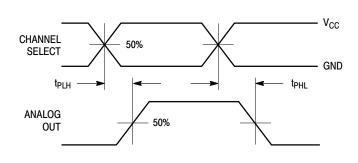
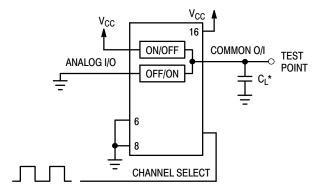
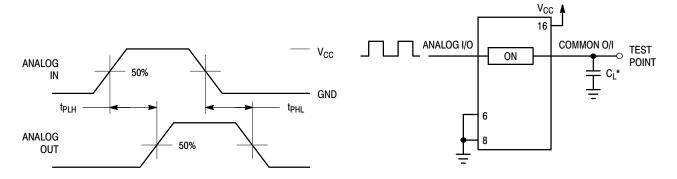


Figure 17. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 18. Propagation Delay, Test Set-Up Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 19. Propagation Delays, Analog In to Analog Out

Figure 20. Propagation Delay, Test Set-Up
Analog In to Analog Out

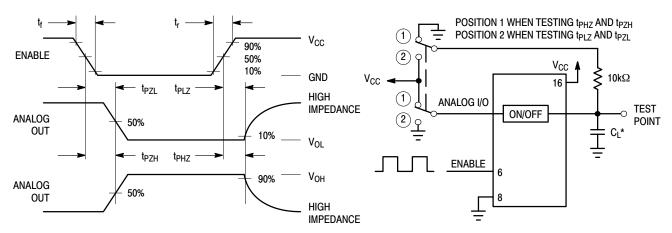


Figure 21. Propagation Delays, Enable to Analog Out

Figure 22. Propagation Delay, Test Set-Up Enable to Analog Out

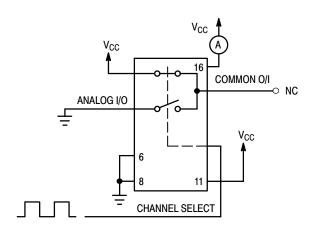


Figure 23. Power Dissipation Capacitance, Test Set-Up

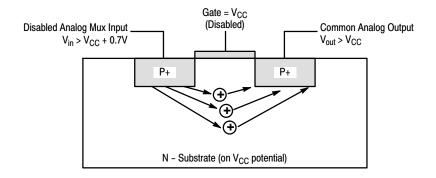


Figure 24. Diagram of Bipolar Coupling Mechanism

Appears if V_{in} exceeds V_{CC} , driving injection current into the substrate

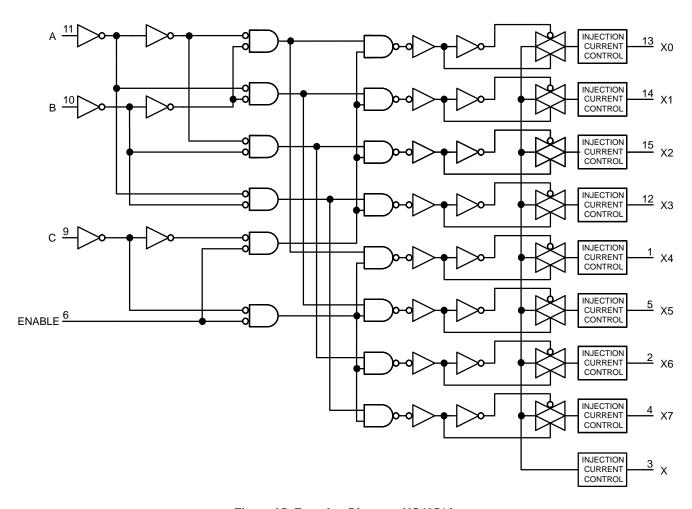


Figure 25. Function Diagram, HC4851A

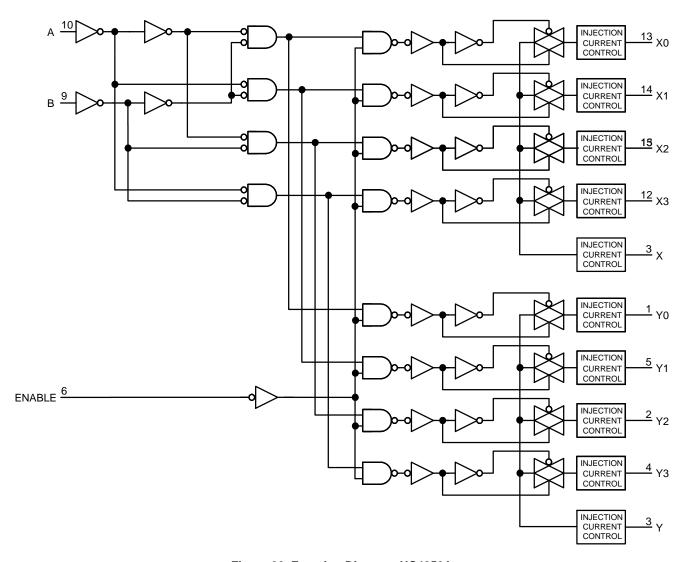


Figure 26. Function Diagram, HC4852A

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC4851ADG		48 Units / Rail
MC74HC4851ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLVHC4851ADR2G*	(2 3 3 3)	2500 Units / Tape & Reel
MC74HC4851ADTR2G	TSSOP-16	2500 Units / Tape & Reel
NLVHC4851ADTR2G*	(Pb-Free)	
MC74HC4851ADWR2G	SOIC-16 WIDE	1000 Units / Tape & Reel
NLVHC4851ADWR2G*	(Pb-Free)	
NLV74HC4851AMNTWG*#	QFN16	3000 Units / Tape & Reel
NLV74HC4851AMN1TWG*#	(Pb-Free)	3000 Units / Tape & Reel

MC74HC4852ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4852ADR2G		2500 Units / Tape & Reel
NLV74HC4852ADR2G*	, ,	2500 Units / Tape & Reel
MC74HC4852ADTR2G	TSSOP-16	2500 Units / Tape & Reel
NLVHC4852ADTR2G*	(Pb-Free)	

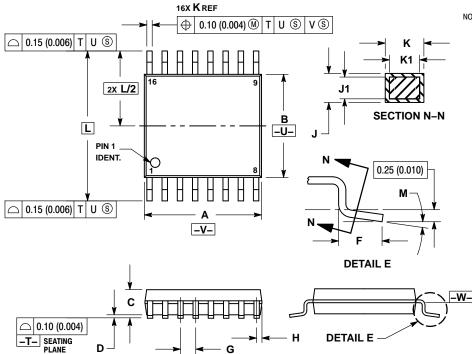
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

[#]MN suffix is with pull-back lead, MN1 is without pull-back lead. Refer to 'Detail A' of case outline on page 16.

PACKAGE DIMENSIONS

TSSOP-16 **DT SUFFIX** CASE 948F **ISSUE B**



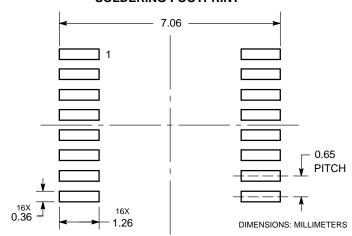
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH.
 PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER
- SIDE.

 JUMENSION B DOES NOT INCLUDE INTERLEAD
 FLASH OR PROTRUSION. INTERLEAD FLASH OR
 PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER
 SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR
- ETHININAL MONIBLE OF A SECTION AS A SEC

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20	-	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252	
м	U o	8 0	0 0	ο 0

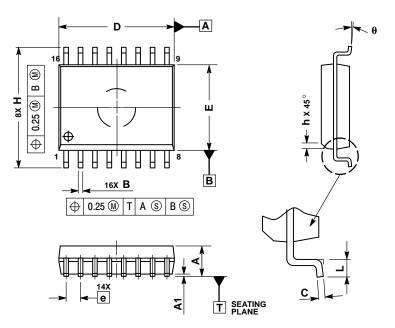
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC-16 WB **DW SUFFIX** CASE 751G-03 ISSUE D



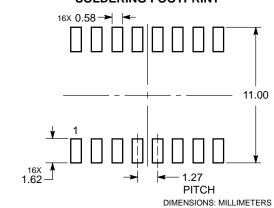
NOTES:

- NOTES:

 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

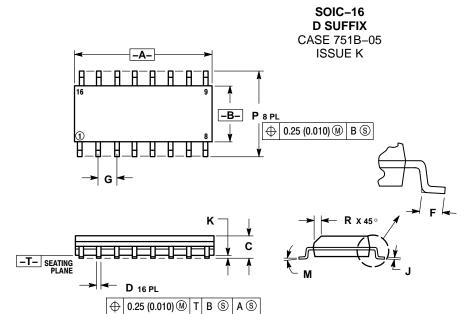
	MILLIMETERS			
DIM	MIN	MAX		
Α	2.35	2.65		
A1	0.10	0.25		
В	0.35	0.49		
С	0.23	0.32		
D	10.15	10.45		
E	7.40	7.60		
е	1.27	BSC		
Н	10.05	10.55		
h	0.25	0.75		
L	0.50	0.90		
а	0 °	7 °		

SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

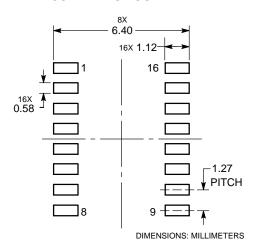


NOTES:

- TES:
 DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD
 PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION
 SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D
 DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0 °	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

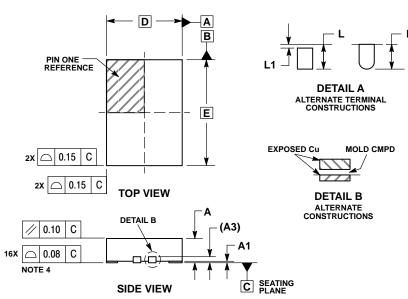
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P CASE 485AW **ISSUE O**



0.15 C A B

F2

⊕ 0.15 C A B

16X b

#

0.10 C A B

0.05 С NOTE 3

Ф

D2

BOTTOM VIEW

DETAIL A

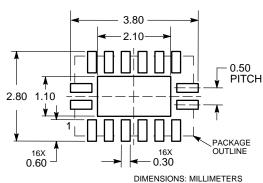
е

e/2

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSIONS b APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN
- 0.15 AND 0.30 MM FROM TERMINAL. COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS.

	MULIMETERS	
	MILLIMETERS	
DIM	MIN	MAX
Α	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
Е	3.50 BSC	
E2	1.85	2.15
е	0.50 BSC	
K	0.20	
٦	0.35	0.45
L1		0.15

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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