





20V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = 25°C		
-20V	1.9Ω @ V _{GS} = -4.5V	-330mA		
	2.4Ω @ $V_{GS} = -2.5V$	-300mA		
	3.4Ω @ V _{GS} = -1.8V	-250mA		
	5Ω @ V _{GS} = -1.5V	-200mA		

Description and Applications

This MOSFET has been designed to minimize the on-state resistance $(R_{DS(on)})$ and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

Features and Benefits

- Low Package Profile, 0.4mm Maximum Package height
- 0.48mm² package footprint, 16 times smaller than SOT23
- Low On-Resistance
- Very low Gate Threshold Voltage, 1.0V max
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

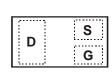
Mechanical Data

- Case: X2-DFN0806-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper leadframe.
 Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (approximate)

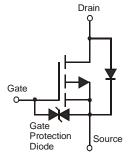




Bottom View



Top View Package Pin Configuration



Equivalent Circuit

Ordering Information (Note 4)

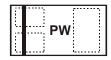
Part Number	Case	Packaging
DMP22D4UFA-7B	DFN0806H4-3	10K/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com.

Marking Information

DMP22D4UFA-7B



Top View Bar Denotes Gate and Source Side

PW = Product Type Marking Code



Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	V _{DSS}	-20	V		
Gate-Source Voltage	V _{GSS}	±8	V		
Continuous Davis Compant (Nata 5) V	Steady State	T _A = 25°C T _A = 70°C	I _D	-330 -260	mA
Continuous Drain Current (Note 5) V _{GS} = -4.5V	t<10s	T _A = 25°C T _A = 70°C	I _D	-400 -310	mA
Continuous Drain Compart (Nata 5) V 4 0V	Steady State	T _A = 25°C T _A = 70°C	I _D	-250 -200	mA
Continuous Drain Current (Note 5) V _{GS} = -1.8V	t<10s	T _A = 25°C T _A = 70°C	I _D	-310 -240	mA
Pulsed Drain Current (Note 6)	I _{DM}	-800	mA		

Thermal Characteristics @TA = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units	
Total Power Dissipation (Note 5)	Steady state	P_{D}	400	mW
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	6	310	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{\theta JA}$	220	°C/W
Operating and Storage Temperature Range	$T_{J_1}T_{STG}$	-55 to +150	°C	

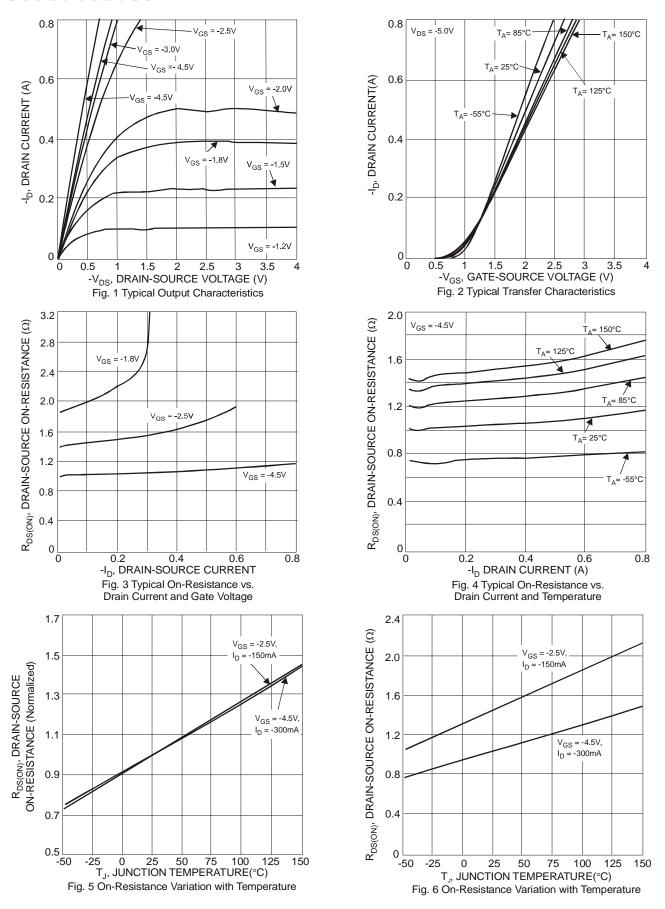
Electrical Characteristics @TA = 25°C unless otherwise specified

Characteristic		Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage		BV _{DSS}	-20	-	-	V	$V_{GS} = 0V, I_{D} = -250\mu A$
Zara Cata Valtaga Drain Current	@T _c = 25°C	I _{DSS}	1	-	100	nA	$V_{DS} = -16V, V_{GS} = 0V$
Zero Gate Voltage Drain Current			-	-	50		$V_{DS} = -5V$, $V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	-	-	±100	nA	$V_{GS} = \pm 5V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage		$V_{GS(th)}$	-0.4	-	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
			-	1.2	1.9		$V_{GS} = -4.5V$, $I_{D} = -100$ mA
			1	1.5	2.4		$V_{GS} = -2.5V, I_D = -50mA$
Static Drain-Source On-Resistance		R _{DS (ON)}	-	2.1	3.4	Ω	$V_{GS} = -1.8V, I_D = -20mA$
			-	2.5	5		$V_{GS} = -1.5V, I_D = -10mA$
			-	4.0	-		$V_{GS} = -1.2V, I_D = -1mA$
Forward Transfer Admittance		Y _{fs}	100	450	-	mS	$V_{DS} = -5V, I_{D} = -125mA$
Diode Forward Voltage		V _{SD}	-	-0.6	-1.0	V	$V_{GS} = 0V$, $I_S = -10mA$
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance		C _{iss}	•	28.7	-	pF	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Output Capacitance	Output Capacitance		ı	4.2	-	pF	$V_{DS} = -15V, V_{GS} = 0V,$ -f = 1.0MHz
Reverse Transfer Capacitance		C _{rss}	1	2.9	-	pF	1 = 1.01011 12
Gate Resistance		R _G	-	0.4	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge		Qg	-	0.4	-	nC	15// // 40//
Gate-Source Charge		Q _{gs}	-	0.08	-	nC	$V_{GS} = -4.5V, V_{DS} = -10V,$ $V_{DS} = -250 \text{mA}$
Gate-Drain Charge		Q_{gd}	-	0.06	-	nC	ID = -250IIIA
Turn-On Delay Time		t _{D(on)}	-	5.8	-	ns	
Turn-On Rise Time		t _r	-	5.7	-	ns	$V_{DD} = -15V, V_{GS} = -4.5V,$
Turn-Off Delay Time		t _{D(off)}	-	31.1	-	ns	$R_G = 2\Omega, I_D = -200 \text{mA}$
Turn-Off Fall Time		t _f	1	16.4	-	ns	7

5. Device mounted on FR-4 PCB, with minimum recommended pad layout. Notes:

Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
 Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.







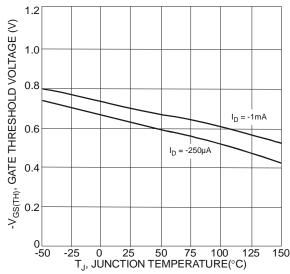
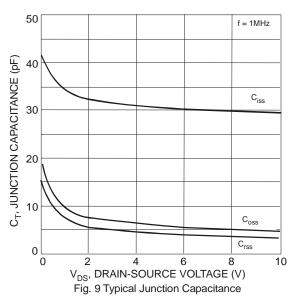
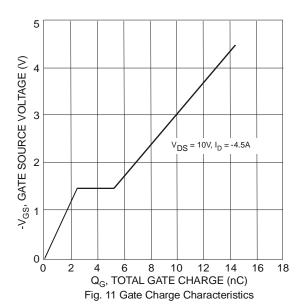
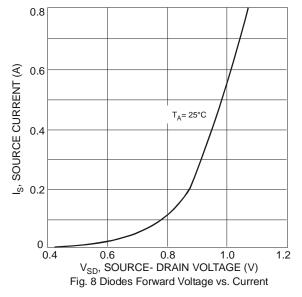
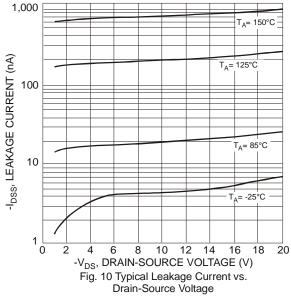


Fig. 7 Gate Threshold Variation vs. Ambient Temperature



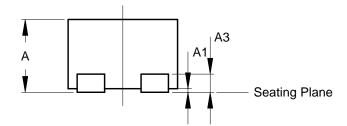


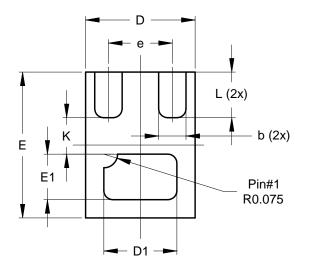






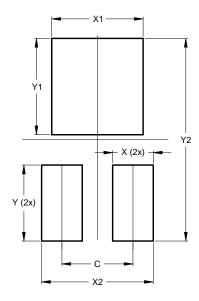
Package Outline Dimensions





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X2-DFN0806-3						
Dim	Min	Max	Тур			
Α	0.375	0.40	0.39			
A1	0	0.05	0.02			
А3	-	-	0.10			
b	0.10	0.20	0.15			
D	0.55	0.65	0.60			
D1	0.35	0.45	0.40			
E	0.75	0.85	0.80			
E1	0.20	0.30	0.25			
е	-	-	0.35			
K	-	-	0.20			
L	0.20	0.30	0.25			
All Dimensions in mm						

Suggested Pad Layout



Dimensions	(in mm)		
С	0.350		
Х	0.200		
X1	0.450		
X2	0.550		
Υ	0.375		
Y1	0.475		
Y2	1.000		



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