

N-Channel Reduced Q_g, Fast Switching MOSFET

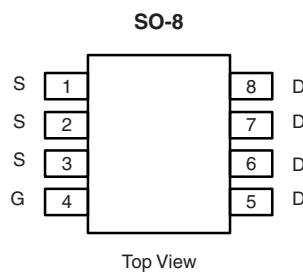
PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
30	0.0032 at V _{GS} = 10 V	25
	0.0036 at V _{GS} = 4.5 V	22

FEATURES

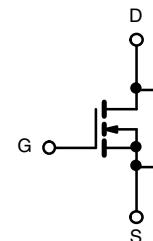
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Switching Losses Improvement
- TrenchFET® Gen II Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4368DY-T1-E3 (Lead (Pb)-free)
Si4368DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

APPLICATIONS

- Low-Side DC/DC Conversion
 - Notebook, Server, VRM Module
- Fixed Telecom

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	30	± 12	V	
Gate-Source Voltage	V _{GS}				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	25	A	
	T _A = 70 °C		20		
Pulsed Drain Current (10 µs Pulse Width)	I _{DM}	70			
Continuous Source Current (Diode Conduction) ^a	I _S	2.9	1.3		
Avalanche Current	I _{AS}	50		W	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.5		
	T _A = 70 °C		2.2		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	29	°C/W
	Steady State		67	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	13	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$		5		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$		0.0026	0.0032	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 22 \text{ A}$		0.0029	0.0036	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 25 \text{ A}$		150		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.66	1.1	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		8340		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			355		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$		53	80	nC
Gate-Source Charge	Q_{gs}			17.5		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.8	1.2	1.8	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}$, $R_L = 15 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 6 \Omega$		25	38	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(\text{off})}$			172	260	
Fall Time	t_f			41	62	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$		42	60	

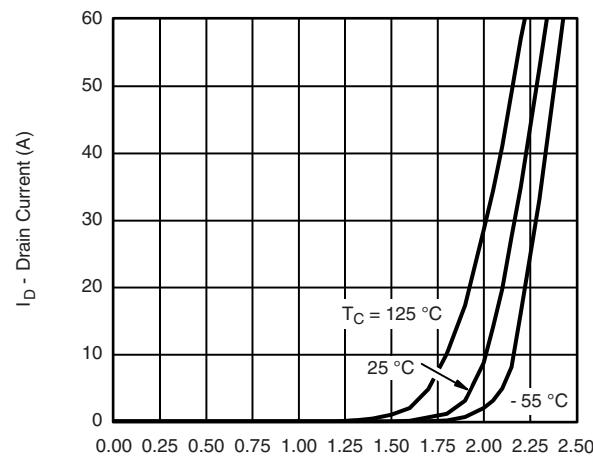
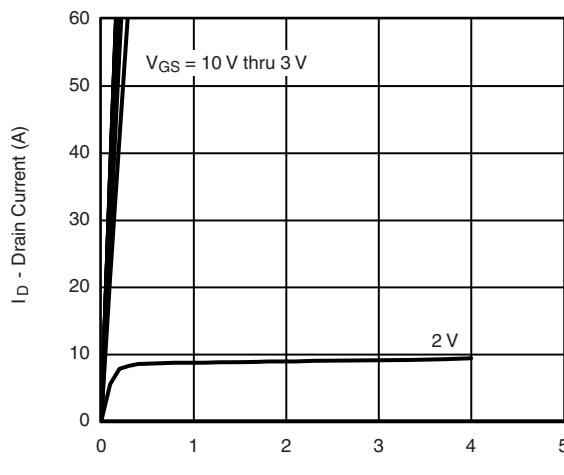
Notes:

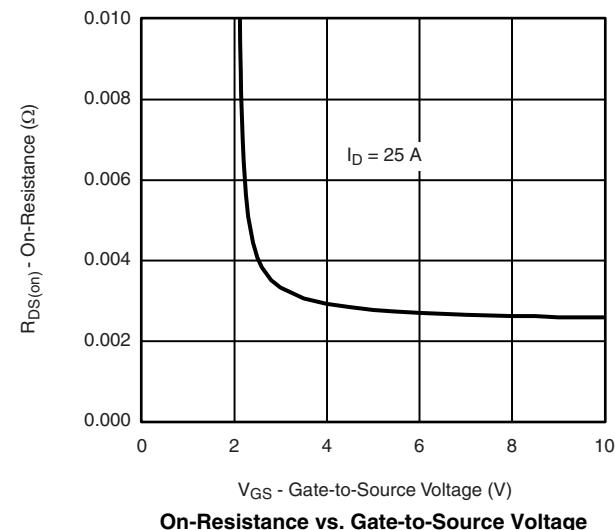
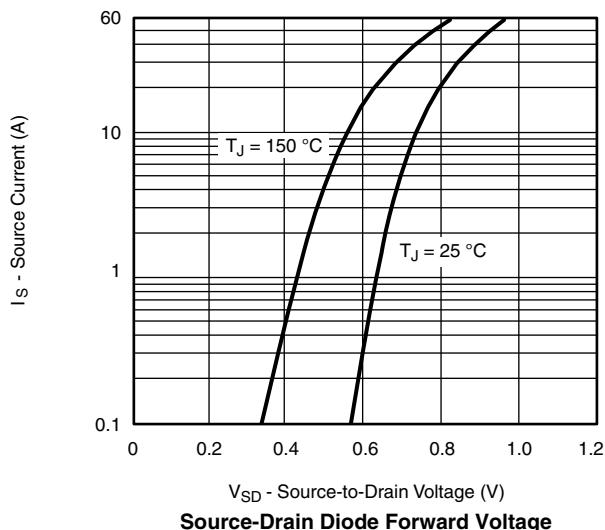
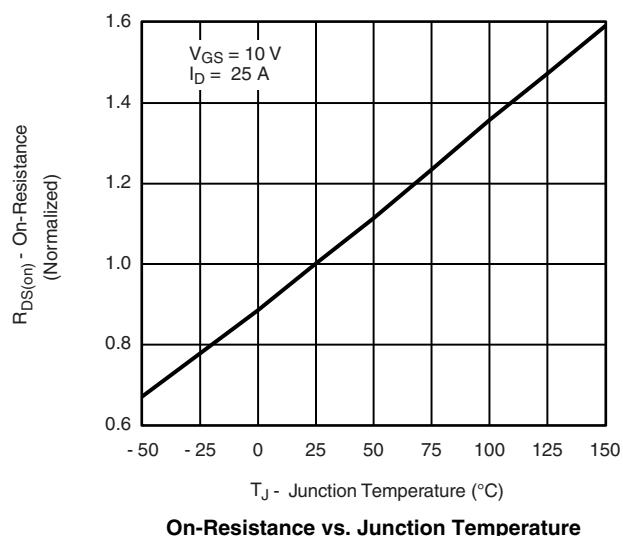
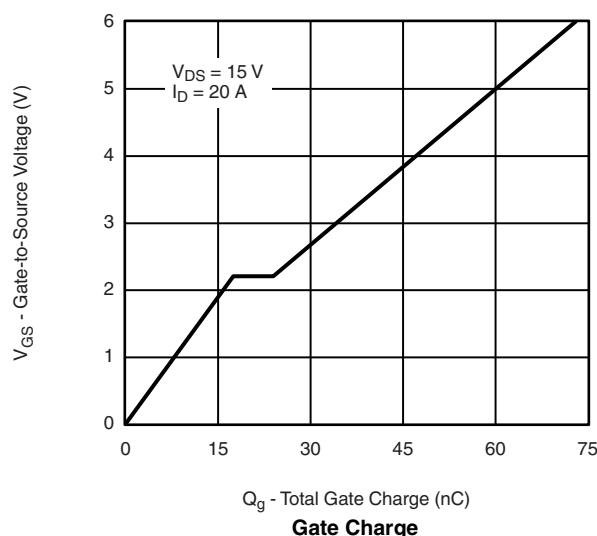
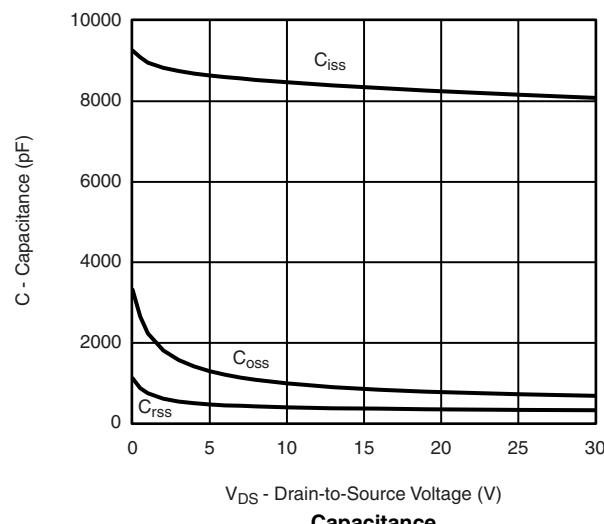
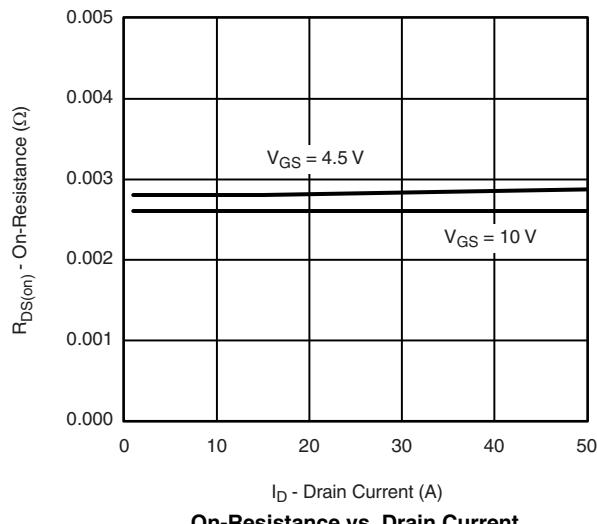
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$.

b. Guaranteed by design, not subject to production testing.

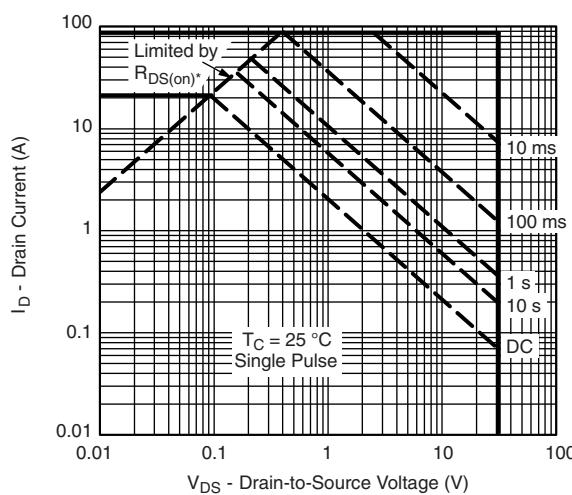
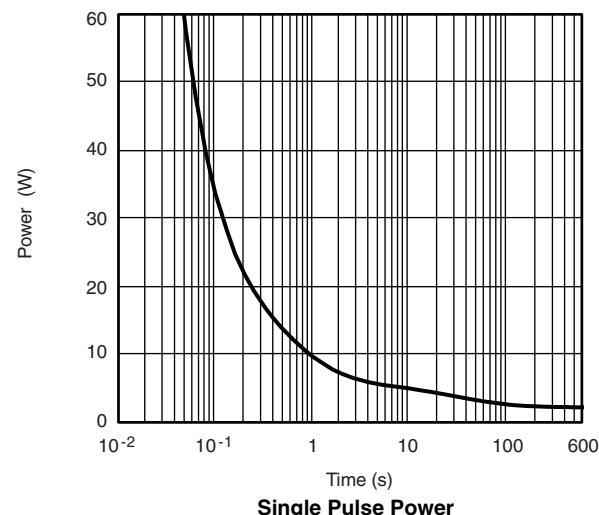
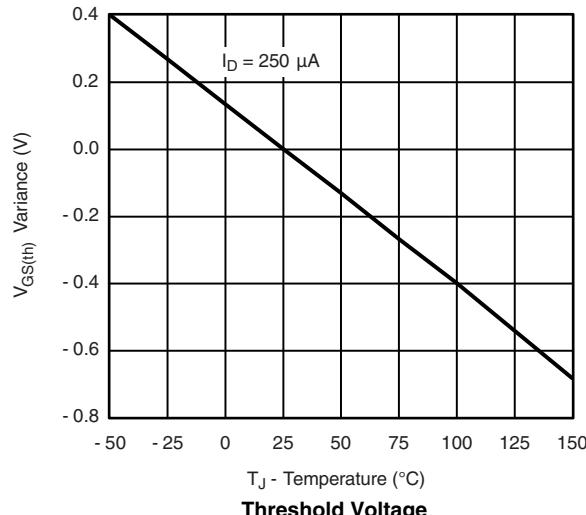
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



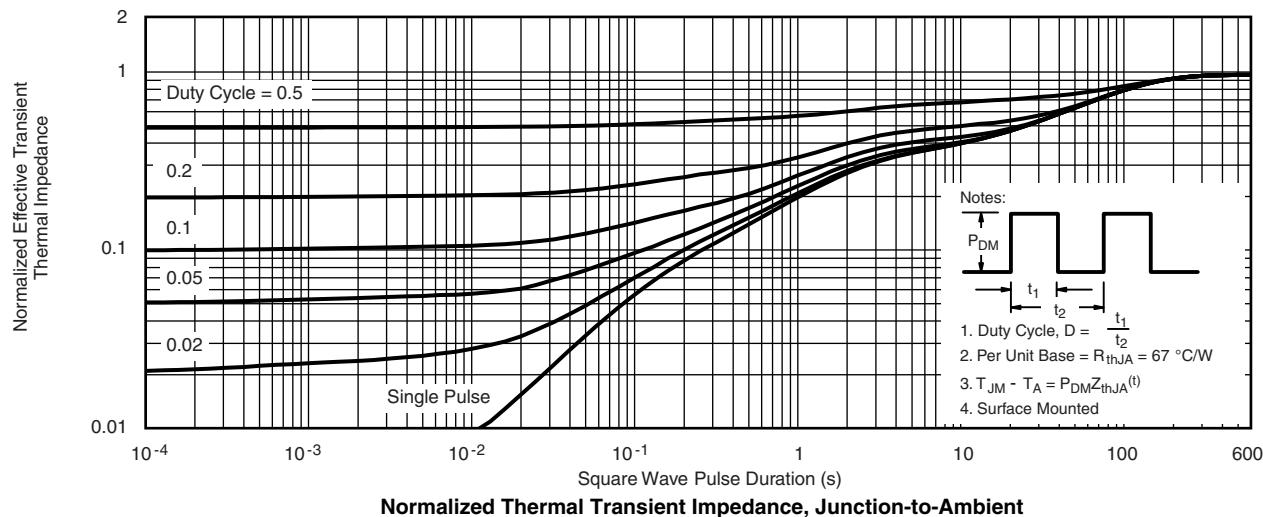
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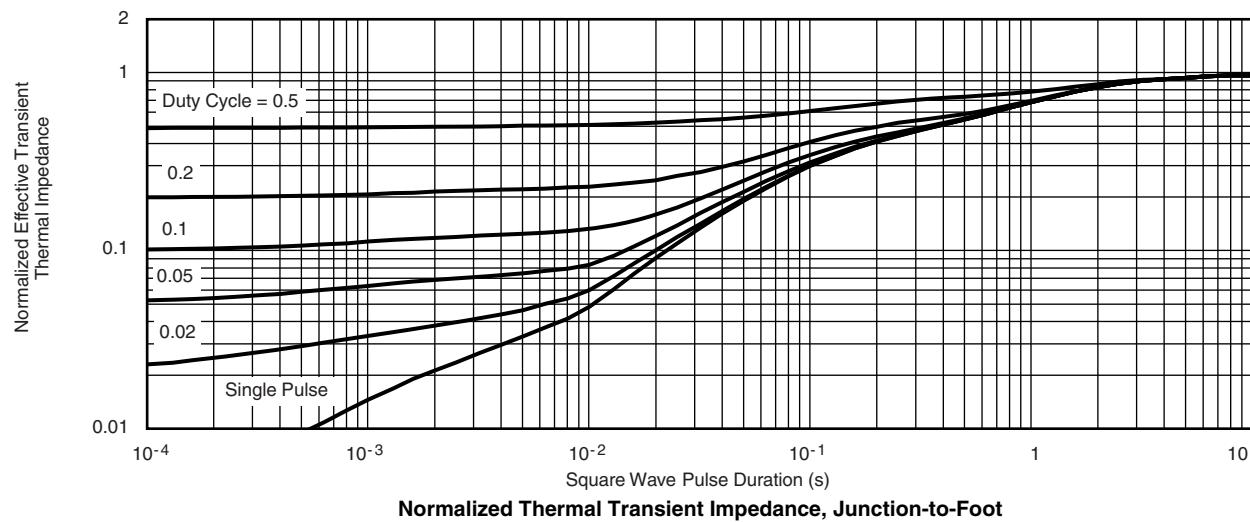


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



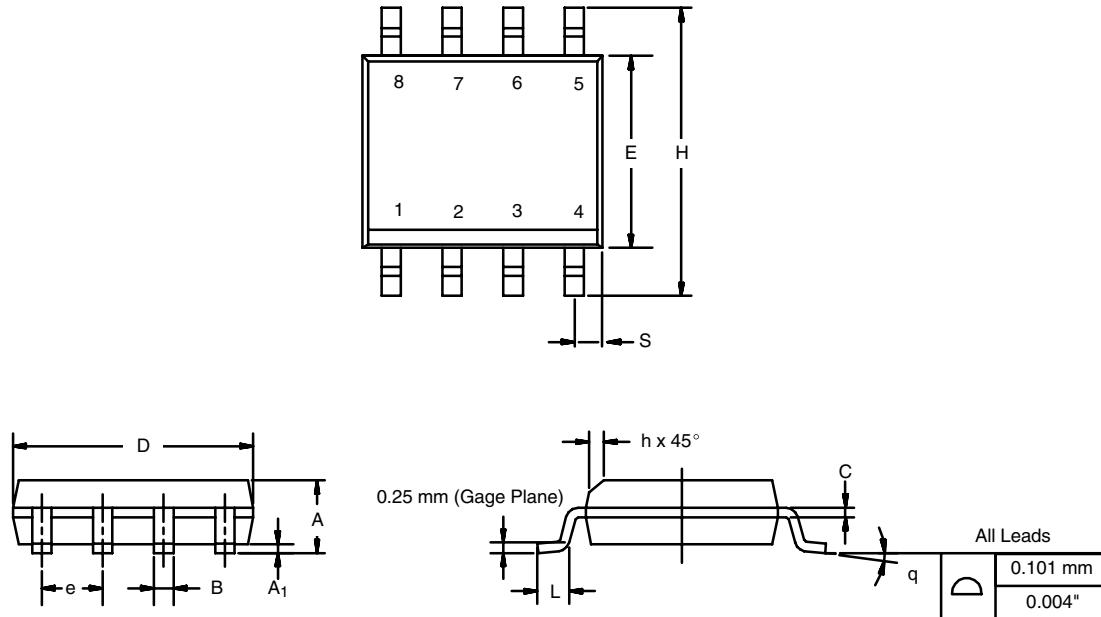
Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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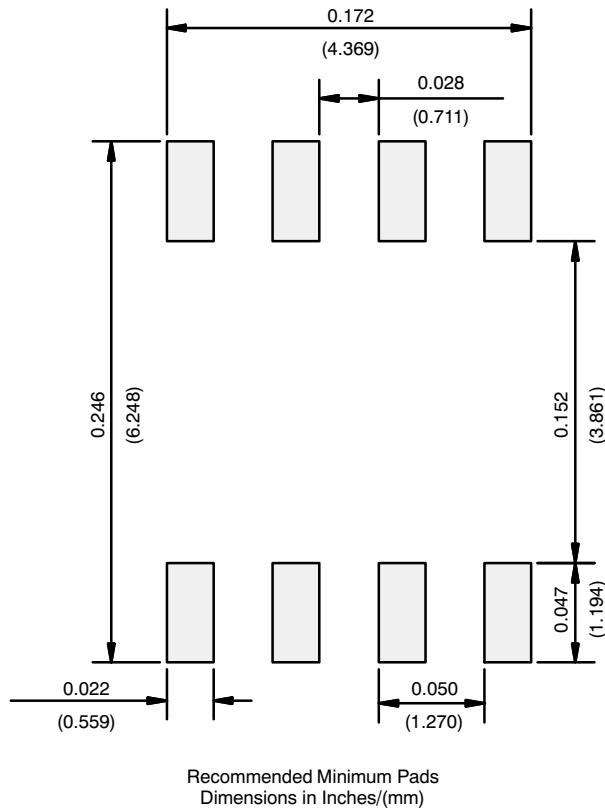
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



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