150W STEREO / 300W MONO PurePath™ HD ANALOG-INPUT POWER STAGE

Check for Samples: TAS5613A

FEATURES

- **Active Enabled Integrated Feedback Provides: (PurePath™ HD)**
  - **Signal Bandwidth up to 80kHz for High Frequency Content From HD Sources**
  - **Ultra Low 0.03% THD at 1W into 4Ω**
  - **Flat THD at all Frequencies for Natural Sound**
  - **80dB PSRR (BTL, No Input Signal)**
  - **>100dB (A Weighted) SNR**
  - **Click and Pop Free Startup and Stop**
- **Pin compatible with TAS5630, TAS5615 and TAS5611**
- **Multiple Configurations Possible on the Same PCB:**
  - **Mono Parallel Bridge Tied Load (PBTL)**
  - **Stereo Bridge Tied Load (BTL)**
  - **2.1 Single Ended (SE) Stereo Pair and Bridge Tied Load Subwoofer**
- **Total Output Power at 10%THD+N**
  - **300W in Mono PBTL Configuration**
  - **150W per Channel in Stereo BTL Configuration**
- **Total Output Power in BTL Configuration at 1%THD+N**
  - **160W Stereo into 3Ω**
  - **125W Stereo into 4Ω**
  - **85W Stereo into 6Ω**
  - **65W Stereo into 8Ω**
- **>90% Efficient Power Stage With 60-mΩ Output MOSFETs**
- **Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short Circuit Protection) With Error Reporting**
- **EMI Compliant When Used With Recommended System Design**
- **Thermally Enhanced Package Options:**
  - **PHD (64-pin QFP)**
  - **DKD (44-pin PSOP3)**

APPLICATIONS

- **Home Theater Systems**
- **AV Receivers**
- **DVD/ Blu-ray Disk™ Receivers**
- **Mini Combo Systems**
- **Active Speakers and Subwoofers**

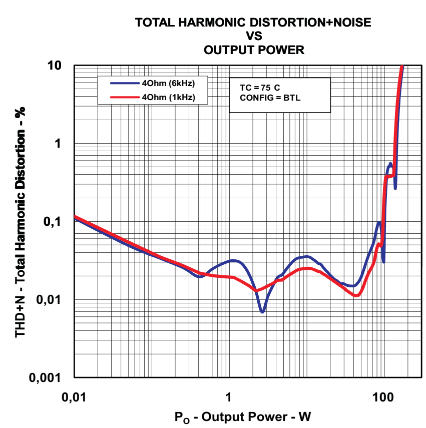
DESCRIPTION

The TAS5613A is a high-performance analog input Class D amplifier with integrated closed loop feedback technology (known as PurePath™ HD). It has the ability to drive up to 150 W.(1) Stereo into 4Ω speakers from a single 36V supply.

PurePath™ HD technology enables traditional AB-Amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class D amplifiers.

Unlike traditional Class-D amplifiers, the distortion curve only increases once the output levels move into clipping.

PurePath™ HD technology enables lower idle losses making the device even more efficient.



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high performance thermal interface material between the package exposed heatslug and the heat sink should be used to achieve high output power levels

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

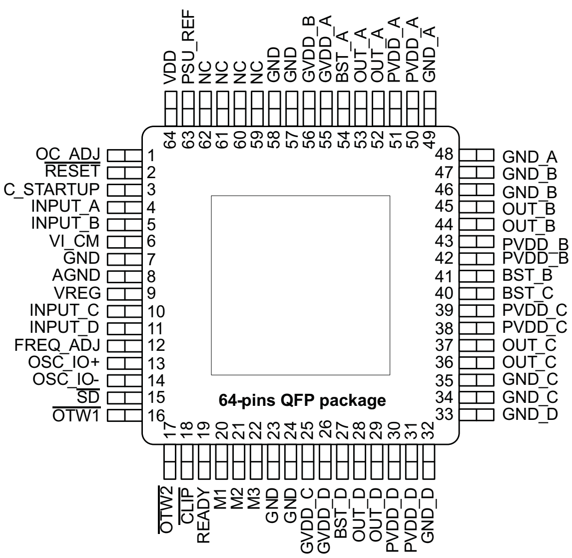
Pin Assignment

The TAS5613A is available in two thermally enhanced packages:

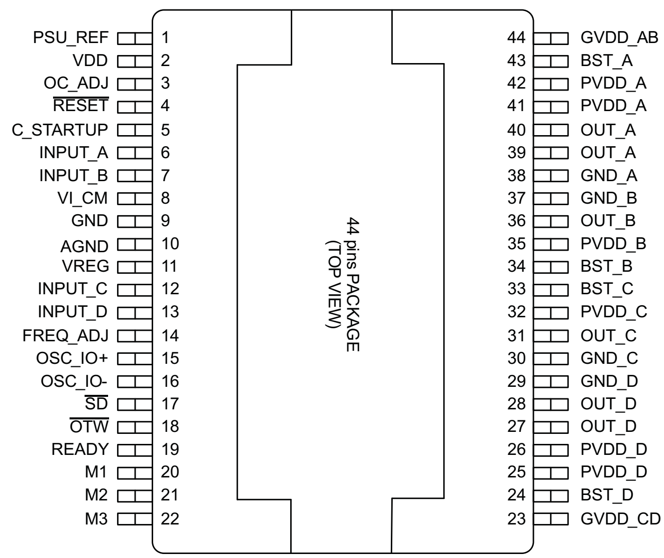
- 64-Pin QFP (PHD) Power Package
- 44-Pin PSOP3 Package (DKD)

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

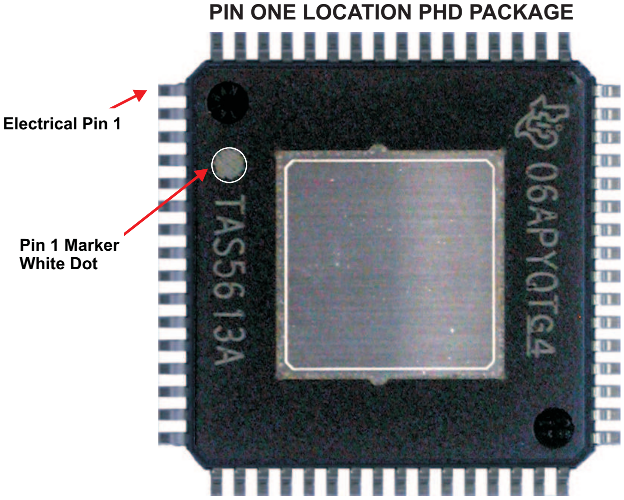
PHD PACKAGE (TOP VIEW)



DKD PACKAGE (TOP VIEW)



PIN ONE LOCATION PHD PACKAGE



MODE SELECTION PINS

<table>
<tr><th colspan="3">MODE PINS</th><th rowspan="2">ANALOG INPUT</th><th rowspan="2">OUTPUT CONFIGURATION</th><th rowspan="2" colspan="3">DESCRIPTION</th></tr>
<tr><th>M3</th><th>M2</th><th>M1</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Differential</td><td>2 × BTL</td><td colspan="3">AD mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>—</td><td>—</td><td colspan="3">Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Differential</td><td>2 × BTL</td><td colspan="3">BD mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Differential (BTL)
Single Ended (SE)</td><td>1 × BTL + 2 × SE</td><td colspan="3">BTL = BD mode, SE = AD mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Single Ended</td><td>4 × SE</td><td colspan="3">AD mode</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">0</td><td rowspan="3">1</td><td rowspan="3">Differential</td><td rowspan="3">1 × PBTL</td><th>INPUT_C (1)</th><th>INPUT_D (1)</th><th></th></tr>
<tr><td>0</td><td>0</td><td>AD mode</td></tr>
<tr><td>1</td><td>0</td><td>BD mode</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td rowspan="2" colspan="5">Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>

(1) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode (1=VREG and 0=GND).

PACKAGE HEAT DISSIPATION RATINGS (1)

PARAMETER	TAS5613APHD	TAS5613ADKD
$R_{\theta JC}$ (°C/W) – 2 BTL or 4 SE channels	3.2	2.1
$R_{\theta JC}$ (°C/W) – 1 BTL or 2 SE channel(s)	5.4	3.5
$R_{\theta JC}$ (°C/W) – 1 SE channel	7.9	5.1
Pad Area (2)	64 mm^2	80 mm^2

(1) J_C is junction-to-case, CH is case-to-heat sink
(2) $R_{\theta H}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heat sink and both channels active. The $R_{\theta CH}$ with this condition is 1.22°C/W for the PHD package and 1.02°C/W for the DKD package.

Table 1. ORDERING INFORMATION (1)

T_A	PACKAGE	DESCRIPTION
0°C–70°C	TAS5613APHD	64 pin HTQFP
	TAS5613ADKD	44 pin PSOP3

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted [(1)]

TAS5613A			UNIT
VDD to GND		–0.3 to 13.2	V
GVDD to GND		–0.3 to 13.2	V
PVDD_X to GND_X [(2)]		–0.3 to 53	V
OUT_X to GND_X [(2)]		–0.3 to 53	V
BST_X to GND_X [(2)]		–0.3 to 66.2	V
BST_X to GVDD_X [(2)]		–0.3 to 53	V
VREG to GND		–0.3 to 4.2	V
GND_X to GND		–0.3 to 0.3	V
GND to AGND		–0.3 to 0.3	V
OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO–, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to GND		–0.3 to 4.2	V
INPUT_X		–0.3 to 7	V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$ to GND		–0.3 to 7	V
Continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$)		9	mA
Operating junction temperature range, T_J		0 to 150	°C
Storage temperature, T_{stg}		–40 to 150	°C
Electrostatic discharge	Human-Body Model [(3)] (all pins)	±2	kV
	Charged-Device Model [(3)] (all pins)	±500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

(3) Failure to follow good anti-static ESD handling during manufacture and rework will contribute to device malfunction. Make sure the operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	18	36	38	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter according to Figure 12 and Figure 13	3.5	4		Ω
R_L(SE)			2.8	3		
R_L(PBTL)			1.6	2		
R_L (BTL)	Load impedance	Output filter according to Figure 12 + Schottky, R_{OC} = 22kΩ	2.8	3		Ω
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	7	10		μH
L_{OUT}(SE)			7	15		
L_{OUT}(PBTL)			7	10		
F_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	385	400	415	kHz
		AM1	315	333	350	
		AM2	260	300	335	
R_{FREQ_ADJ}	PWM frame rate programming resistor	Nominal; Master mode	9.9	10	10.1	kΩ
		AM1; Master mode	19.8	20	20.2	
		AM2; Master mode	29.7	30	30.3	
C_{PVDD}	PVDD close decoupling capacitors			2.0		μF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22	30		kΩ
$R_{OC\_LATCHED}$	Over-current programming resistor	Resistor tolerance = 5%	47	64		kΩ
V_{FREQ_ADJ}	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
T_J	Junction temperature		0		125	°C

PIN FUNCTIONS

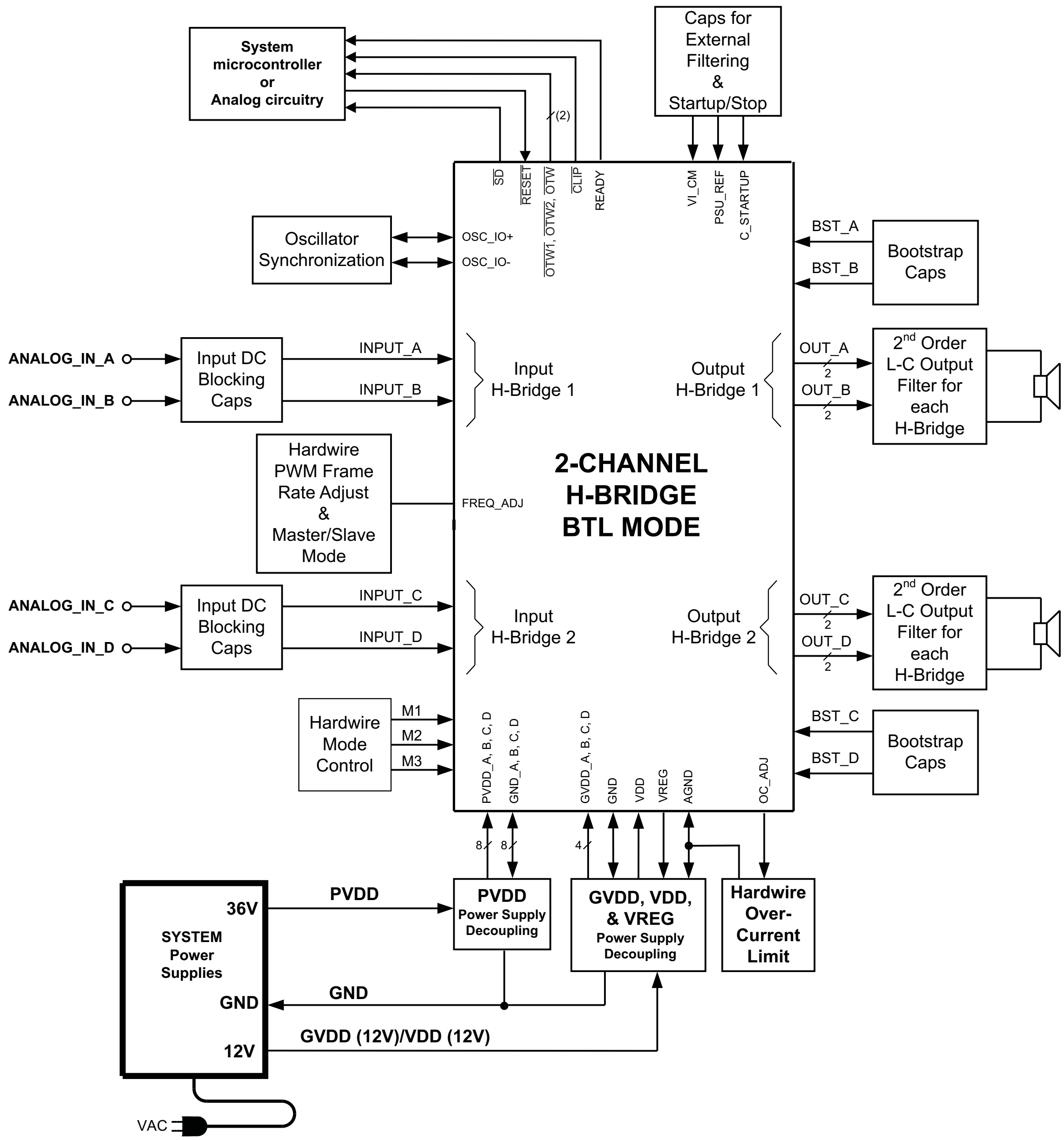
PIN			FUNCTION(1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
AGND	8	10	P	Analog ground
BST_A	54	43	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_A required.
BST_B	41	34	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_B required.
BST_C	40	33	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_C required.
BST_D	27	24	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_D required.
$\overline{\text{CLIP}}$	18	–	O	Clipping warning; open drain; active low
C_STARTUP	3	5	O	Startup ramp requires a charging capacitor of 4.7nF to GND
FREQ_ADJ	12	14	I	PWM frame rate programming pin requires resistor to GND
GND	7, 23, 24, 57, 58	9	P	Ground
GND_A	48, 49	38	P	Power ground for half-bridge A
GND_B	46, 47	37	P	Power ground for half-bridge B
GND_C	34, 35	30	P	Power ground for half-bridge C
GND_D	32, 33	29	P	Power ground for half-bridge D
GVDD_A	55	–	P	Gate drive voltage supply requires 0.1 μF capacitor to GND_A
GVDD_B	56	–	P	Gate drive voltage supply requires 0.1 μF capacitor to GND_B
GVDD_C	25	–	P	Gate drive voltage supply requires 0.1 μF capacitor to GND_C
GVDD_D	26	-	P	Gate drive voltage supply requires 0.1 uF capacitor to GND_D
GVDD_AB	–	44	P	Gate drive voltage supply requires 0.22 μF capacitor to GND_A/GND_B
GVDD_CD	–	23	P	Gate drive voltage supply requires 0.22 μF capacitor to GND_C/GND_D

(1) I = Input, O = Output, P = Power

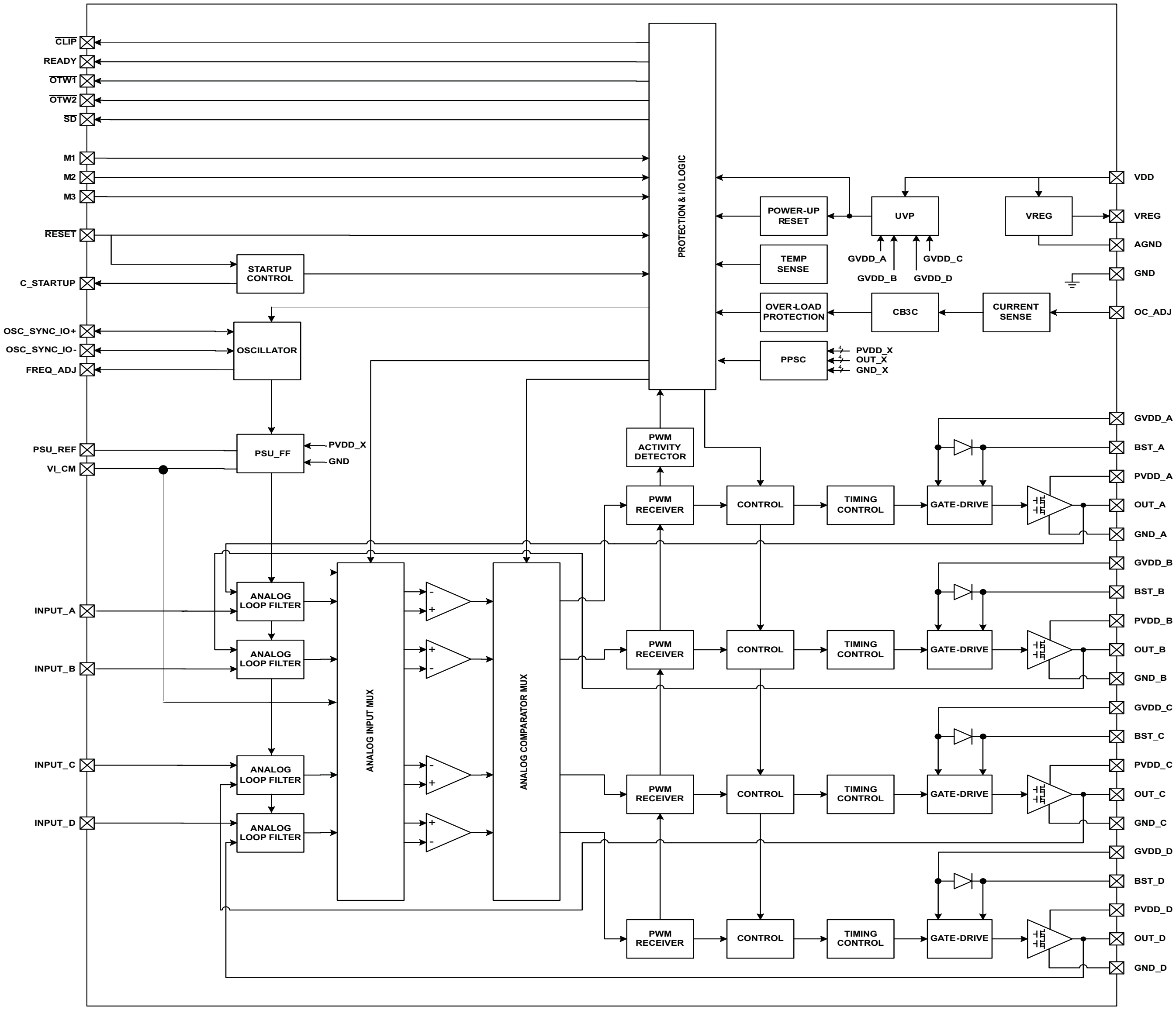
PIN FUNCTIONS (continued)

PIN			FUNCTION(1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
INPUT_A	4	6	I	Input signal for half bridge A
INPUT_B	5	7	I	Input signal for half bridge B
INPUT_C	10	12	I	Input signal for half bridge C
INPUT_D	11	13	I	Input signal for half bridge D
M1	20	20	I	Mode selection
M2	21	21	I	Mode selection
M3	22	22	I	Mode selection
NC	59-62	–	–	No connect, pins may be grounded.
OC_ADJ	1	3	O	Analog over current programming pin requires 30kΩ resistor to ground:
OSC_IO+	13	15	I/O	Oscillator master/slave output/input.
OSC_IO–	14	16	I/O	Oscillator master/slave output/input.
/OTW	-	18	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW1}}$	16	–	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW2}}$	17	–	O	Overtemperature warning signal, open drain, active low.
OUT_A	52, 53	39, 40	O	Output, half bridge A
OUT_B	44, 45	36	O	Output, half bridge B
OUT_C	36, 37	31	O	Output, half bridge C
OUT_D	28, 29	27, 28	O	Output, half bridge D
PSU_REF	63	1	P	PSU Reference requires close decoupling of 330pF to GND
PVDD_A	50, 51	41, 42	P	Power supply input for half bridges A requires close decoupling of 2μF capacitor to GND_A.
PVDD_B	42, 43	35	P	Power supply input for half bridges B requires close decoupling of 2μF capacitor to GND_B.
PVDD_C	38, 39	32	P	Power supply input for half bridges C requires close decoupling of 2μF capacitor to GND_C.
PVDD_D	30, 31	25, 26	P	Power supply input for half bridges D requires close decoupling of 2μF capacitor to GND_D.
READY	19	19	O	Normal operation; open drain; active high
$\overline{\text{RESET}}$	2	4	I	Device reset Input; active low, requires 47kΩ pull up resistor to VREG
$\overline{\text{SD}}$	15	17	O	Shutdown signal, open drain, active low
VDD	64	2	P	Power supply for internal voltage regulator requires a 10-μF capacitor with a 0.1-μF capacitor to GND for decoupling.
VI_CM	6	8	O	Analog comparator reference node requires close decoupling of 1nF to GND
VREG	9	11	P	Internal regulator supply filter pin requires 0.1-μF capacitor to GND

TYPICAL SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



AUDIO CHARACTERISTICS (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 36V, GVDD_X = 12V, R_L = 4Ω, f_S = 400kHz, R_{OC} = 30kΩ, T_C = 75°C, Output Filter: L_{DEM} = 7μH, C_{DEM} = 680nF, mode = 010, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3Ω, 10% THD+N (R_{OC} = 22kΩ, add Schottky diodes from OUT_X to GND_X)		200		W
		R_L = 4Ω, 10% THD+N		150		
		R_L = 3Ω, 1% THD+N (R_{OC} = 22kΩ, add Schottky diodes from OUT_X to GND_X)		160		
		R_L = 4Ω, 1% THD+N		125		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		185		μV
$\|V_{OS}\|$	Output offset voltage	Inputs AC coupled to GND		8	25	mV
SNR	Signal-to-noise ratio(1)			100		dB
DNR	Dynamic range			100		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching(2)		1.8		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

AUDIO CHARACTERISTICS (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 36V, GVDD_X = 12V, R_L = 2Ω, f_S = 400 kHz, R_{OC} = 30kΩ, T_C = 75°C, Output Filter: L_{DEM} = 7μH, C_{DEM} = 680nF, MODE = 101-BD, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2Ω, 10% THD+N		300		W
		R_L = 3Ω, 10% THD+N		200		
		R_L = 4Ω, 10% THD+N		160		
		R_L = 2Ω, 1% THD+N		250		
		R_L = 3Ω, 1% THD+N		160		
		R_L = 4Ω, 1% THD+N		130		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted		182		μV
SNR	Signal to noise ratio(1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted		100		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		1.8		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

PVDD_X = 36V, GVDD_X = 12V, VDD = 12V, T_C (Case temperature) = 75°C, f_S = 400kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node	VDD = 12V	3	3.3	3.6	V
	Analog comparator reference node, VI_CM		1.5	1.75	1.9	V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		20		mA
		Idle, reset mode		20		
I_{GVDD_x}	Gate-supply current per half-bridge	50% duty cycle		10		mA
		Reset mode		1.5		
I_{PVDD_x}	Half-bridge idle current	50% duty cycle with recommended output filter		12.5		mA
		Reset mode, No switching		620		μA
ANALOG INPUTS						
R_{IN}	Input resistance	READY = HIGH		33		kΩ
V_{IN}	Maximum input voltage swing			7		V
I_{IN}	Maximum input current				1	mA
G	Inverting voltage Gain, (V_{OUT}/V_{IN})			21		dB
OSCILLATOR						
f_{OSC_IO+}	Nominal, Master Mode	F_{PWM} × 10	3.85	4	4.15	MHz
	AM1, Master Mode		3.15	3.33	3.5	
	AM2, Master Mode		2.6	3	3.35	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, Includes metallization resistance, GVDD = 12V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	mΩ
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x and VDD			9.5		V
$V_{uvp,hyst}$ (1)				0.6		V
OTW	Overtemperature warning 1, $\overline{\text{OTW1}}$ (1)		95	100	105	°C
	Overtemperature warning 2, $\overline{\text{OTW}}$, $\overline{\text{OTW2}}$ (1)		115	125	135	°C
OTW_{HYST} (1)	Temperature drop needed below OTW temperature for $\overline{\text{OTW}}$ to be inactive after $\overline{\text{OTW}}$ event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
OTE-$OTW_{differential}$ (1)	OTE-OTW differential			30		°C
OTE_{HYST} (1)	A reset needs to occur for $\overline{\text{SD}}$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 400kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 30kΩ		14		A
		Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22kΩ (with Schottky diodes on output nodes)		18		
$I_{OC\_LATCHED}$	Overcurrent limit protection	Resistor – programmable, peak current in 1Ω load, R_{OCP} = 64kΩ		14		A
		Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 47kΩ (with Schottky diodes on output nodes)		18		
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent.		150		ns
I_{PD}	Output pulldown current of each half	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA

(1) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 36V, GVDD_X = 12V, VDD = 12V, T_C (Case temperature) = 75°C, f_S = 400kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	INPUT_X, M1, M2, M3, RESET	1.9			V
V_{IL}	Low level input voltage	INPUT_X, M1, M2, M3, RESET			0.8	V
Leakage	Input leakage current				100	μA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{OTW1}}$ to VREG, $\overline{\text{OTW2}}$ to VREG, $\overline{\text{SD}}$ to VREG		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7kΩ to 5V	4.5		5	V
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
FANOUT	Device fanout $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{SD}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$	No external pullup		30		devices

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

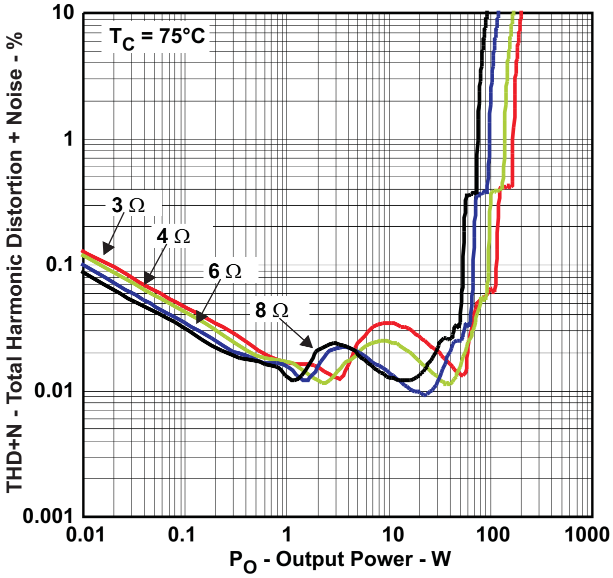


Figure 1.

OUTPUT POWER vs SUPPLY VOLTAGE

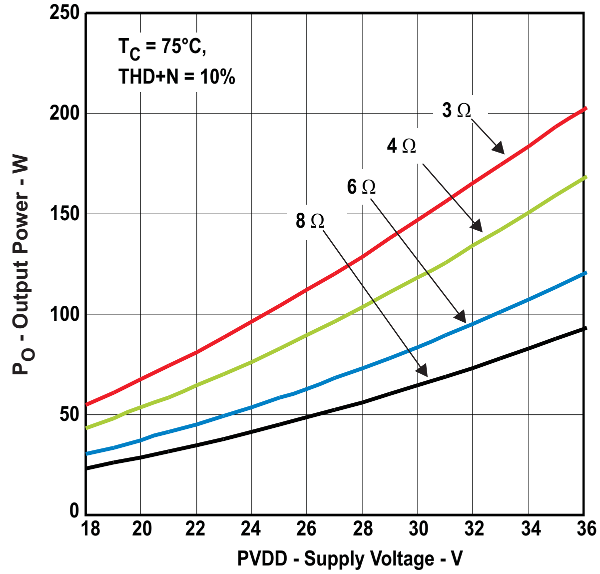


Figure 2.

UNCLIPPED OUTPUT POWER vs SUPPLY VOLTAGE

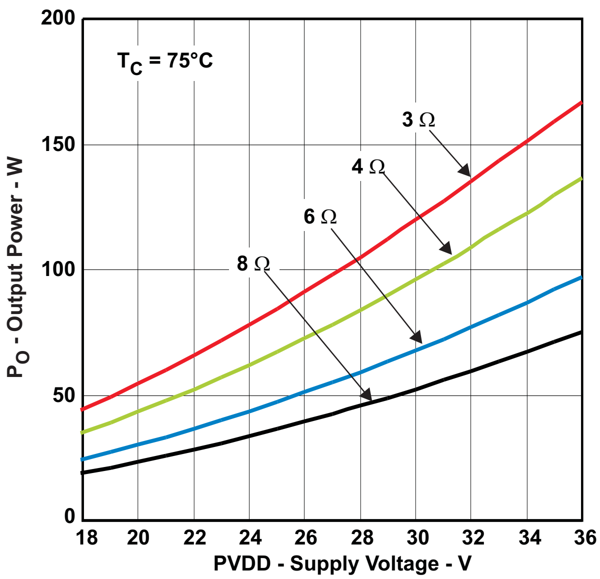


Figure 3.

SYSTEM EFFICIENCY vs OUTPUT POWER

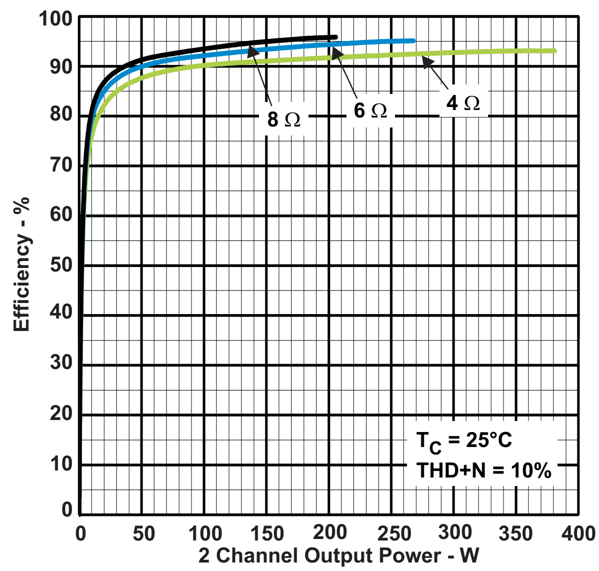


Figure 4.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

SYSTEM POWER LOSS vs OUTPUT POWER

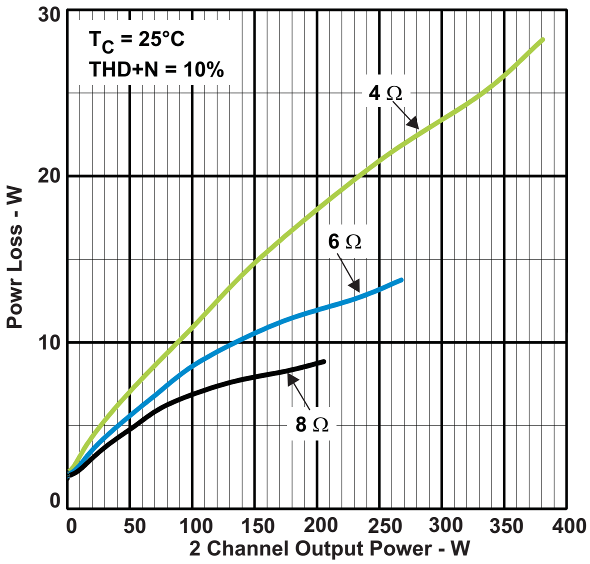


Figure 5.

OUTPUT POWER vs CASE TEMPERATURE

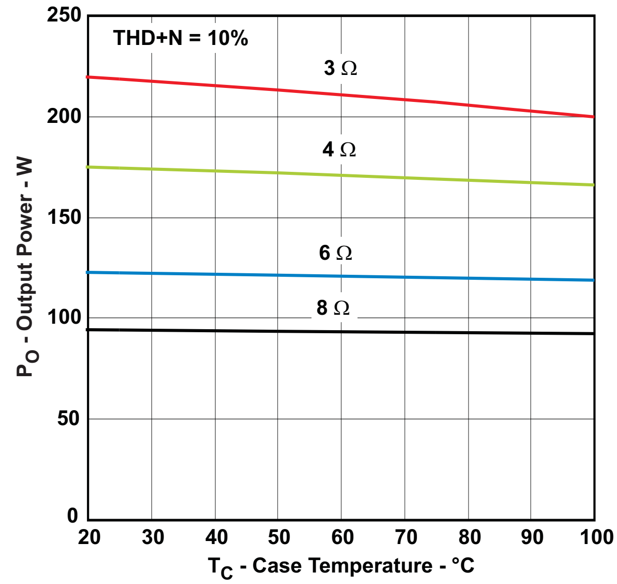


Figure 6.

NOISE AMPLITUDE vs FREQUENCY

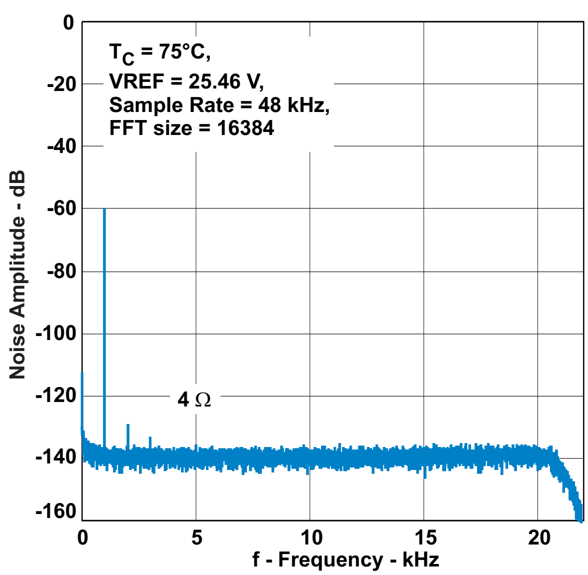


Figure 7.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

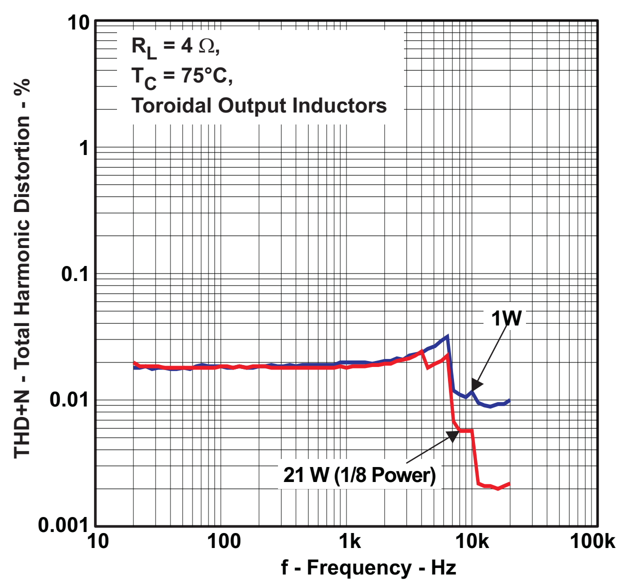


Figure 8.

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

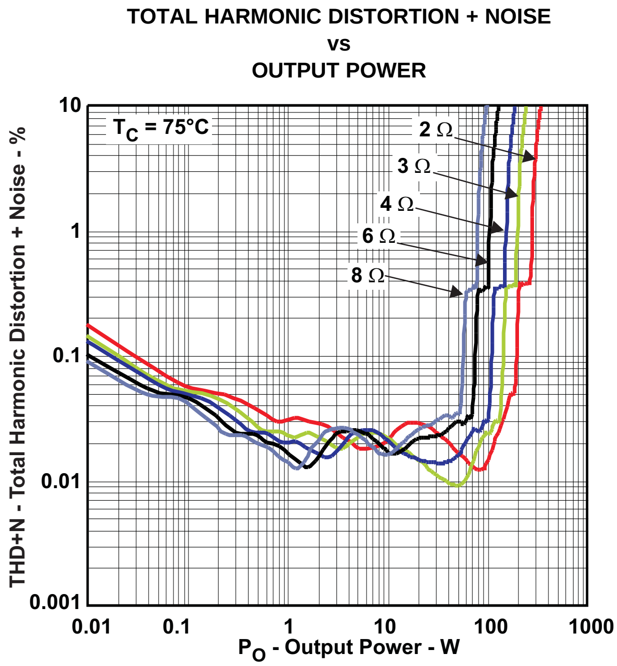


Figure 9.

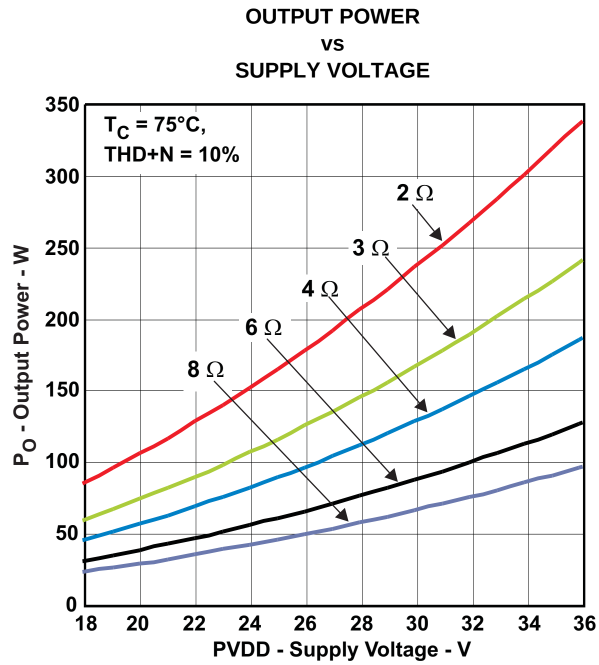


Figure 10.

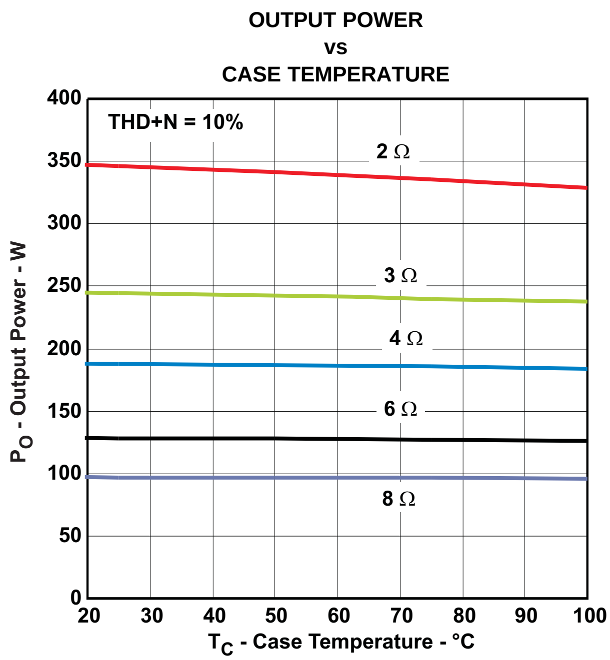


Figure 11.

APPLICATION INFORMATION

PCB MATERIAL RECOMMENDATION

FR-4 Glass Epoxy material with 2 oz. (70µm) is recommended for use with the TAS5613A. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 50V will support more applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

DECOUPLING CAPACITOR RECOMMENDATIONS

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 2µF that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50V is required for use with a 36V power supply.

SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate best practices in the use of the TAS5613A.

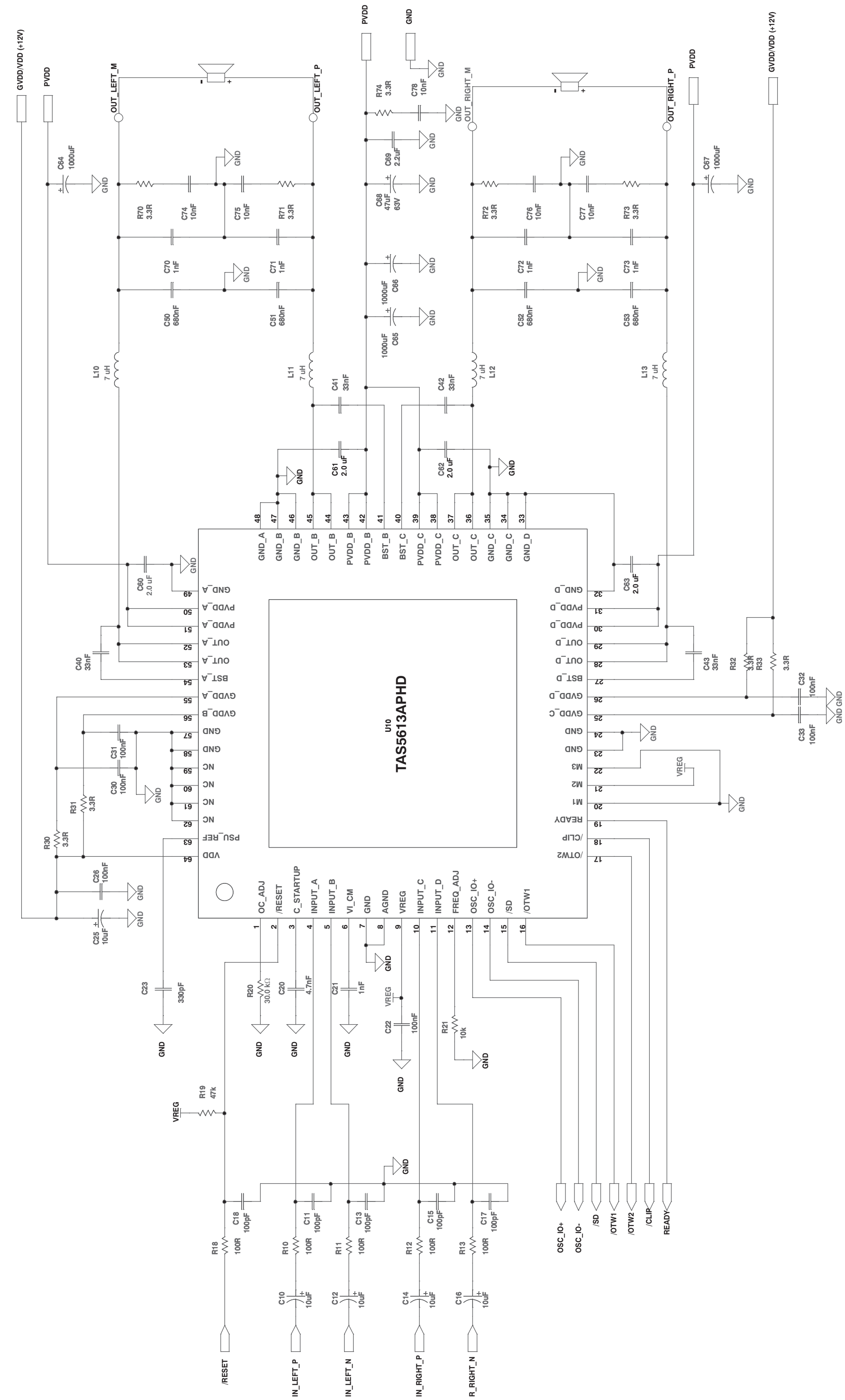


Figure 12. Typical Differential Input BTL Application With BD Modulation Filters

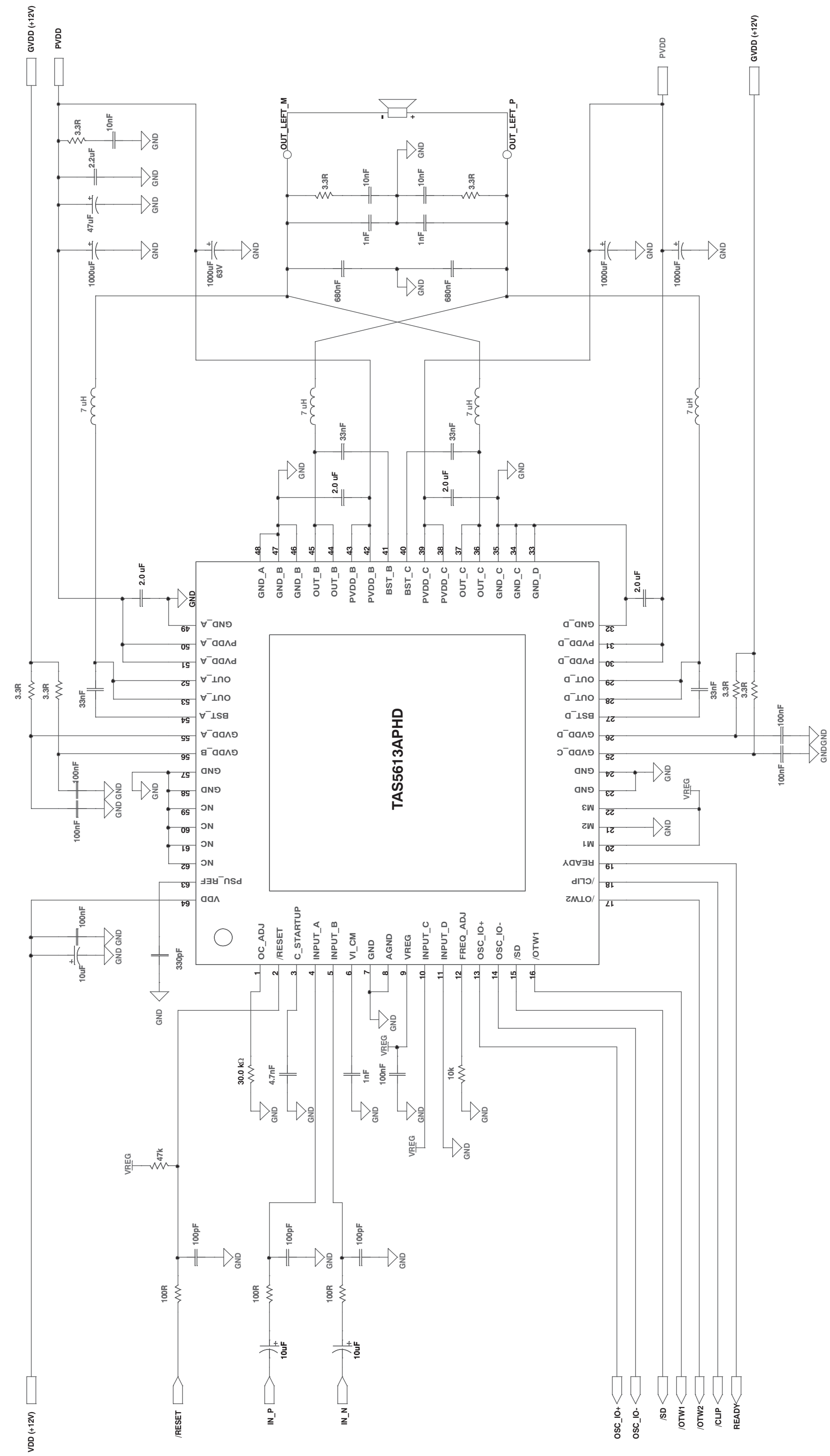


Figure 13. Typical Differential (2N) PBTL Application With BD Modulation Filters

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5613A needs only a 12V supply in addition to the (typical) 36V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Gate drive supply (GVDD_X) is separate for each half bridge for the PHD package and separate per full bridge for the DKD package. Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12V source, separating to GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300kHz to 400kHz, it is recommended to use 33nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2-μF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5613A reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 36V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5613A is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5613A does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5613A does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks.

ERROR REPORTING

The SD, OTW, OTW1 and OTW2 pins are active-low, open-drain outputs. The function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the SD pin going low. Also, OTW and OTW2 go low when the device junction temperature exceeds 125°C, and OTW1 goes low when the junction temperature exceeds 100°C (seeTable 2).

Table 2. Error Reporting

SD	OTW1	OTW2, OTW	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP) Junction temperature higher than 125°C (overtemperature warning)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP). Junction temperature lower than 100°C
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting either RESET low forces the SD signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3V is provided on both SD and OTW outputs. Level compliance for 5V logic can be obtained by adding external pullup resistors to 5 V (see the Electrical Characteristics section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5613A contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5613A responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the SD pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device will function on errors, as shown in Table 3.

Table 3. Device Protection

BTL	MODE	PBTL	MODE	SE	MODE
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
A	A+B	A	A+B+C+D	A	A+B
B		B		B	
C	C+D	C		C	C+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert SD).

PIN-TO-PIN SHORT CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15ms/μF. While the PPSC detection is in progress, SD is kept low, and the device will not react to changes applied to the RESET pins. If no shorts are present the PPSC detection passes, and SD is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

PHD Package

The TAS5613A PHD package option has a three-level temperature-protection system that asserts an active-low warning signal (OTW1) when the device junction temperature exceeds 100°C (typical), (OTW2) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

DKD Package

The TAS5613A DKD package option has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5613A fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the Electrical Characteristics table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high impedance state when asserting the reset input low.

Asserting reset input low removes any fault information to be signalled on the SD output, i.e., SD is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of SD.

SYSTEM DESIGN CONSIDERATION

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

Apply only audio when the state of READY is high that will start and stop the amplifier without having audible artifacts that is heard in the output transducers.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply controlling a low and a high rail.

The device is inverting the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

OSCILLATOR

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

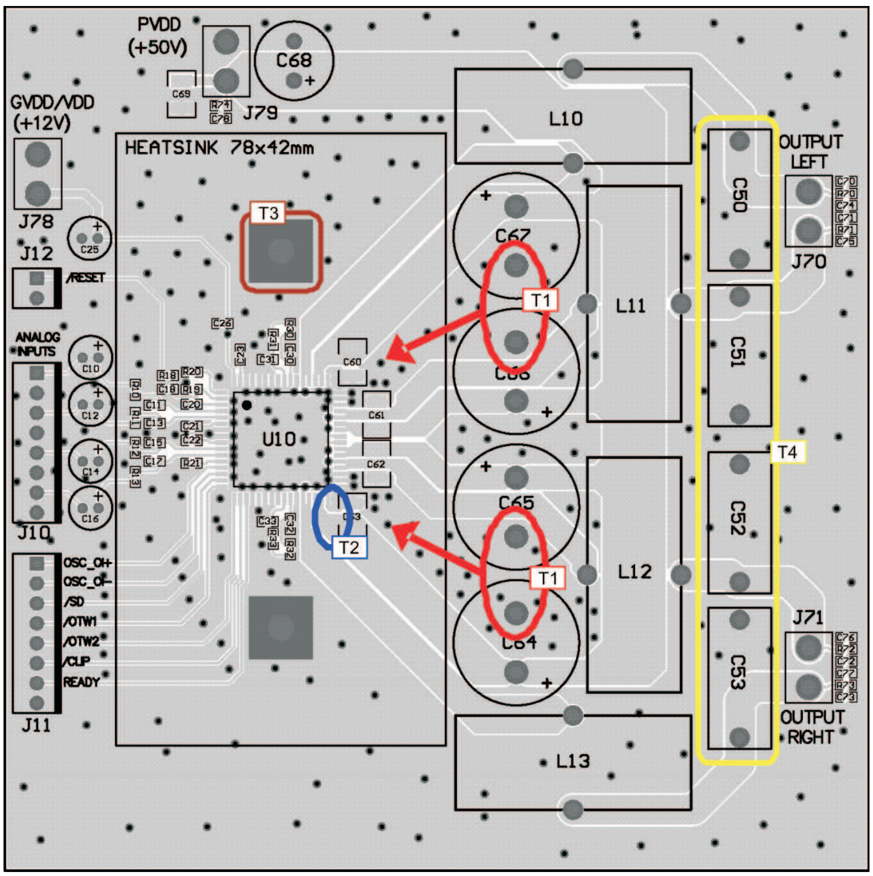
To reduce interference problems while using radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower value switching frequencies together results in the fewest cases of interference throughout the AM band. can be selected by the value of the FREQ_ADJ resistor connected to AGND in master mode.

For slave mode operation, turn of the oscillator by pulling the FREQ_ADJ pin to VREG. This configures the OSC_I/O pins as inputs and needs to be slaved from an external differential clock.

PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high fast switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing the audio input should be kept short and together with the accompanied audio source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce.

Netlist for this printed circuit board is generated from the schematic in Figure 12.



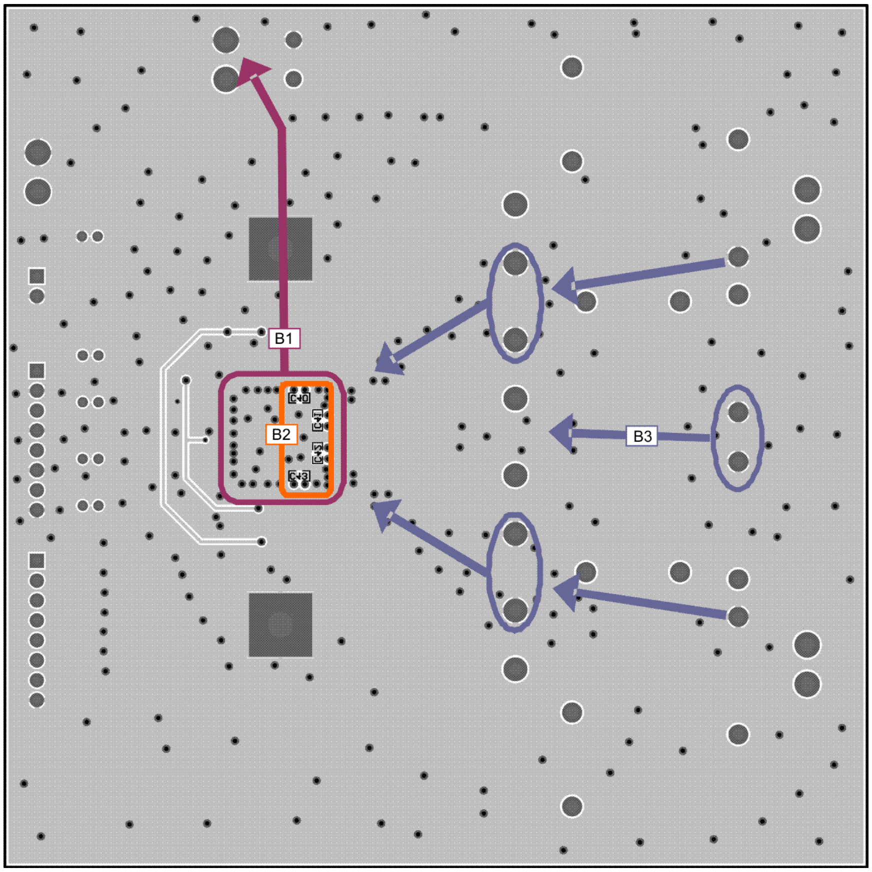
Note T1: PVDD decoupling bulk capacitors C60-C64 should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

Note T3: Heat sink needs to have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range preferable metal film types.

Figure 14. Printed Circuit Board - Top Layer



Note B1: It is important to have a direct low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low impedance X7R ceramic capacitors placed on bottom side providing a short low inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors.

Figure 15. Printed Circuit Board - Bottom Layer

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5613ADKD	ACTIVE	HSSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5613A	Samples
TAS5613ADKDR	ACTIVE	HSSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5613A	Samples
TAS5613APHD	ACTIVE	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5613A	Samples
TAS5613APHDR	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5613A	Samples
TAS5613PHD	NRND	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5613	
TAS5613PHDR	NRND	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5613	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

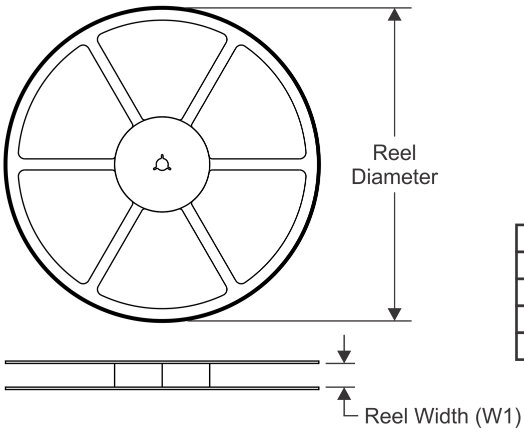
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

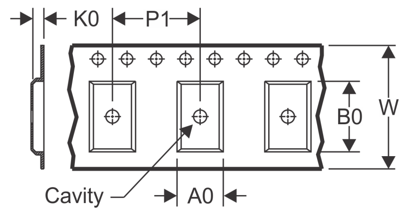
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

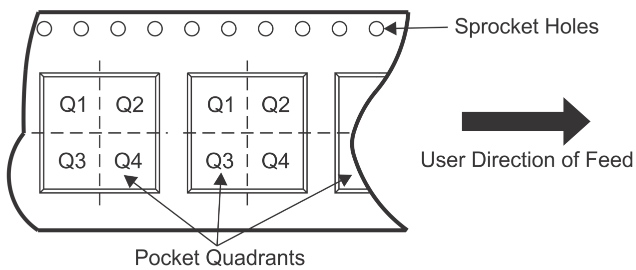


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

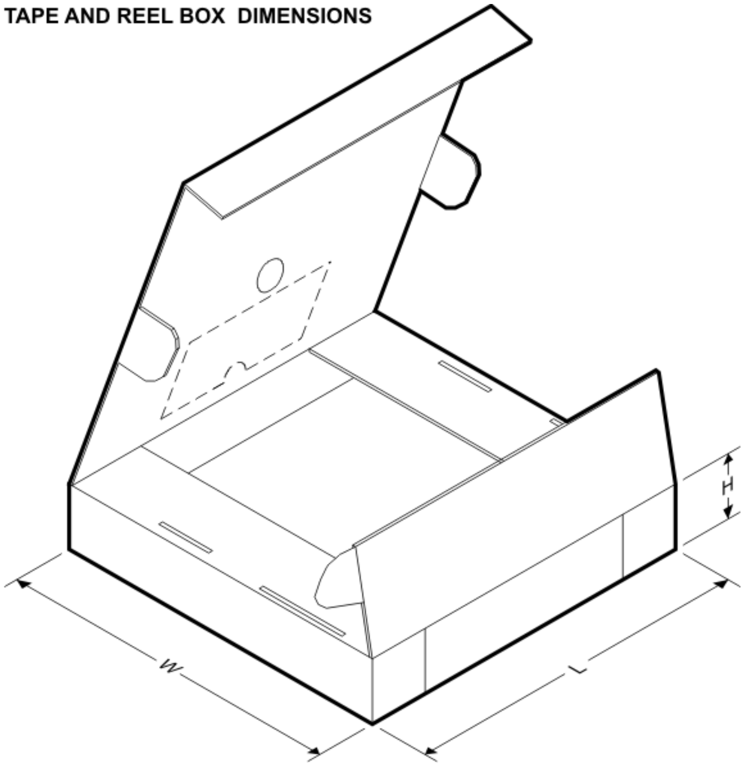
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5613ADKDR	HSSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5613APHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
TAS5613PHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5613ADKDR	HSSOP	DKD	44	500	350.0	350.0	43.0
TAS5613APHDR	HTQFP	PHD	64	1000	350.0	350.0	43.0
TAS5613PHDR	HTQFP	PHD	64	1000	350.0	350.0	43.0

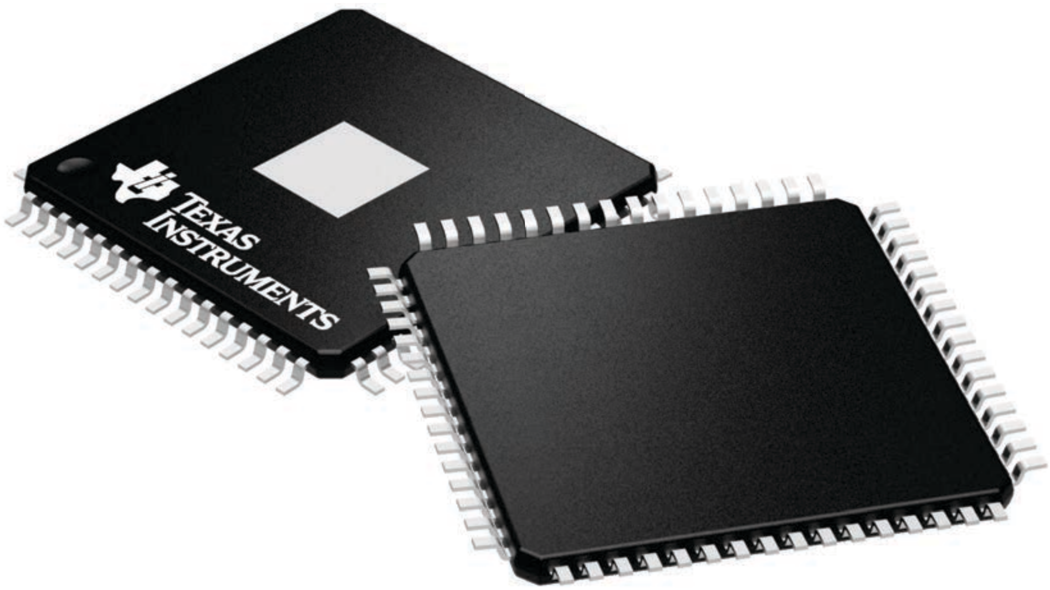
PHD 64

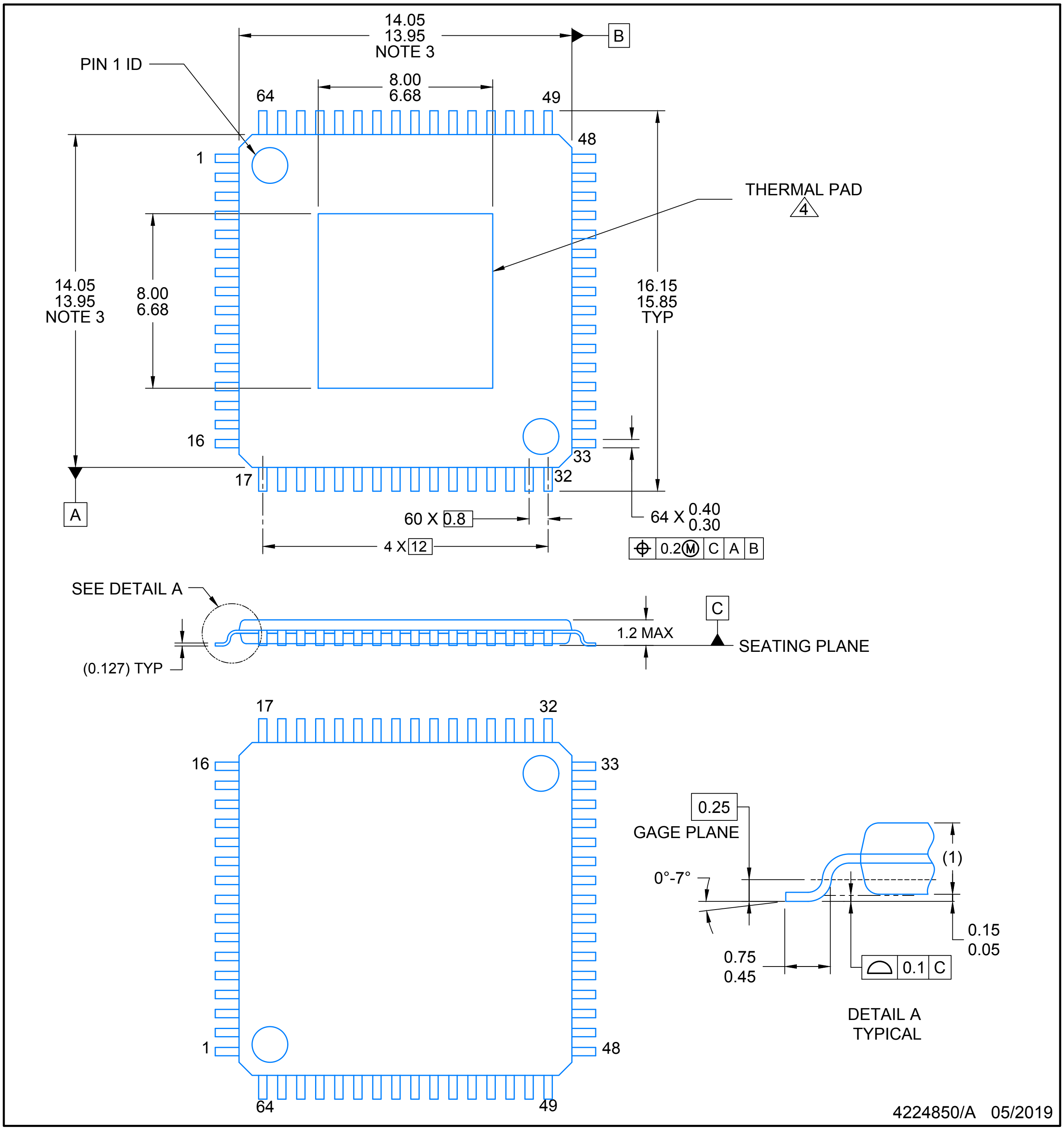
HTQFP - 1.20 mm max height

14 x 14, 0.8 mm pitch

QUAD FLATPACK

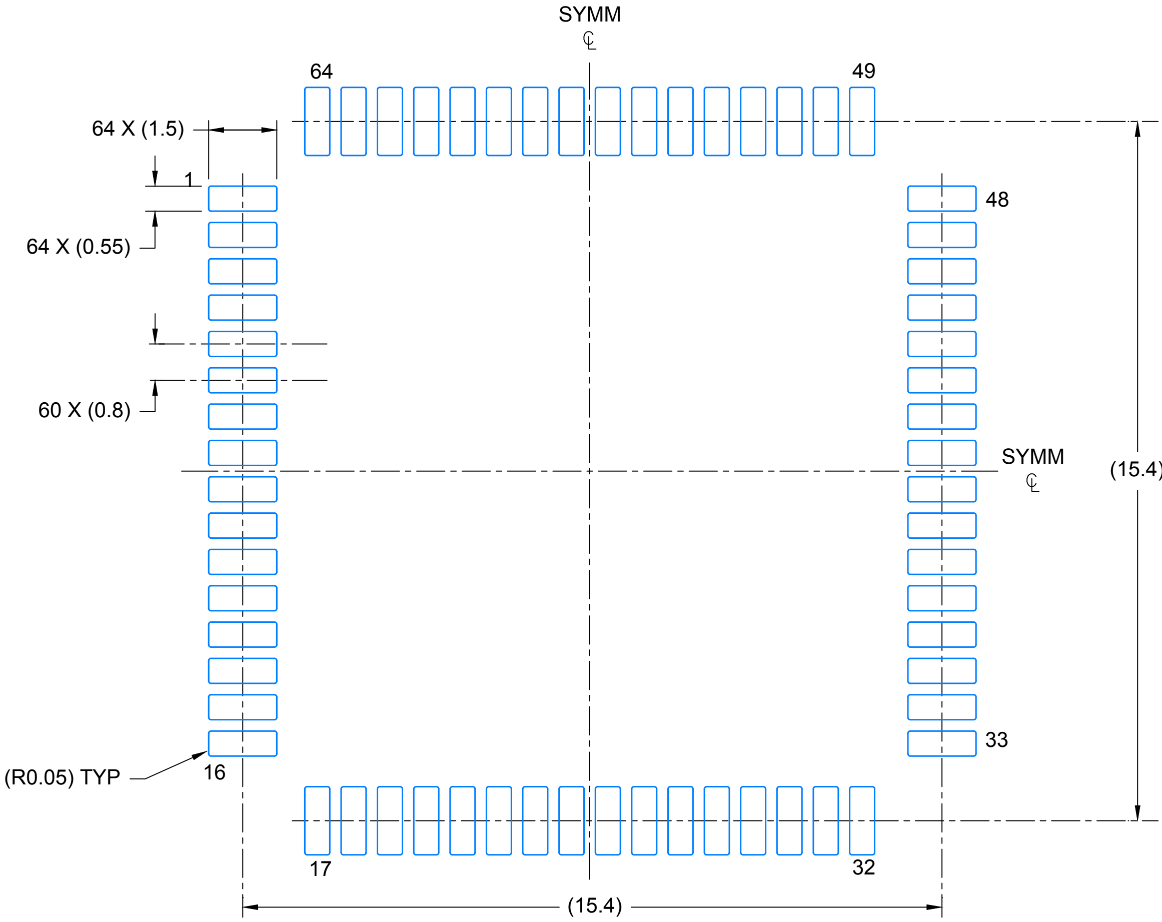
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



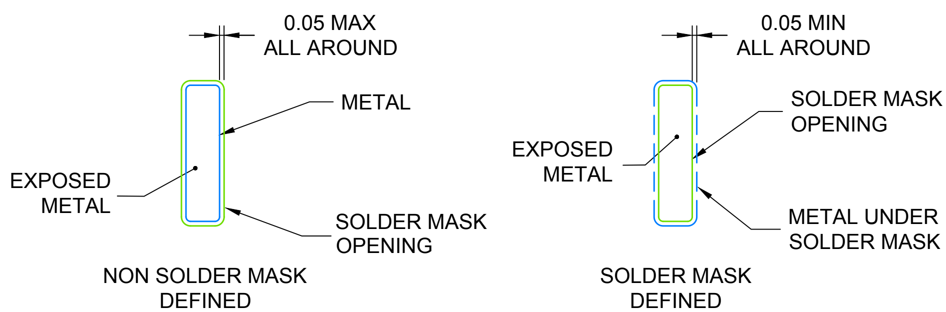


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X

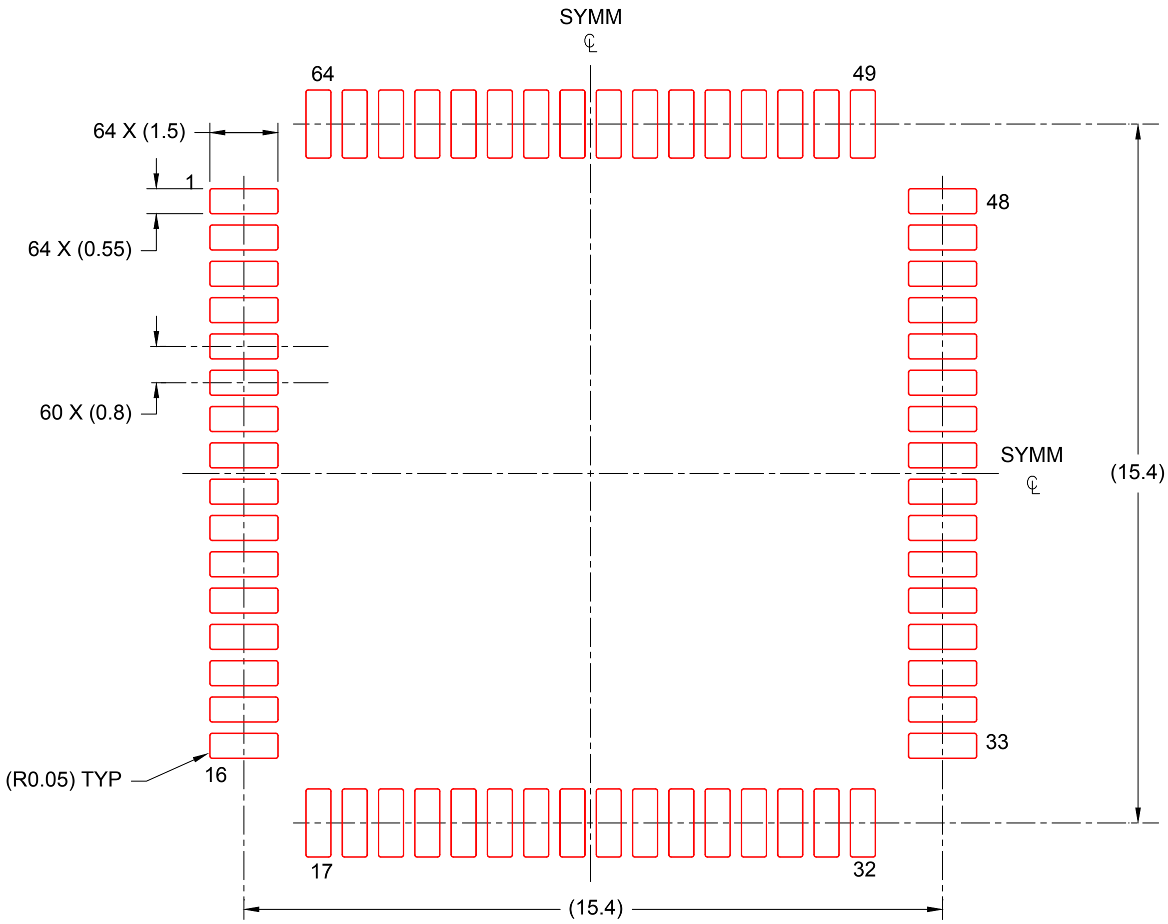


SOLDER MASK DETAILS

4224850/A 05/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
SCALE: 6X

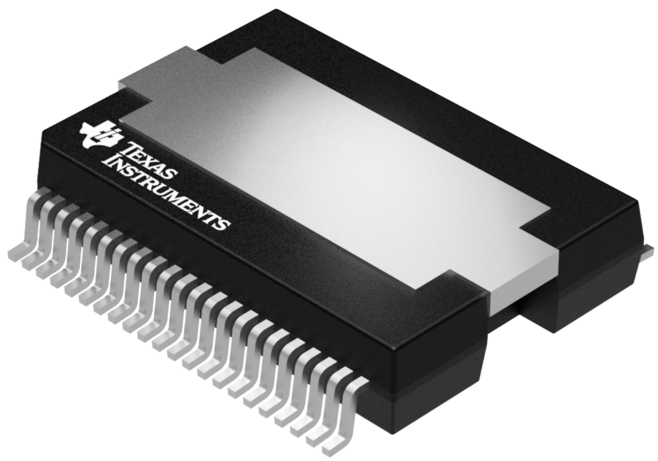
4224850/A 05/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DKD 44 **PowerPAD™ HSSOP - 3.6 mm max height**

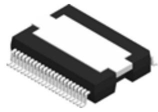
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204421-3/N

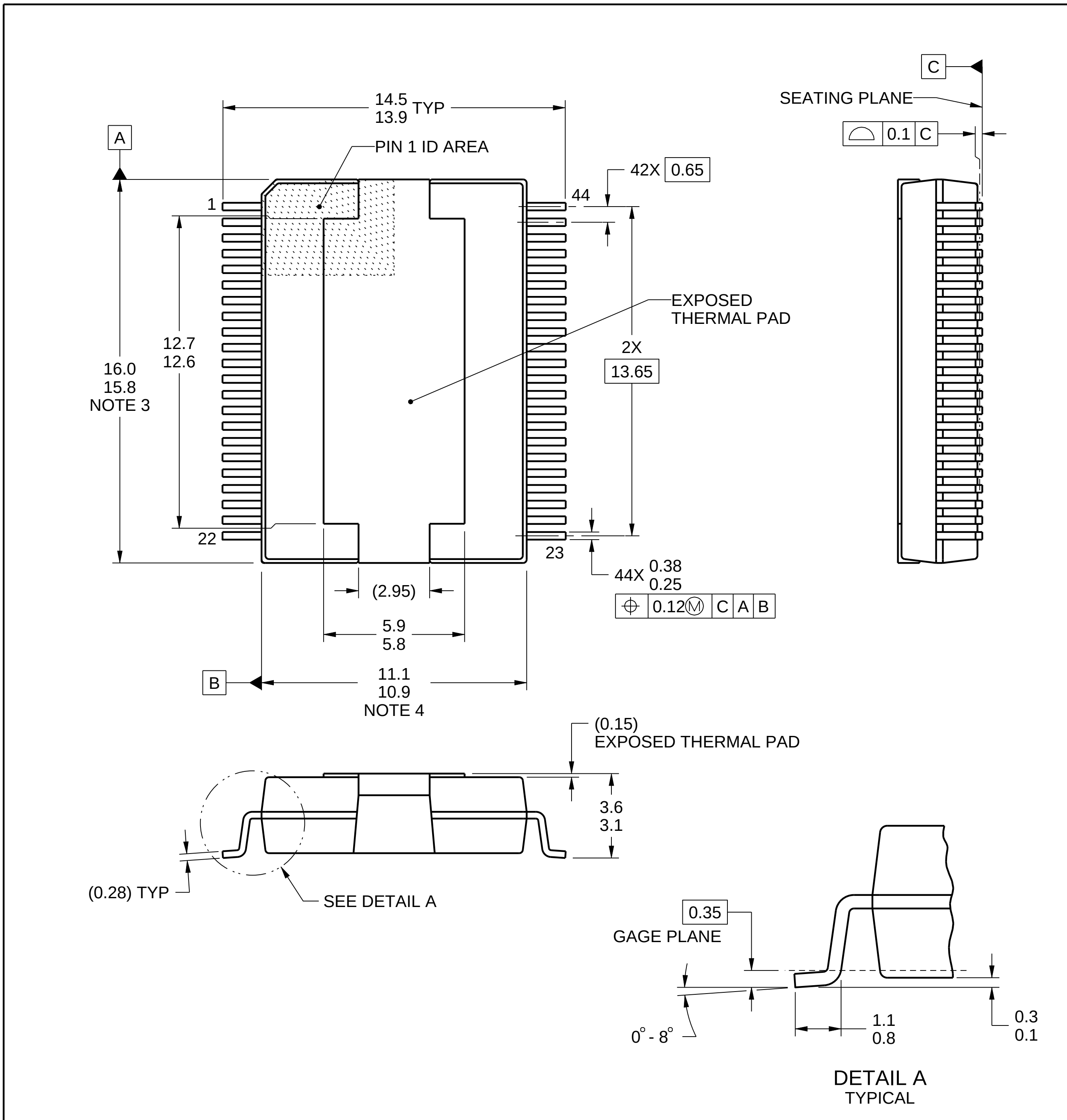
PACKAGE OUTLINE



DKD0044A

PowerPAD™ SSOP - 3.6 mm max height

PLASTIC SMALL OUTLINE

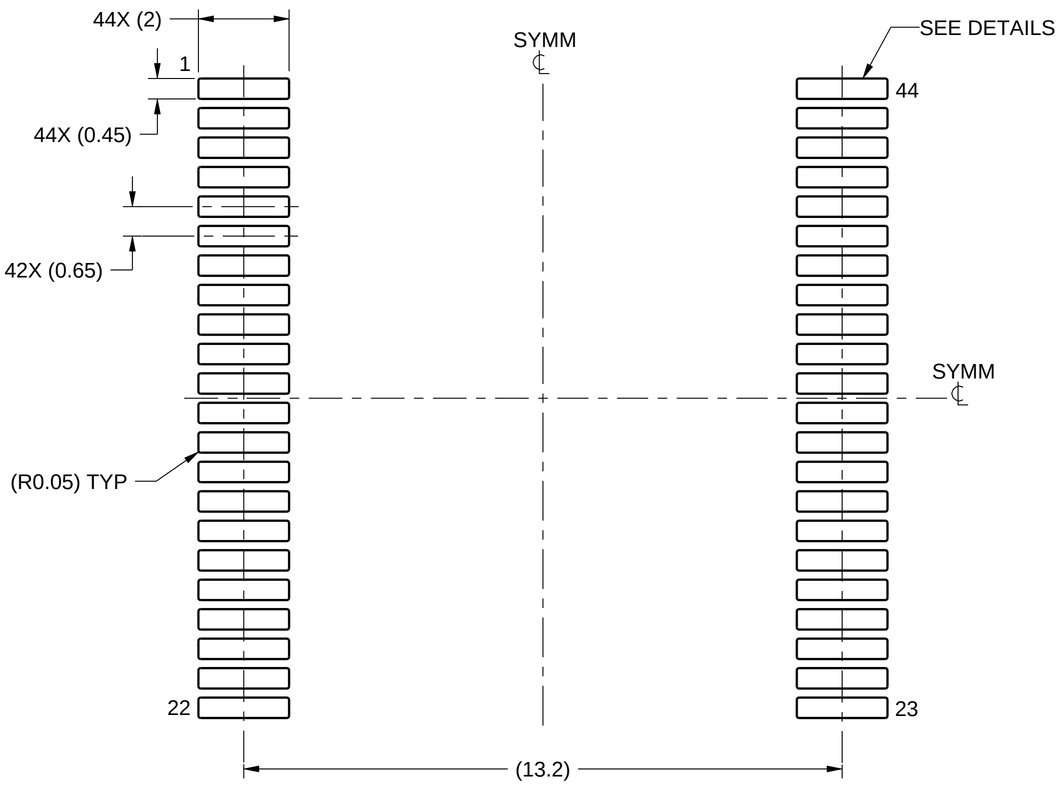


4218846/A 07/2016

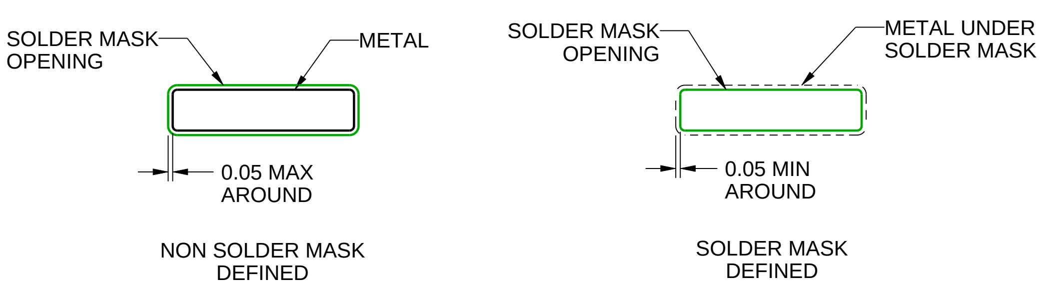
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. The exposed thermal pad is designed to be attached to an external heatsink.



LAND PATTERN EXAMPLE
SCALE:6X

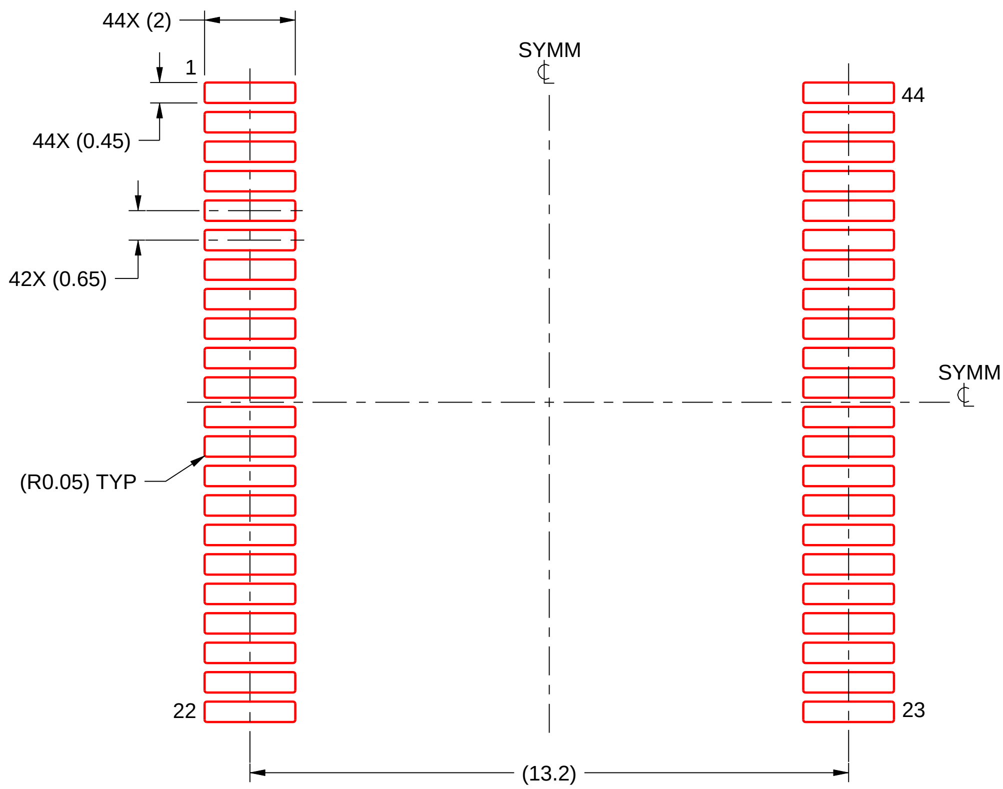


SOLDER MASK DETAILS
NOT TO SCALE

4218846/A 07/2016

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

4218846/A 07/2016

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.