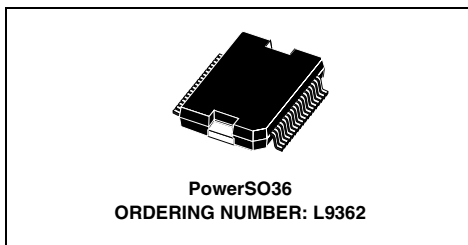


## QUAD LOW SIDE DRIVER

- QUAD LOW-SIDE DRIVER FOR AUTOMOTIVE APPLICATION
- CURRENT FEEDBACK OUTPUT FOR EACH POWER STAGE
- 5V SUPPLY VOLTAGE
- INTERNAL FAILURE DIAGNOSTIC
- OUTPUT VOLTAGE SLOPE CONTROL FOR LOW ELECTRO MAGNETIC EMISSIONS
- INTERNAL SHORT CIRCUIT PROTECTION
- OVERTEMPERATURE PROTECTION AND OVERCURRENT PROTECTION AND DISABLE
- SWITCHING FREQUENCY UP TO 2KHZ
- INTERNAL ZENER CLAMP OF THE OUTPUT VOLTAGE FOR INDUCTIVE LOADS
- PARALLEL INPUT
- SPI FOR DIAGNOSTIC INFORMATION EXCHANGE
- RESET INPUT

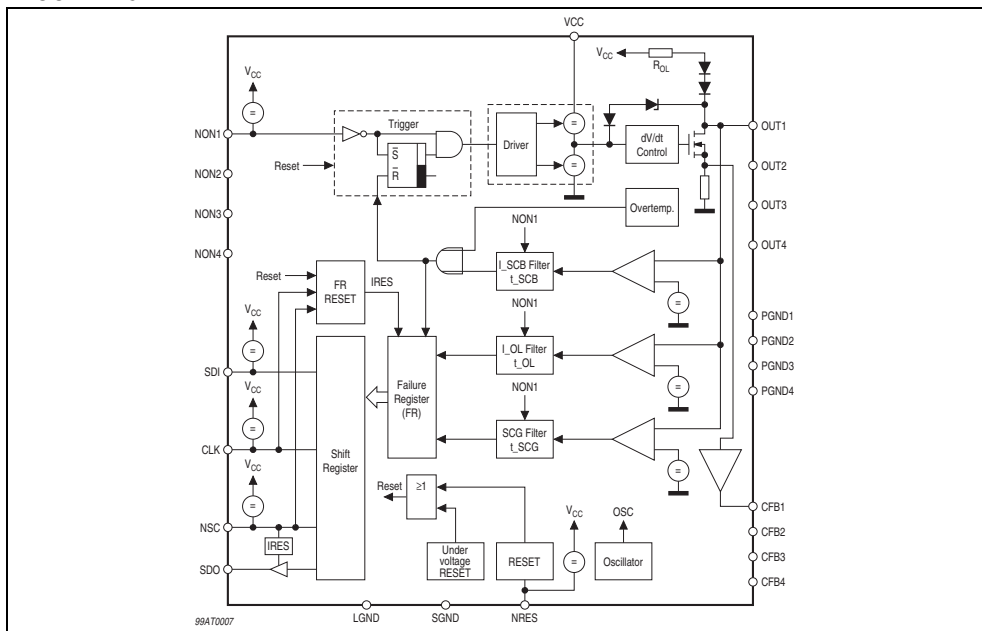


- TYPICAL INTERNAL OSCILLATOR FREQUENCY 325kHz

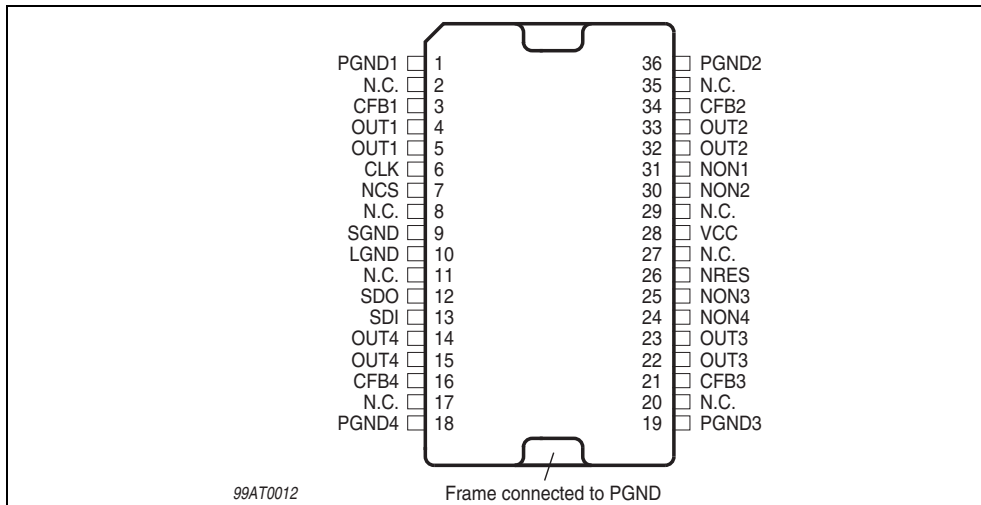
### DESCRIPTION

The Quad Driver is an integrated quad low-side power switch with power limitation, load interrupt and shorted load detection, thermal shutdown, error detection via SPI interface and integrated Z-diodes for output clamping, free running diodes.

### BLOCK DIAGRAM



## PIN CONNECTION



## PIN FUNCTIONS

Pin No.	Pin Name	Pin Description	Notes
1	PGND1	Power Ground	
2	N.C.		
3	CFB1	Output Current feedback	Sinks current proportional to $I_{OUT1}$
4	OUT1	Output Power Switch	
5	OUT1	Output Power Switch	
6	CLK	Input Clock	Digital input, Schmitt trigger, internal Pullup current
7	NCS	inverted Chip Select Input	Digital input, Schmitt trigger, internal Pullup current
8	N.C.		
9	SGND	Signal Ground	
10	LGND	Ground of digital part	
11	N.C.		
12	SDO	Serial Data Output	Digital tristate output
13	SDI	Serial Data Input	Digital input, Schmitt trigger, internal Pullup current
14	OUT4	Output Power Switch	
15	OUT4	Output Power Switch	
16	CFB4	Output Current feedback	Sinks current proportional to $I_{OUT4}$
17	N.C.		
18	PGND4	Power Ground	
19	PGND3	Power Ground	
20	N.C.		
21	CFB3	Output Current feedback	Sinks current proportional to $I_{OUT3}$
22	OUT3	Output Power Switch	
23	OUT3	Output Power Switch	
24	NON4	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current

## PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Description	Notes
25	NON3	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
26	NRES	Inverted Reset Input	Digital input, Schmitt trigger, internal Pullup current
27	N.C.		
28	VCC	5V Supply Voltage Input	
29	N.C.		
30	NON2	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
31	NON1	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
32	OUT2	Output Power Switch	
33	OUT2	Output Power Switch	
34	CFB2	Output Current feedback	Sinks current proportional to $I_{OUT2}$
35	N.C.		
36	PGND2	Power Ground	

## THERMAL DATA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Thermal resistance</b>						
$R_{th\ j-case}$	Thermal resistance junction to case (one powerstage in use)	Die must be soldered on the frame.			4.5	°C/W
$R_{thja}$	Thermal resistance junction-ambient	pad layout		50		°C/W
$R_{thja}$	Thermal resistance junction-ambient	pad layout + 6 cm <sup>2</sup> on board heat sink		35		°C/W
<b>ESD</b>						
ESD	MIL 883C				±2	KV

## ABSOLUTE MAXIMUM RATINGS

For externally applied voltages or currents exceeding these limits damage of the circuit may occur

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Supply Voltages</b>						
$V_{CC}$	Supply voltage		-0.3		7	V
<b>Outputs (Out 1 ... 4)</b>						
$V_{Out}$	Continues output voltage	With no reverse current.	-0.3		45	V
$I_{outc}$	Continues current				3.0	A
$I_{SCBpeak}$	Peak output current		-10		$I_{SCB}$	A
$W_{OFF}$	Clamped energy at the switching OFF	For 2ms, see fig. 8			50	mJ
<b>Inputs (NONx; NCS; CLK; NRES; SDI)</b>						
$V_{IN}$	Input voltage		-0.3		7	V
<b>Outputs (SDO; CFB)</b>						
$V_{OUT}$	Output voltage		-0.3		$V_{CC} + 0.3$	V
<b>Operating junction temperature</b>						
$T_j$	Operating junction temperature		-40		150	°C

Note: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

**ELECTRICAL CHARACTERISTICS**4.5V ≤ V<sub>CC</sub> ≤ 5.5V, -40°C ≤ T<sub>J</sub> ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Supply current</b>						
I <sub>CCRES</sub>	Standby current	Without load. T <sub>J</sub> ≤ 85°C NRES = LOW			1.3	mA
I <sub>CCOPM</sub>	Operating mode	I <sub>OUT 1 ... 4</sub> = 2A		11	17	mA
I <sub>CCLV</sub>	Low voltage supply current	V <sub>CC</sub> < 0,5V			80	µA
<b>Inputs (NONx; NCS; CLK; NRES; SDI)</b>						
V <sub>INL</sub>	Low threshold		-0.3		0.2 • V <sub>CC</sub>	V
V <sub>INH</sub>	High threshold		0.7 • V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>hyst</sub>	Hysteresis		0.85			V
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = V <sub>CC</sub>			10	µA
I <sub>IN</sub>	Input current (NONx, NCS, CLK, SDI)	V <sub>IN</sub> ≤ 0.8 • V <sub>CC</sub>	20		100	µA
I <sub>IN NRES</sub>	Input current NRES		3		20	µA
<b>Serial Data Output</b>						
V <sub>SDOH</sub>	High output level	(I <sub>SDO</sub> = -2mA)	V <sub>CC</sub> - 0.4			V
V <sub>SDDL</sub>	Low output level	(I <sub>SDO</sub> = 3.2mA)			0.4	V
I <sub>SDDL</sub>	Tristate leakage current	(NCS = HIGH; V <sub>SDO</sub> = 0V ... V <sub>CC</sub> )	-10		10	µA
<b>Outputs (Out 1 ... 4)</b>						
I <sub>OUTL1</sub>	Leakage current 1	(NON = HIGH; V <sub>OUT</sub> = 14V; V <sub>CC</sub> = 5V)			10	µA
V <sub>clpa</sub>	Output clamp voltage	V <sub>clpa</sub> (I <sub>OUT</sub> = 0.5A)	45	50	60	V
W <sub>OFF</sub>	Clamped energy at the switching OFF <sup>1)</sup>	For 2ms, see fig. 8			50	mJ
R <sub>DSON</sub>	ON resistance	I <sub>OUT</sub> = 2A; T <sub>J</sub> = 150°C; T <sub>J</sub> = 25°C <sup>2)</sup>		250	500 300	mΩ mΩ
OVR <sub>p1</sub>	Positive output voltage ramp (with inductive load)	V <sub>OUT</sub> = 30% ... 80% of V <sub>BAT</sub> = 16V <sup>3)</sup> V <sub>OUT</sub> = V <sub>BAT</sub> ... 0.9 • V <sub>clp</sub> <sup>3)</sup>	0.3	0.9	1.35	V/µs
OVR <sub>p2</sub>			0.75		2.25	V/µs
OVR <sub>n</sub>	Negative output voltage ramp	80% ... 30% of V <sub>BAT</sub> = 16V with inductive load <sup>3)</sup>	0.3	0.9	1.35	V/µs
t <sub>dON</sub>	Turn ON delay	NON = 50%; V <sub>OUT</sub> = 0.8 • V <sub>BAT</sub>	0	4	10	µs
t <sub>dOFF</sub>	Turn OFF delay	NON = 50%; V <sub>OUT</sub> = 0.3 • V <sub>BAT</sub>	0	4	10	µs

Note 1: Typical loads for the zener clamping and the output voltage ramps are:

- a) 10Ω, 16mH at all outputs or
- b) 25Ω, 160mH

Note 2: At 150°C guaranteed by design and electrical characterisation

Note 3: Tested with resistive load of R<sub>load</sub> = 50Ω

**ELECTRICAL CHARACTERISTICS** (continued)4.5V ≤ V<sub>CC</sub> ≤ 5.5V, -40°C ≤ T<sub>J</sub> ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Powerstage protection</b>						
I <sub>SCB</sub>	Short current detection and switch off threshold	With filter-time t <sub>SCB</sub> .	3.0		5.0	A
t <sub>SCB</sub>	Short circuit switch off delay time			3	30	μs
V <sub>ocmin</sub>	V <sub>CC</sub> undervoltage		3.0		4.0	V
<b>Current feedback</b>						
T <sub>Ratio 1</sub>	I <sub>CFB</sub> / I <sub>OUT</sub> for I <sub>OUT</sub> =0.4...2A <sup>4)</sup>	V <sub>CFB</sub> ≥ 1.8V	1.45	1.65	2	mA/A
T <sub>MPS1</sub> <sup>6)</sup>	<sup>5)</sup>	Temperature stability for 0.4A to < 2.0A, related to 25°C		±3	±6	%
CURS1	for I <sub>OUT</sub> = 0.4A to 2A <sup>5)</sup>	Current stability Δgain/Gain at 2A  T <sub>J</sub> = -40°C T <sub>J</sub> = +25°C T <sub>J</sub> = +125°C	-12 -6 -5		17 10 5	% % %
CURlin1 <sup>6)</sup> CURlin2	for I <sub>OUT</sub> = 0.4A to 1.0A <sup>4)</sup> for I <sub>OUT</sub> = 1.0A to 2.0A <sup>4)</sup>	Linearity Error (within the calibration points at 0.5A, 1A, 2A)		±0.2	±1 ±0.7	% %

Note 4: At 150°C guaranteed by design and electrical characterisation

Note 5: Guaranteed by design and electrical characterisation

Note 6: Values for T<sub>MPS1</sub>, CURlin1 and CURlin2 are typical values from testing results

<b>Diagnostic</b>						
V <sub>REF1</sub>	Short to GND threshold voltage	for I <sub>OUT</sub> ≤ 2A	0.390 •V <sub>CC</sub>		0.435 •V <sub>CC</sub>	V
t <sub>SCG</sub>	Short to GND filter time		140		250	μs
I <sub>OL</sub>	Open load threshold current		10		55	mA
t <sub>OL</sub>	Open load filter time		140		265	μs
R <sub>OL</sub>	Pullup resistor at OUT1, OUT2, OUT3 and OUT4 for OL detection		2.0		8.0	kΩ
T <sub>OFF</sub>	Temperature detection threshold <sup>7)</sup>		155	170	190	°C

Note 7: Guaranteed by measurement and correlation

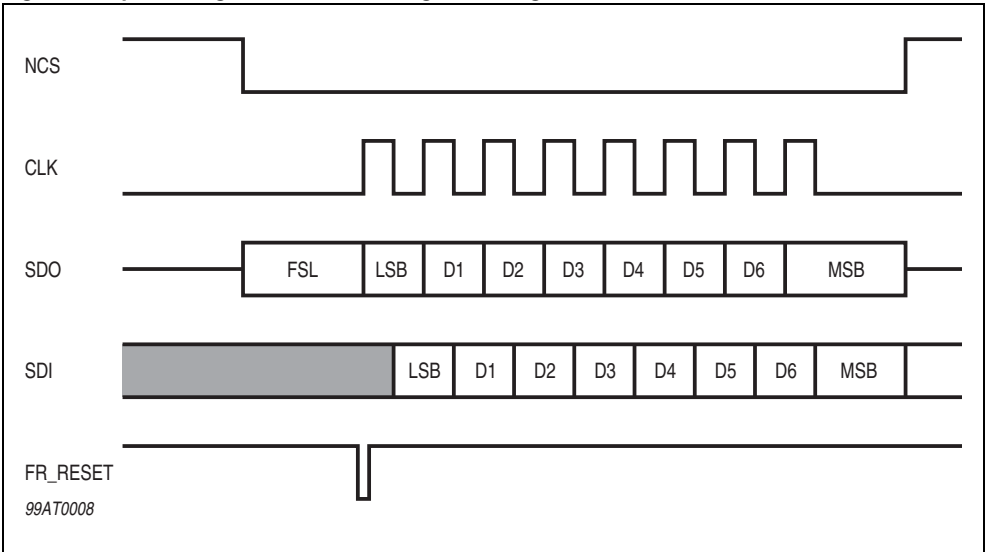
**ELECTRICAL CHARACTERISTICS** (continued)4.5V ≤ V<sub>CC</sub> ≤ 5.5V, -40°C ≤ T<sub>J</sub> ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Serial diagnostic link (external Load capacitor at SDO = 100pF)</b>						
f <sub>clk</sub>	Clock frequency	50% duty cycle.	0		3	MHz
t <sub>clh</sub>	Minimum time CLK = HIGH		100			ns
t <sub>cll</sub>	Minimum time CLK = LOW		100			ns
t <sub>pcl</sub>	Propagation delay	CLK to data at SDO valid.			100	ns
t <sub>csdv</sub>	NCS = LOW	To data at SDO valid.			100	ns
t <sub>sc</sub>	CLK low before NCS low	Setup time CLK to NCS change H/L.	100			ns
t <sub>hc</sub>	CLK change L/H after NCS = LOW		100			ns
t <sub>sd</sub>	SDI input setup time	CLK change H/L after SDI data valid.	20			ns
t <sub>hd</sub>	SDI input hold time	SDI data hold after CLK change H/L.	20			ns
t <sub>sc</sub>	CLK low before NCS high		150			ns
t <sub>hc</sub>	CLK high after NCS high		150			ns
t <sub>pdz</sub>	NCS L/H to output data float				100	ns
t <sub>fNCS</sub>	NCS filter-time	Pulses ≤ t <sub>fNCS</sub> will be ignored.	10		40	ns

Note: 8. Input Pin Capacitance of SDI, CLK, NCS, NON1, NON2, NON3, NON4 6pF typical; Output Pin Capacitance of SDO 12pF typical

1.0 Diagnostic Register and SPI timing

Figure 1. Impulse diagram to read the Diagnostic Register



Note: FR\_RESET means Reset failure storage (internal signal)

Figure 2. Diagnostic Failure Register Structure

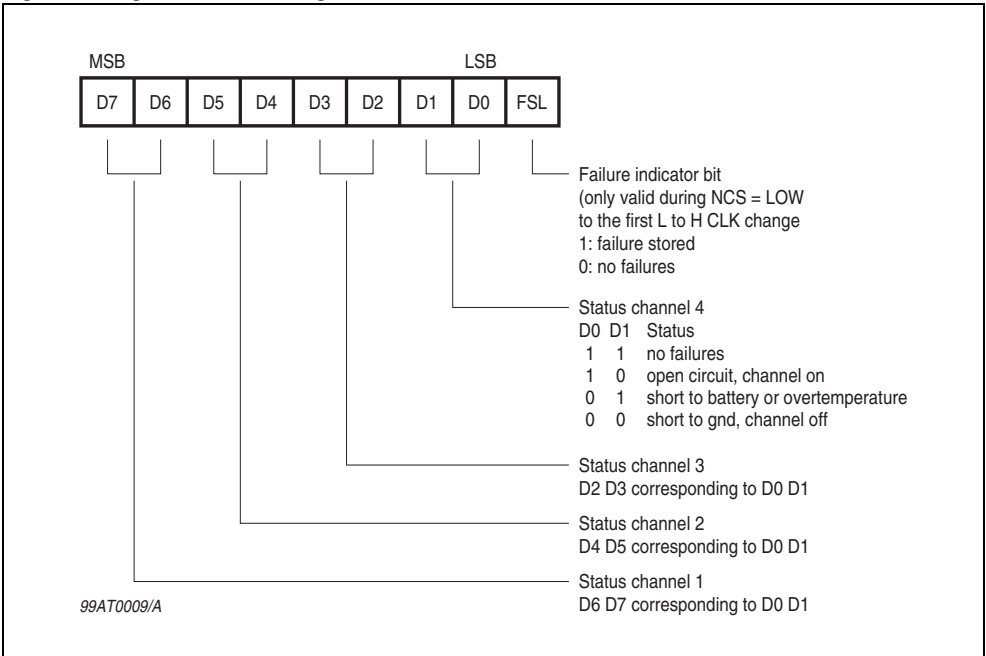


Figure 3. Timing of the Serial Interface

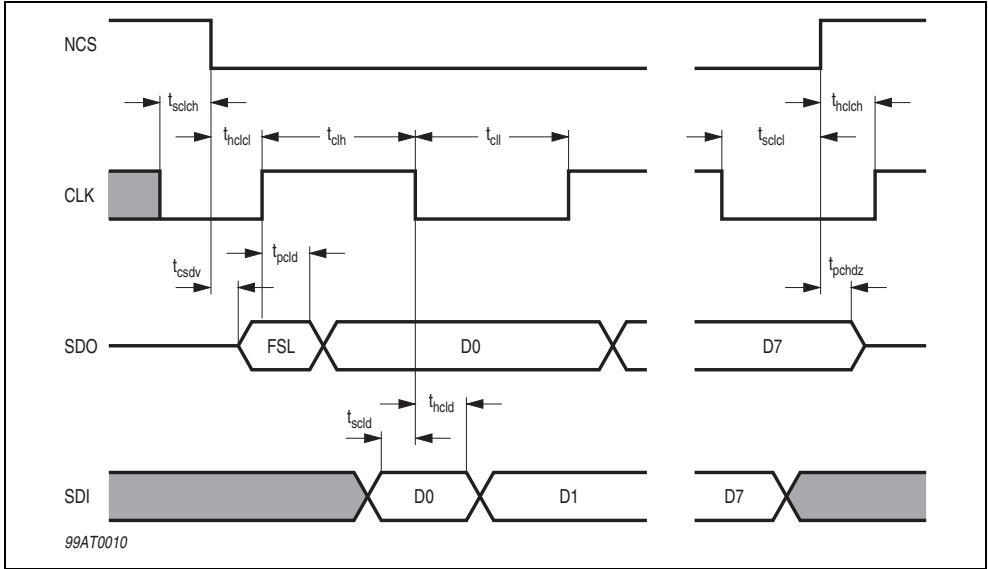


Figure 4. Short-Circuit to GND Failure (SCG-Failure) Detection

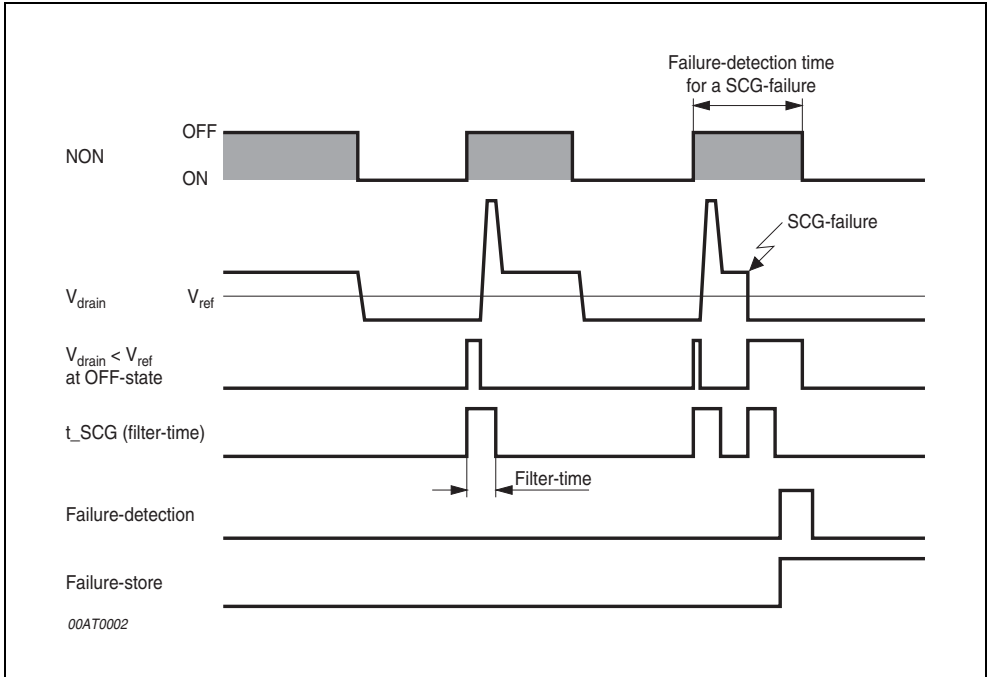




Figure 5. Open-Load Failure (OL-Failure) Detection

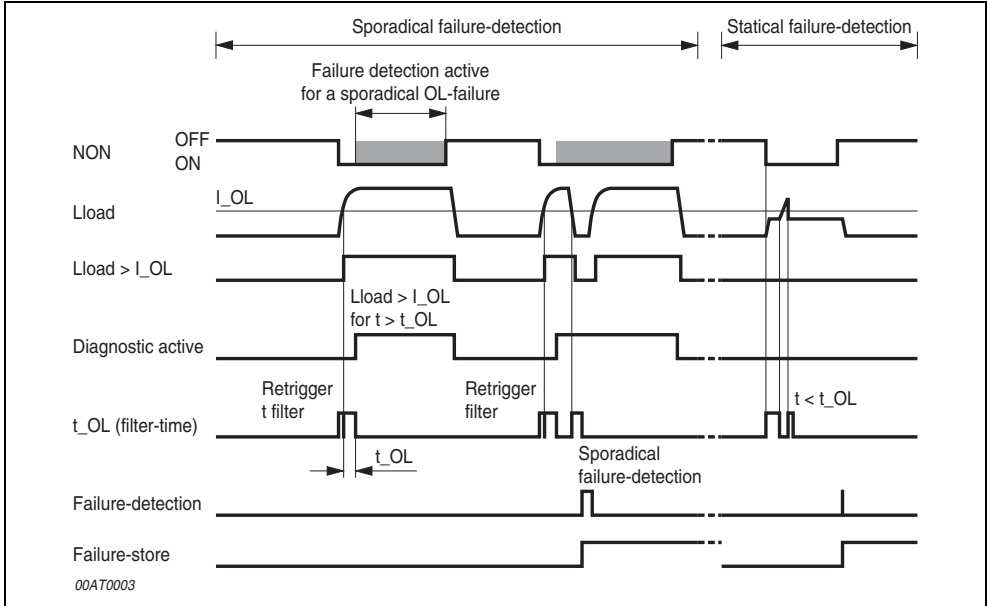


Figure 6. Different cases for an Open Load failure detection (case 1 to 10)

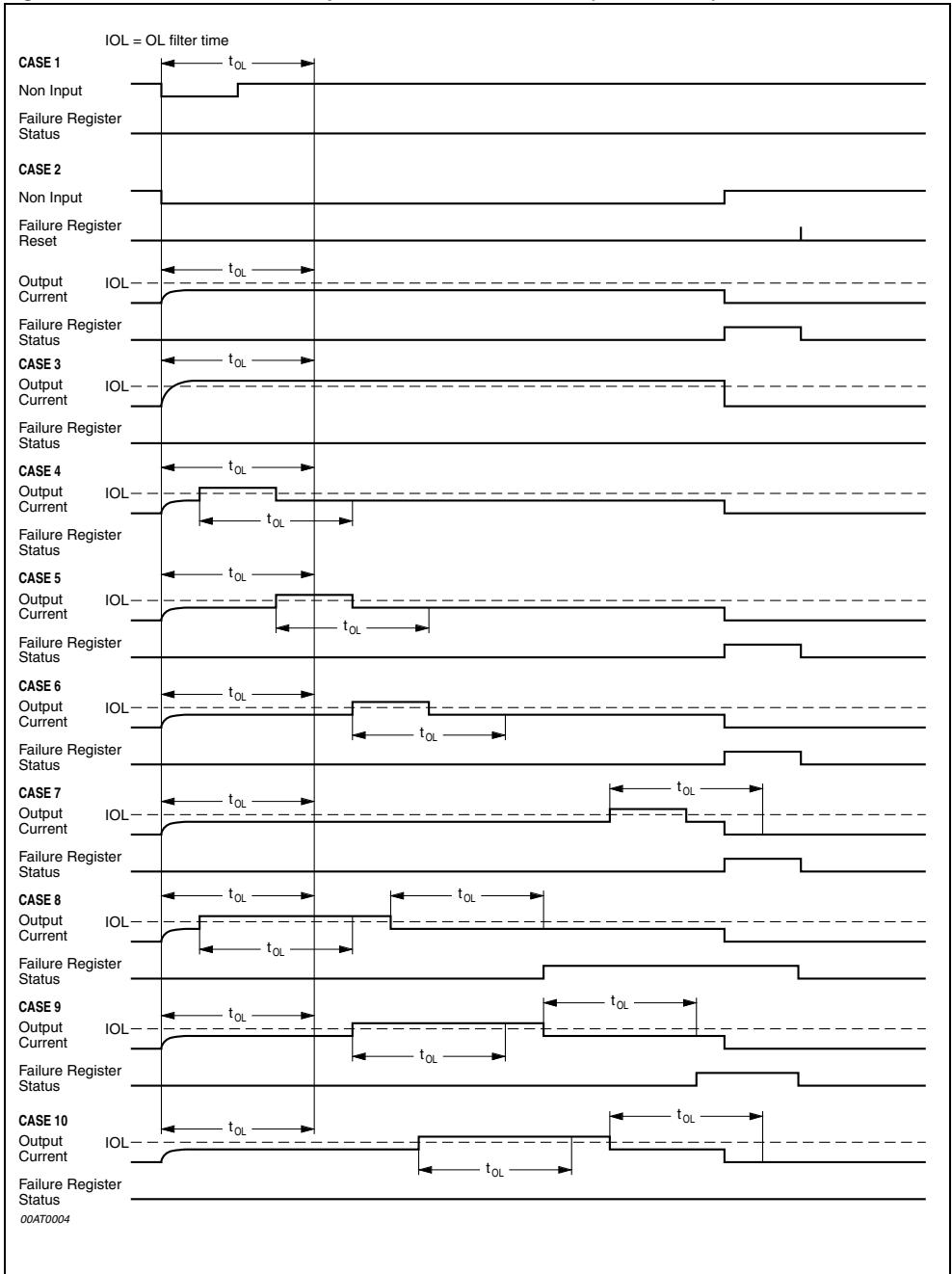


Figure 7. Different cases for an Open Load failure detection (case 11 to 20)

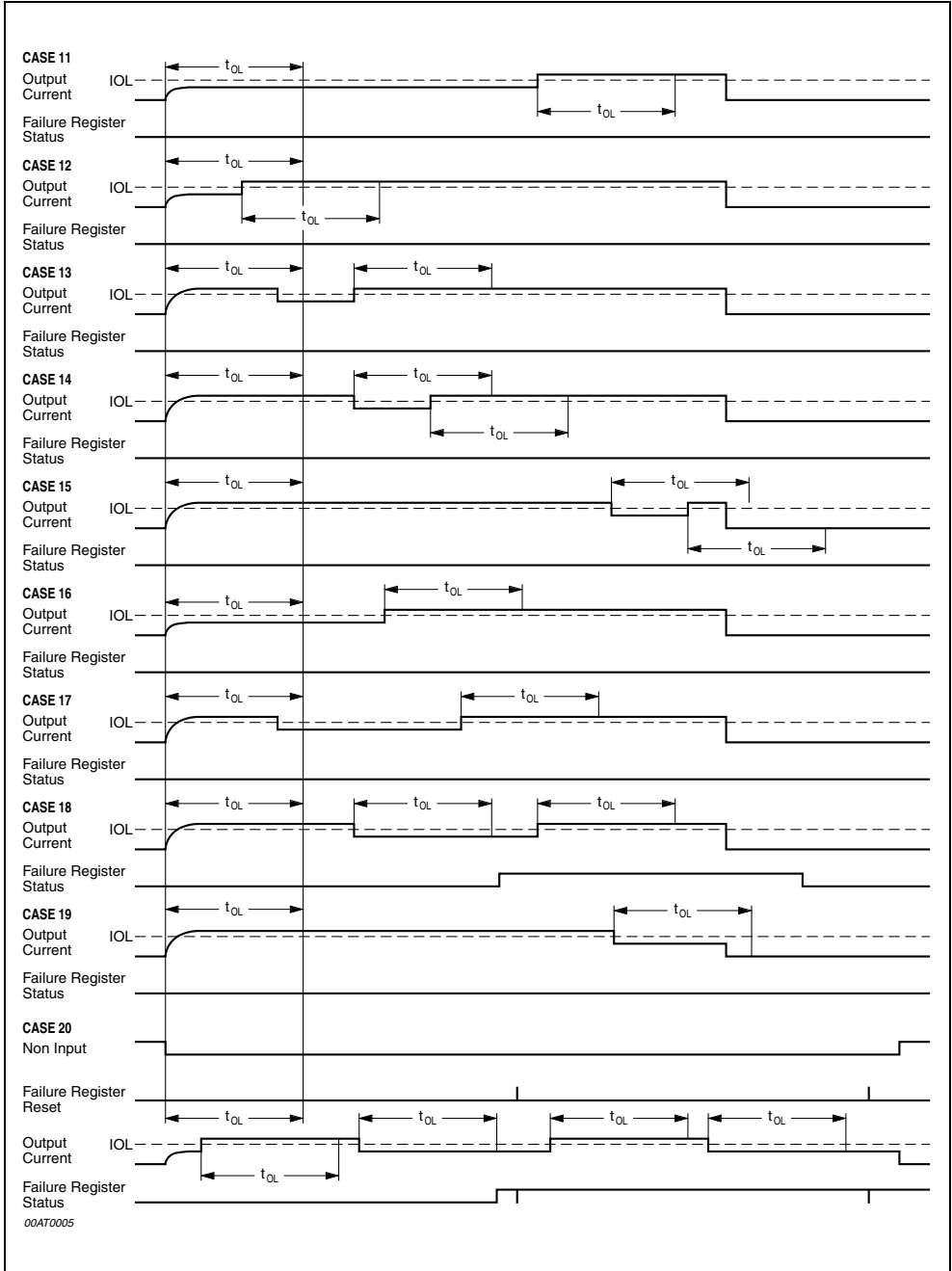


Figure 8. Max Clamp Energy Specification

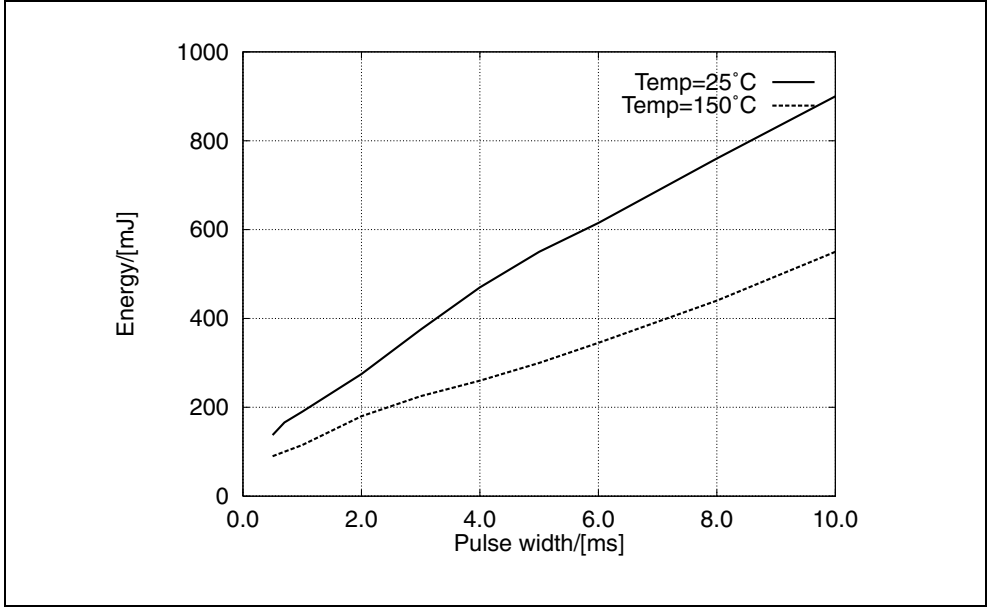


Figure 9. Ratio of Current Feedback output versus output current

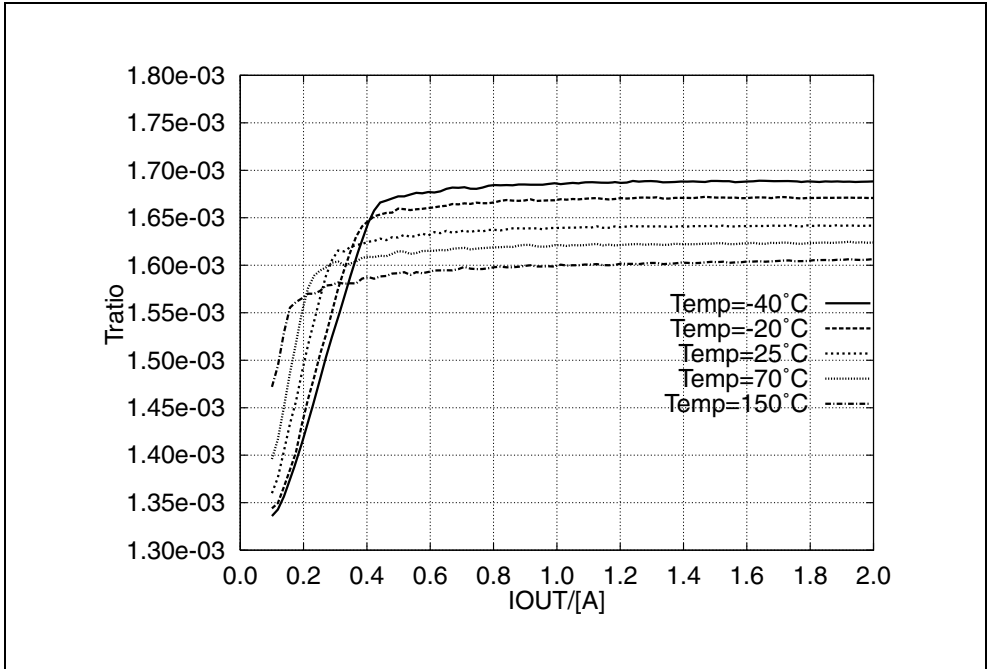
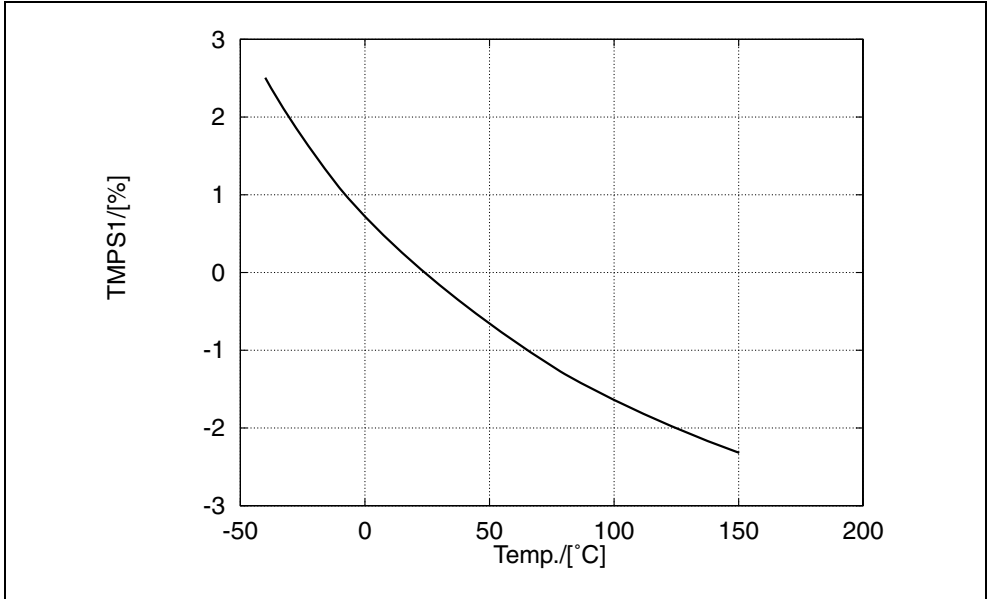


Figure 10. TMPS1 vs. Temperature ( $4.5V \leq V_{CC} \leq 5.5V$ ;  $0.5A \leq I_{out1...4} \leq 3A$ ).



## FUNCTIONAL DESCRIPTION

### Introduction

The Quad Low Side Driver UF07 is built up of four identical channels (Low Side Drivers), controlled by four CMOS input stages. Each Channel is protected against short to  $V_{Bat}$  and by a zener clamp against overvoltage. A diagnostic logic recognizes four failure types at the output stage: overcurrent, short to GND, open-load and overtemperature.

The failures are stored individually for each channel in one byte which can be read out via a serial interface (SPI).

Each channel has a current feedback output which sinks a current proportional to the load current of the Low Side Switch.

### Output Stage Control

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

### Power Transistors

Each of the four output stages has its own zener clamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. Output voltage ramp occurring when the output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase the current capability. In this case, the associated inputs, outputs and current feedback outputs should be connected together.

### Diagnostics

Following failures at the output stage are recognized:

Short circuit to  $V_{Bat}$  or overtemp.....= SCB (Highest priority)

Short circuit to GND.....=SCG

Open Load.....= OL (Lowest Priority)

### Short-Circuit and Overtemperature Protection (SCB)

If the output current increases above the short current limit for a longer time than  $t_{SCB}$  or if the temperature increases above  $T_{OFF}$ , then the power transistor is immediately switched off. It remains switched off until the control signal at the NON-Input is switched off and on again. This filter time has the purpose to suppress wrong detection on short spikes.

All four outputs have an independent overtemperature detection and shutdown. This measurement is active while the powerstage is switched on.

The Short circuit detection and the overtemperature detection are using the same bit in the Diagnostic (one for each channel).

A **SCG** failure will be recognized, when the drain voltage of the output stage is lower as the “Short Cut to Ground threshold voltage”, while the output stage is switched off (see Fig. 4). The SCG failure is filtered with a digital filter ( $t_{SCG}$ ) to suppress the storage of a failure at small SCG spikes, which are typical during the transition of the power output. This filter is triggered by the NON input and the (analog) SCG detection.

If the current through the output stage is lower than the IOL-reference, then an **OL** failure will be recognized after a filter time. This measurement is active while the powerstage is switched on.

The Open Load failure detection has 2 different modes, the statical failure detection and the sporadic failure detection. One main difference is, that a statical failure is transferred to the Failure register with the next rising edge of NON, whereas a sporadic failure is transferred immediately to the Failure register (see fig. 5, 6 and 7). In both failure modes the OL detection is filtered ( $t_{OL}=t_{OL}$ ) and is using together with the SCG detection the same digital filter for suppression of spikes.

The failures are stored regarding to their priority (see above). A failure with a higher priority overwrites an eventually already detected failure with a lower priority.

### Diagnostic interface

The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the H/L change at the NCS pin the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is tristate when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of the CLK pin and new SDI data will be latched on every falling edge into the shift register. With the first positive pulse of the CLK the contents of the failure register is copied to the SPI shift register and a internal reset (FR\_RESET) is generated. This internal reset clears the failure register and thus the failure register is capable of detecting failures also during the SPI read cycle. There is no bus collision at a small spike at the NCS. The CLK has to be LOW, while the NCS signal is changing.

### Current feedback

Each channel has a current feedback output which sinks a current proportional to the load current of the Low Side Switch. Using this output servo loop applications can be realized by applying a PWM signal to the NON input. A typical diagram of the Current Feedback output at different temperatures is shown in figure 9.

## Reset

There are two different reset functions realized:

### Undervoltage reset

As long as the voltage of  $V_{CC}$  is lower than  $V_{CCmin}$ , the powerstages are switched off, the failure register is reset and the SDO output remains tristate.

### External reset

As long as the NRES pin is low following circuits are reset:

Powerstages

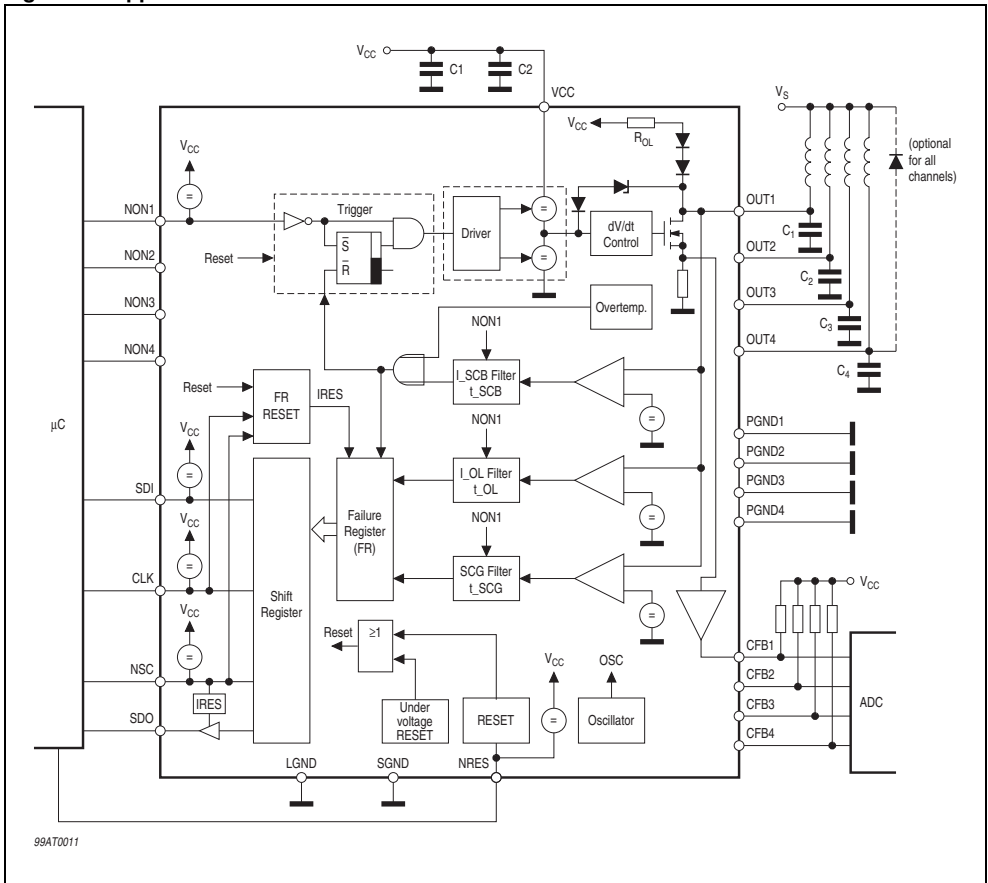
Failure register

and the SDO output is tristate.

## Undervoltage protection

At  $V_{CC}$  below  $V_{CCmin}$  the device remains switched off even if there is a voltage ramp at the OUT pin.

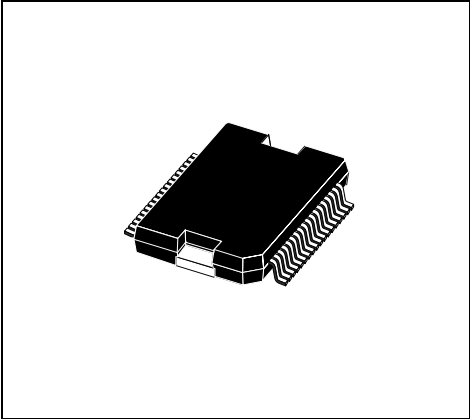
**Figure 11. Application Circuit**



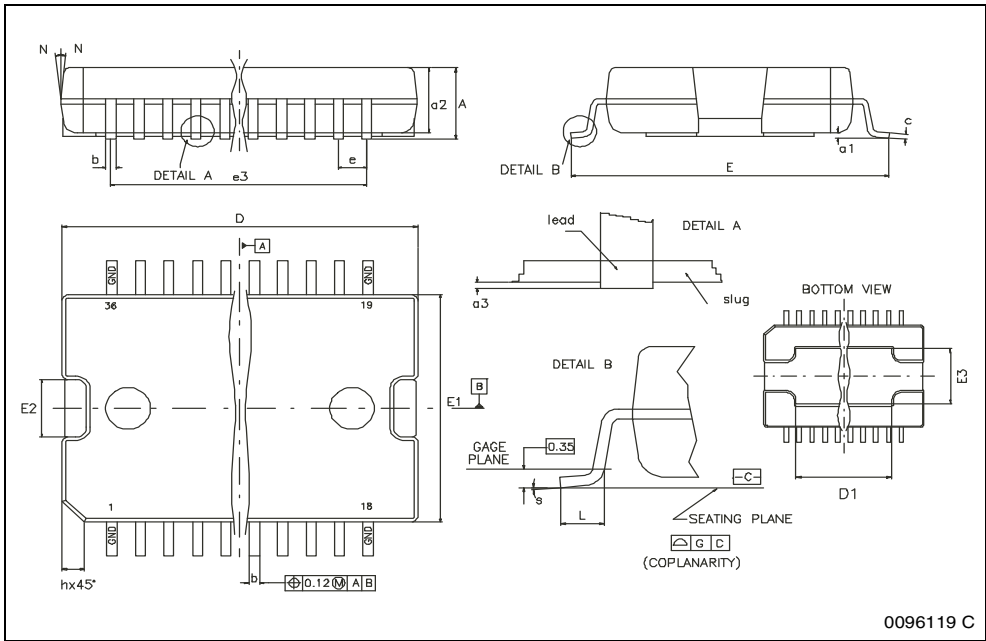
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: "D and E1" do not include mold flash or protrusions.  
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions are "a3", "E" and "G".

## OUTLINE AND MECHANICAL DATA



## PowerSO-36



0096119 C





**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[L9362](#) [L9362013TR](#)