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NC7NZ14 TinyLogic[®] UHS Inverter with Schmitt Trigger Input

Features

- Ultra-High Speed: t_{PD} 3.7 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving US8 Surface Mount Package

Description

The NC7NZ14 is a single inverter with Schmitt trigger input from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a very broad $V_{\rm CC}$ operating range. The device is specified to operate over the 1.65 V to 5.5 V $V_{\rm CC}$ range. The inputs and outputs are high-impedance when $V_{\rm CC}$ is 0 V. Inputs tolerate voltages up to 7 V independent of $V_{\rm CC}$ operating voltage.

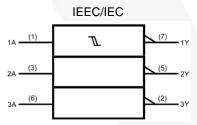


Figure 1. Logic Symbol

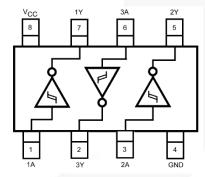


Figure 2. Connection Diagram (Top View)

Ordering Information

Part Number	Operating Temperature	Top Mark	Package	Packing Method
NC7NZ14K8X	40 to 1959C	NZ14	8-Lead, US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 Units on Tape & Reel
NC7NZ14L8X	-40 to +85°C	P6	8-Lead MicroPak™, 1.6 mm Wide	5000 Units on Tape & Reel

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Pin Configurations

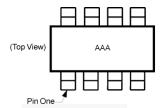


Figure 3. US8

Notes:

- 1. AAA represents product code top mark (see ordering table).
- 2. Orientation of top mark determines pin one location. Reading the top product code mark left to right, pin one is the lower left pin.

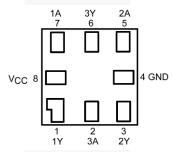


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # US8	Pin # MicroPak™	Name	Description
1	7	1A	Input
2	6	3Y	Output
3	5	2A	Input
4	4	GND	Ground
5	3	2Y	Output
6	2	3A	Input
7	1	1Y	Output
8	8	V _{cc}	Supply Voltage

Function Table

Y = /A

Inputs	Output
Α	Y
L	Н
Н	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage		-0.5	7.0	V
V _{OUT}	DC Output Voltage		-0.5	7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < -0.5 V		-50	mA
	V _{OUT} < -0.5 V		-50	m Λ	
I _{OK}	DC Output Diode Current	$V_{OUT} > 6.0 \text{ V}, V_{CC} = GND$		+20	mA
I _{OUT}	DC Output Current			±50	mA
I _{CC} / I _{GND}	DC V _{CC} or Ground Current		P	±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under E	Bias		+150	°C
TL	Junction Lead Temperature (S	Soldering, 10 Seconds)	1	+260	°C
P _D	Power Dissipation at +85°C		1	250	mW
Human Body Model, JEDEC:JESD		ESD22-A114		4000	\/
ESD	Charge Device Model, JEDEC:JESD22-C101			2000	V

Recommended Operating Conditions⁽³⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
V	Supply Voltage Operating		1.65	5.50	V	
V_{CC}	Supply Voltage Data Retention		1.5	5.5	V	
V_{IN}	Input Voltage		0	5.5	V	
V _{OUT}	Output Voltage		0	V _{CC}	V	
T _A	Operating Temperature		-40	+85	°C	
0	Thermal Resistance	US8	/	250	90044	
$\theta_{\sf JA}$	Thermal Resistance	Micropak™		400	°C/W	

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

0	Danamatan.	V 00	0	7	Γ _A =+25°	С	T _A =-40 to +85°C		1111
Symbol	Parameter	V _{CC} (V)	Conditions	Min.	Тур.	Max.	Min.	Max.	Units
		1.65		0.70	1.10	1.50	0.70	1.50	
		2.30		1.00	1.40	1.80	1.00	1.80	
V_{P}	V _P Positive Threshold Voltage	3.00		1.30	1.75	2.20	1.30	2.20	
	Voltage	4.50		1.90	2.45	3.10	1.90	3.10	
		5.50	1	2.20	2.90	3.60	2.20	3.60	
		1.65		0.25	0.55	0.90	0.25	0.90	
		2.30		0.40	0.75	1.15	0.40	1.15	
V_N	Negative Threshold Voltage	3.00		0.60	1.00	1.50	0.60	1.50	V
	Voltage	4.50		1.00	1.43	2.00	1.00	2.00	
		5.50		1.20	1.70	2.30	1.20	2.30	
		1.65		0.15	0.54	1.00	0.15	1.00	
		2.30		0.25	0.65	1.10	0.25	1.10	
V_{H}	Hysteresis Voltage	3.00		0.40	0.77	1.20	0.40	1.20	V
		4.50		0.60	1.01	1.50	0.60	1.50	_
	7.1	5.50		0.70	1.18	1.70	0.70	1.70	
		1.65		1.55	1.65		1.55	A	
	7	2.30	V _{IN} =V _{IL} ,	2.20	0 2.30	2.20			
		3.00	I _{OH} =-100 μA	2.90	3.00		2.90		
		4.50		4.40	4.50		4.4		
V_{OH}	HIGH Level Output	1.65	I _{OH} =-4 mA	1.29	1.52		1.29		
	Voltage	2.30	I _{OH} =-8 mA	1.90	2.15		1.90		
		3.00	I _{OH} =-16 mA	2.40	2.80		2.40		
		3.00	I _{OH} =-24 mA	2.30	2.68		2.30		
		4.50	I _{OH} =-32 mA	3.80	4.20		3.80		
		1.65			0.00	0.10	1	0.10	
		2.30	V _{IN} =V _{IH} ,		0.00	0.10	ái –	0.10	
		3.00	I _{OL} =100 μA		0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
V_{OL}	LOW Level Output	1.65	I _{OL} =4 mA		0.08	0.24		0.24	V
92 (00)	Voltage	2.30	I _{OL} =8 mA		0.10	0.30		0.30	
		3.00	I _{OL} =16 mA		0.15	0.40		0.40	1
		3.00	I _{OL} =24 mA		0.22	0.55		0.55	1
		4.50	I _{OL} =32 mA		0.22	0.55	75	0.55	1
I _{IN}	Input Leakage Current	0 to 5.5	V _{IN} =5.5 V, GND			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5 V			1		10	μA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5 V, GND			1.0		10	μA

AC Electrical Characteristics

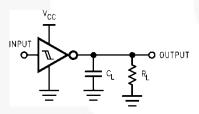
Symbol	Parameter	V _{cc} (V) Condition		1	A=+25°	°C	T _A =-46 +85°		Units	Figure
				Min.	Тур.	Max.	Min.	Max.		
		1.80 ± 0.15		2.0	7.6	12.5	2.0	13.0		
		2.50 ± 0.20	C _L =15 pF,	1.0	5.0	9.0	1.0	9.5	ns	Figure 5 Figure 6 Figure 5
	Branagation Dalay	3.30 ± 0.30	R _L =1 MΩ	1.0	3.7	6.3	1.0	6.5		
t _{PLH} , t _{PHL}	Propagation Delay	5.00 ± 0.50		0.5	3.1	5.2	0.5	5.5		
		3.30 ± 0.30	C _L =50 pF,	1.5	4.4	7.2	1.5	7.5		
		5.00 ± 0.50	$R_L=500 \Omega$	0.8	3.7	5.9	0.8	6.2		Figure 6
C _{IN}	Input Capacitance	0.00			2.5				pF	
6	Power Dissipation	3.30			9		·		n.E	Figure 7
CPD	Capacitance ⁽⁴⁾ 5.00				11				pF	Figure 7

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static).

Dynamic Switching Characteristics

	Cumbal	Davamatar	Conditions	V	T _A =25°c	l lmi4	
	Symbol	Parameter	Conditions	V _{cc}	Тур.	Unit	
Ī	V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C -50 pE V -5 0 V V -0 V	5.0	0.8	V	
Ī	V _{OLV}	Quiet Output Dynamic Valley Vol	$C_L=50 \text{ pF}, V_{IH}=5.0 \text{ V}, V_{IL}=0 \text{ V}$	5.0	-0.8	V	



Note:

 C_L includes load and stray capacitance; Input PRR=1.0 MHz; t_W=500 ns

Figure 5. AC Test Circuit

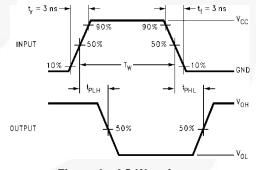
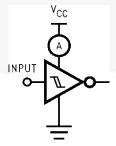


Figure 6. AC Waveforms

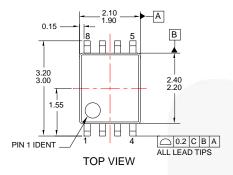


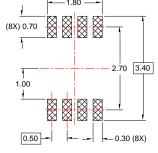
Note:

6. Input=AC Waveform; t_r=t_f=1.8 ns; PRR=10 MHz; Duty Cycle =50%.

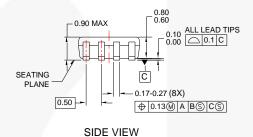
Figure 7. I_{CCD} Test Circuit

Physical Dimensions



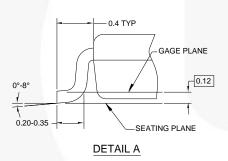


RECOMMENDED LAND PATTERN



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.
- E. FILE DRAWING NAME: MKT-MAB08Arev4



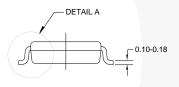


Figure 8. 8-Lead US8, JEDEC MO-187, Variation CA, 3.1 mm Wide

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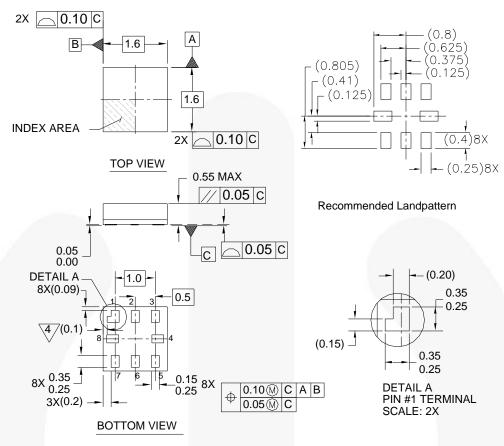
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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/US8_Pack_TNR.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
K8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

- 1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994
- 4/PIN 1 FLAG, END OF PACKAGE OFFSET
- 5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 9. 8-Lead, MicroPak™, 1.0 mm Wide

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Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.			
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