24-Bit Σ-Δ ADC with Low Noise PGA

AD1555/AD1556

FEATURES

AD1555
- Fourth Order Σ-Δ Modulator
- Large Dynamic Range
  - 116 dB Min, 120 dB Typical @ 1 ms
  - 117 dB Typical @ 0.5 ms
- Low Input Noise: 80 nV rms @ 4 ms with Gain of 34,128
- Low Distortion: –111 dB Max, –120 dB Typical
- Low Intermodulation: 122 dB
- Sampling Rate at 256 kSPS
- Very High Jitter Tolerance
- No External Antialias Filter Required
- Programmable Gain Front End
- Input Range: ±2.25 V
- Robust Inputs
- Gain Settings: 1, 2.5, 8.5, 34, 128
- Common-Mode Rejection (DC to 1 kHz)
  - 93 dB Min, 101 dB Typical @ Gain of 1
- 77 mW Typical Low Power Dissipation
- Standby Modes

AD1556
- FIR Digital Filter/Decimator
- Serial or Parallel Selection of Configuration
- Output Word Rates: 250 SPS to 16 kSPS
- 6.2 mW Typ Low Power Dissipation
- 70 μW in Standby Mode
- Reference Design and Evaluation Board with Software Available

APPLICATIONS

Seismic Data Acquisition Systems
Chromatography
Automatic Test Equipment

GENERAL DESCRIPTION

The AD1555 is a complete sigma-delta modulator, combined with a programmable gain amplifier intended for low frequency, high dynamic range measurement applications. The AD1555 outputs a ones-density bitstream proportional to the analog input. When used in conjunction with the AD1556 digital filter/decimator, a high performance ADC is realized.

The continuous-time analog modulator input architecture avoids the need for an external antialias filter. The programmable gain front end simplifies system design, extends the dynamic range, and reduces the system board area. Low operating power and standby modes makes the AD1555 ideal for remote battery-powered data acquisition systems.

The AD1555 is fabricated on Analog Devices' BiCMOS process that has high performance bipolar devices along with CMOS transistors. The AD1555 and AD1556 are packaged, respectively, in 28-lead PLCC and 44-lead MQFP packages and are specified from –55°C to +85°C (AD1556 and AD1555 B Grade) and from 0°C to 85°C (AD1555 A Grade).

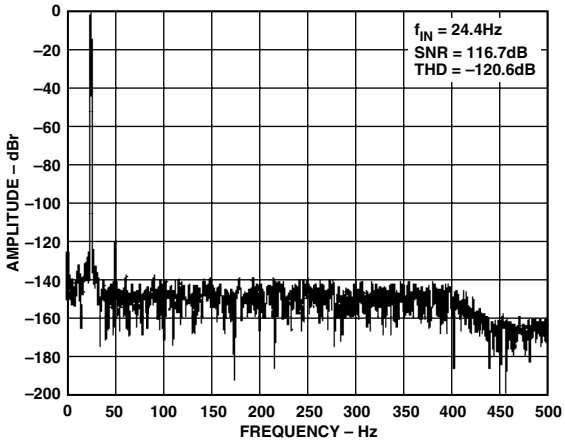
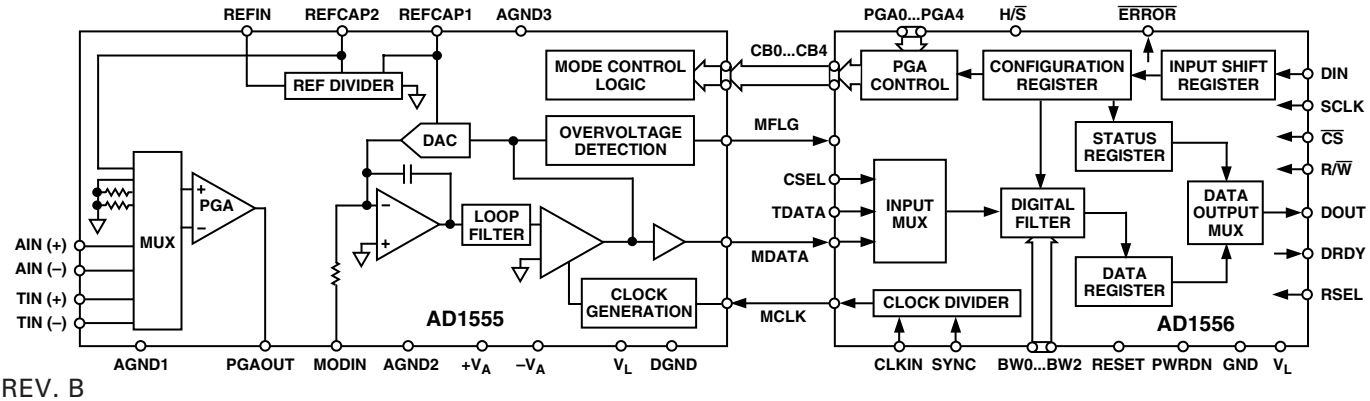


Figure 1. FFT Plot, Full-Scale AIN Input, Gain of 1

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD1555–SPECIFICATIONS

($+V_A$ = +5 V; $-V_A$ = –5 V; V_L = 5 V; AGND = DGND = 0 V; MCLK = 256 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Notes	AD1555BP Min	AD1555BP Typ	AD1555BP Max	AD1555AP Min	AD1555AP Typ	AD1555AP Max	Unit
PGA Gain Settings	1, 2.5, 8.5, 34, 128							
AC ACCURACY								
Dynamic Range[1]	PGA Gain of 1	116.5	120		116	120		dB
	PGA Gain of 2.5	116	119.5		115.5	119.5		dB
	PGA Gain of 8.5	114	117.5		114	117.5		dB
	PGA Gain of 34	104.5	109.5		104.5	109.5		dB
	PGA Gain of 128		98			98		dB
Total Harmonic Distortion[2]	PGA Gain of 1		–120	–111		–120	–107	dB
	PGA Gain of 2.5		–116	–108		–116	–107	dB
	PGA Gain of 8.5		–116	–106		–116	–105	dB
	PGA Gain of 34		–115	–101		–115	–101	dB
	PGA Gain of 128		–108			–108		dB
Jitter Tolerance[3]				300			300	ps
Intermodulation Distortion[4]	PGA Gain of 1		122			122		dB
DC ACCURACY								
Absolute Gain Error[5]	PGA Gain of 1, 2.5	–3.5		+3.5	–3.5		+3.5	%
	PGA Gain of 8.5	–4.5		+4.5	–4.5		+4.5	%
	PGA Gain of 34	–10		+10	–10		+10	%
Gain Stability Over Temperature[5]			±15			±15		ppm/°C
Offset[5, 6]	All PGA Gain		–60			–60		mV
Offset Drift[5, 6]			6			6		µV/°C
ANALOG INPUT								
Full-Scale Nondifferential Input	MODIN			±2.25			±2.25	V
Input Impedance	MODIN		20			20		kΩ
Full-Scale Differential Input	PGA Gain of 1			±2.25			±2.25	V
	Other PGA Gain Settings		See Table I			See Table I		
Differential Input Impedance	AIN, TIN Inputs		140			140		MΩ
Common-Mode Range				±2.25			±2.25	V
Common-Mode Rejection Ratio	V_{CM} = ±2.25 V, f_{IN} = 200 Hz							
	PGA Gain of 1	93	101		91	101		dB
	PGA Gain of 2.5	95	102		91.5	102		dB
	PGA Gain of 8.5, 34	95.5	108		94.5	108		dB
	PGA Gain of 128		108			108		dB
Power Supply Rejection Ratio[7]			50			50		dB
AIN to TIN Crosstalk Isolation	f_{IN} = 200 Hz		130			130		dB
Differential Input Current			130			130		nA
TEMPERATURE RANGE[8]								
Specified Performance	T_{MIN} to T_{MAX}	–55		+85	0		85	°C
REFERENCE INPUT[9]								
Input Voltage Range		2.990	3.0	3.010	2.990	3.0	3.010	V
Input Current			130			130		µA
DIGITAL INPUTS OUTPUTS								
V_{IL}		–0.3		+0.8	–0.3		+0.8	V
V_{IH}		2.0		V_L + 0.3	2.0		V_L + 0.3	V
I_{IL}		–10		+10	–10		+10	µA
I_{IH}		–10		+10	–10		+10	µA
V_{OL}	I_{SINK} = +2 mA			0.4			0.4	V
V_{OH}	I_{SOURCE} = –2 mA	2.4			2.4			V

Parameter	Notes	AD1555BP Min	AD1555BP Typ	AD1555BP Max	AD1555AP Min	AD1555AP Typ	AD1555AP Max	Unit
POWER SUPPLIES								
Recommended Operating Conditions								
$+V_A$		4.75	5	5.25	4.75	5	5.25	V
$-V_A$		–5.25	–5	–4.75	–5.25	–5	–4.75	V
V_L		4.75	5	5.25	4.75	5	5.25	V
Quiescent Currents								
$I(+V_A)$[10]			8	10		8	10	mA
$I(-V_A)$[10]			8	9.5		8	9.5	mA
$I(V_L)$			30	42		30	42	µA
Power Dissipation[10]			77	96		77	96	mW
	PGA in Standby Mode[11]		56	70		56	70	mW
	In Power-Down Mode[11, 12]							
	Reference Input = 3 V		650			650		µW
	Reference Input = 0 V		250			250		µW

NOTES
[1]Tested at the output word rate F_O = 1 kHz. F_O is the AD1556 output word rate, the inverse of the sampling rate. See Tables I, Ia, Ib for other output word rates.
[2]Tested with a full-scale input signal at approximately 24 Hz.
[3]This parameter is guaranteed by design.
[4]Tested at the output word rate F_O = 1 kHz with input signals of 30 Hz and 50 Hz, each 6 dB down full scale.
[5]This specification is for the AD1555 only and does not include the errors from external components as, for instance, the external reference.
[6]This offset specification is referred to the modulator output.
[7]Characterized with a 100 mV p-p sine wave applied separately to each supply.
[8]Contact factory for extended temperature range.
[9]Recommended Reference: AD780BR.
[10]Specified with analog inputs grounded.
[11]See Table III for configuration conditions.
[12]Specified with MCLK input grounded.

Specifications subject to change without notice.

AD1556–SPECIFICATIONS (V_L = 2.85 V to 5.25 V; CLKIN = 1.024 MHz; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	Notes	AD1556AS Min	AD1556AS Typ	AD1556AS Max	Unit
FILTER PERFORMANCES					
Pass-Band Ripple		–0.05		+0.05	dB
Stop-Band Attenuation	All Filters Except F_O =16 kHz			–135	dB
	F_O =16 kHz			–86	dB
Filters Characteristics			See Table II		
DIGITAL INPUTS OUTPUTS					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		V_L + 0.3	V
I_{IL}		–10		+10	µA
I_{IH}		–10		+10	µA
V_{OL}	I_{SINK} = +2 mA			+0.5	V
V_{OH}	I_{SOURCE} = –2 mA	V_L – 0.6			V
POWER SUPPLIES					
Specified Performance					
V_L		2.85		5.25	V
Quiescent Currents					
$I(V_L)$			4	5	mA
Power Dissipation	V_L = 3.3 V, F_O = 1 kHz		6.2	8.5	mW
	In Power-Down Mode		70		µW
TEMPERATURE RANGE*					
Specified Performance, T_{MIN} to T_{MAX}		–55		+85	°C

*Contact factory for extended temperature range.

Specifications subject to change without notice.

Table I. Dynamic and Noise Typical Performances

Input and Gain	MODIN	PGA = 1 (0 dB)	PGA = 2.5 (8 dB)	PGA = 8.5 (19 dB)	PGA = 34 (31 dB)	PGA = 128 (42 dB)
Input Range	1.6 V rms	1.6 V rms	636 mV rms	187 mV rms	47 mV rms	12.4 mV rms
Dynamic Range						
F_O = 16 kHz (1/16 ms)	40 dB	40 dB	40 dB	40 dB	40 dB	40 dB
F_O = 8 kHz (1/8 ms)	69 dB	69 dB	69 dB	69 dB	69 dB	69 dB
F_O = 4 kHz (1/4 ms)	98 dB	98 dB	98 dB	98 dB	97 dB	91 dB
F_O = 2 kHz (1/2 ms)	117 dB	117 dB	116.5 dB	114.5 dB	106.5 dB	95 dB
F_O = 1 kHz (1 ms)	120 dB	120 dB	119.5 dB	117.5 dB	109.5 dB	98 dB
F_O = 500 Hz (2 ms)	123 dB	123 dB	122.5 dB	120 dB	112.5 dB	101 dB
F_O = 250 Hz (4 ms)	126 dB	126 dB	125.5 dB	123 dB	115.5 dB	104 dB
Equivalent Input Noise						
F_O = 16 kHz (1/16 ms)	15.5 mV rms	15.5 mV rms	6.17 mV rms	1.84 mV rms	470 µV rms	138 µV rms
F_O = 8 kHz (1/8 ms)	560 µV rms	560 µV rms	220 µV rms	65.5 µV rms	16.4 µV rms	4.5 µV rms
F_O = 4 kHz (1/4 ms)	20 µV rms	20 µV rms	8 µV rms	2.36 µV rms	661 nV rms	351 nV rms
F_O = 2 kHz (1/2 ms)	2.25 µV rms	2.25 µV rms	952 nV rms	353 nV rms	225 nV rms	223 nV rms
F_O = 1 kHz (1 ms)	1.59 µV rms	1.59 µV rms	674 nV rms	250 nV rms	159 nV rms	159 nV rms
F_O = 500 Hz (2 ms)	1.13 µV rms	1.13 µV rms	477 nV rms	187 nV rms	113 nV rms	111 nV rms
F_O = 250 Hz (4 ms)	797 nV rms	797 nV rms	338 nV rms	133 nV rms	80 nV rms	79 nV rms

Table Ia. Minimum Dynamic Performances (AD1555AP Only)*

Input and Gain	MODIN	PGA = 1 (0 dB)	PGA = 2.5 (8 dB)	PGA = 8.5 (19 dB)	PGA = 34 (31 dB)
F_O = 1 kHz (1 ms)	116	116	115.5	114	104.5
F_O = 500 Hz (2 ms)	119	119	118.5	117	107.5
F_O = 250 Hz (4 ms)	122	122	121.5	120	110.5

*Not tested in production. Guaranteed by design.

Table Ib. Minimum Dynamic Performances (AD1555BP Only)*

Input and Gain	MODIN	PGA = 1 (0 dB)	PGA = 2.5 (8 dB)	PGA = 8.5 (19 dB)	PGA = 34 (31 dB)
F_O = 1 kHz (1 ms)	116.5	116.5	116	114	104.5
F_O = 500 Hz (2 ms)	119.5	119.5	119	117	107.5
F_O = 250 Hz (4 ms)	122.5	122.5	121	120	110.5

*Not tested in production. Guaranteed by design.

Table II. Filter Characteristics

Output Word Rate F_O (Sampling Rate in ms)	Pass Band (Hz)	–3 dB Frequency (Hz)	Stop Band (Hz)	Group Delay (ms)
16000 Hz (1/16 ms)	6000	6480	8000	0.984
8000 Hz (1/8 ms)	3000	3267.5	4000	3
4000 Hz (1/4 ms)	1500	1634	2000	6
2000 Hz (1/2 ms)	750	816.9	1000	12
1000 Hz (1 ms)	375	408.5	500	24
500 Hz (2 ms)	187.5	204.2	250	48
250 Hz (4 ms)	93.75	101.4	125	93

TIMING SPECIFICATIONS ($+V_A$ = +5 V ± 5%; $-V_A$ = –5 V ± 5%; AD1555 V_L = 5 V ± 5%, AD1556 V_L = 2.85 V to 5.25 V; CLKIN = 1.024 MHz; AGND = DGND = 0 V; C_L = 50 pF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

	Symbol	Min	Typ	Max	Unit
CLKIN Frequency[1]	f_{CLKIN}	0.975	1.024	1.075	MHz
CLKIN Duty Cycle Error		45		55	%
MCLK Output Frequency[1]			$f_{CLKIN}/4$		
SYNC Setup Time	t_1	10			ns
SYNC Hold Time	t_2	10			ns
CLKIN Rising to MCLK Output Falling on SYNC	t_3			20	ns
CLKIN Falling to MCLK Output Rising	t_4			20	ns
CLKIN Falling to MCLK Output Falling	t_5			20	ns
MCLK Input Falling to MDATA Falling	t_6			30	ns
MCLK Input Rising to MDATA and MFLG Valid	t_7			100	ns
TDATA Setup Time after SYNC	t_8	5			ns
TDATA Hold Time	t_9	5			ns
RESET Setup Time	t_{10}	15			ns
RESET Hold Time	t_{11}	15			ns
CLKIN Falling to DRDY Rising	t_{12}			20	ns
CLKIN Rising to $\overline{\text{DRDY}}$ Falling[2]	t_{13}			20	ns
CLKIN Rising to $\overline{\text{ERROR}}$ Falling	t_{14}			50	ns
RSEL to Data Valid	t_{15}			25	ns
RSEL Setup to SCLK Falling	t_{16}	10			ns
DRDY to Data Valid	t_{17}			25	ns
DRDY High Setup to SCLK Falling	t_{18}	10			ns
R/$\overline{\text{W}}$ to Data Valid	t_{19}			25	ns
R/$\overline{\text{W}}$ High Setup to SCLK Falling	t_{20}	10			ns
$\overline{\text{CS}}$ to Data Valid	t_{21}			25	ns
$\overline{\text{CS}}$ Low Setup to SCLK Falling	t_{22}	10			ns
SCLK Rising to DOUT Valid	t_{23}			25	ns
SCLK High Pulsewidth	t_{24}	25			ns
SCLK Low Pulsewidth	t_{25}	25			ns
SCLK Period	t_{26}	70			ns
SCLK Falling to DRDY Falling[2]	t_{27}			20	ns
$\overline{\text{CS}}$ High or R/$\overline{\text{W}}$ Low to DOUT Hi-Z	t_{28}			20	ns
R/$\overline{\text{W}}$ Low Setup to SCLK Falling	t_{29}	10			ns
$\overline{\text{CS}}$ Low Setup to SCLK Falling	t_{30}	10			ns
Data Setup Time to SCLK Falling	t_{31}	10			ns
Data Hold Time after SCLK Falling	t_{32}	10			ns
R/$\overline{\text{W}}$ Hold Time after SCLK Falling	t_{33}	10			ns

NOTES
[1]The gain of the modulator is proportional to f_{CLKIN} and MCLK frequency.
[2]With DRDYBUF low only. When DRDYBUF is high, this timing also depends on the value of the external pull-down resistor.

Specifications subject to change without notice.

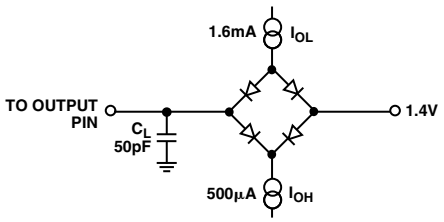


Figure 2. Load Circuit for Digital Interface Timing

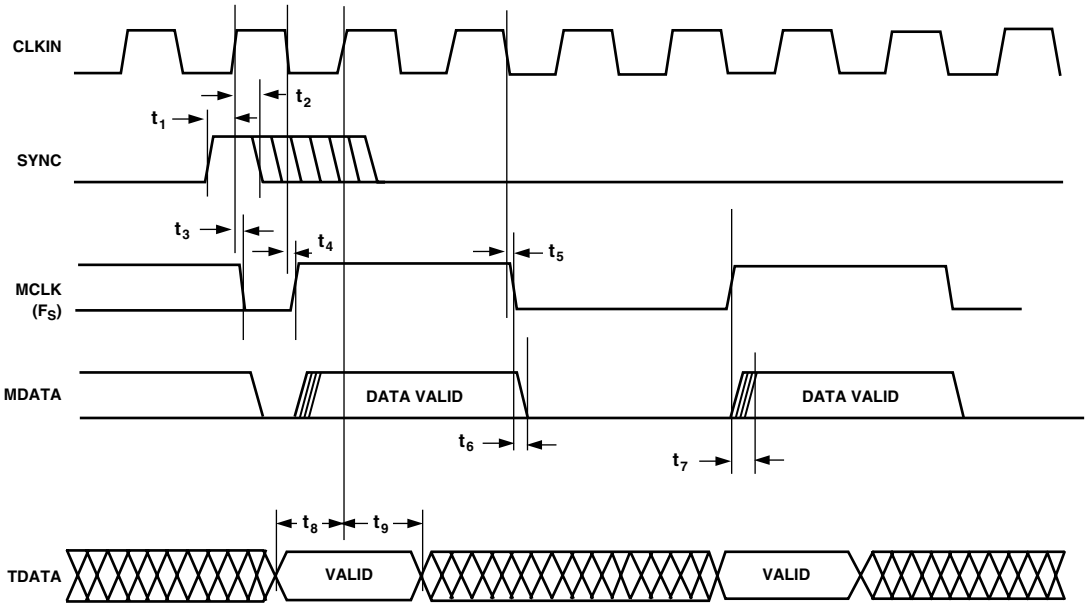


Figure 3. AD1555/AD1556 Interface Timing

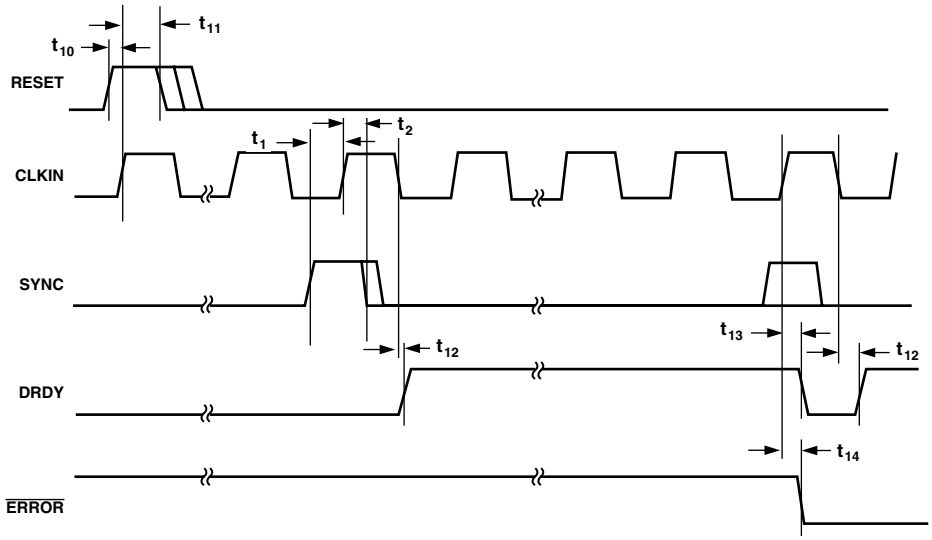


Figure 4. AD1556 RESET, DRDY, and Overwrite Timings

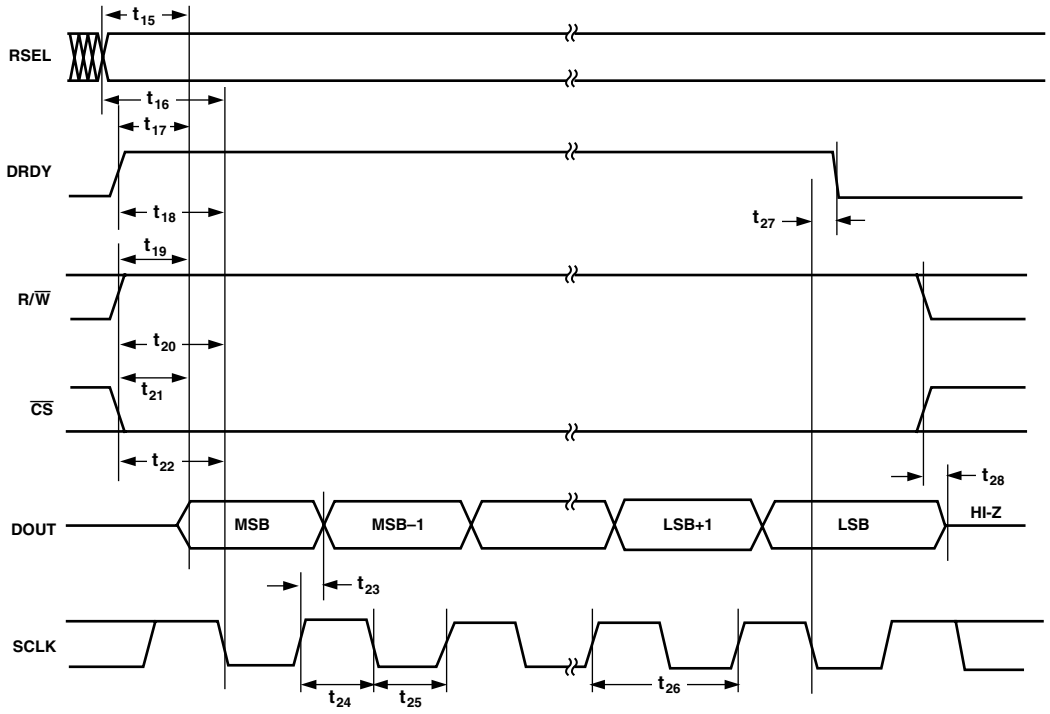


Figure 5. Serial Read Timing

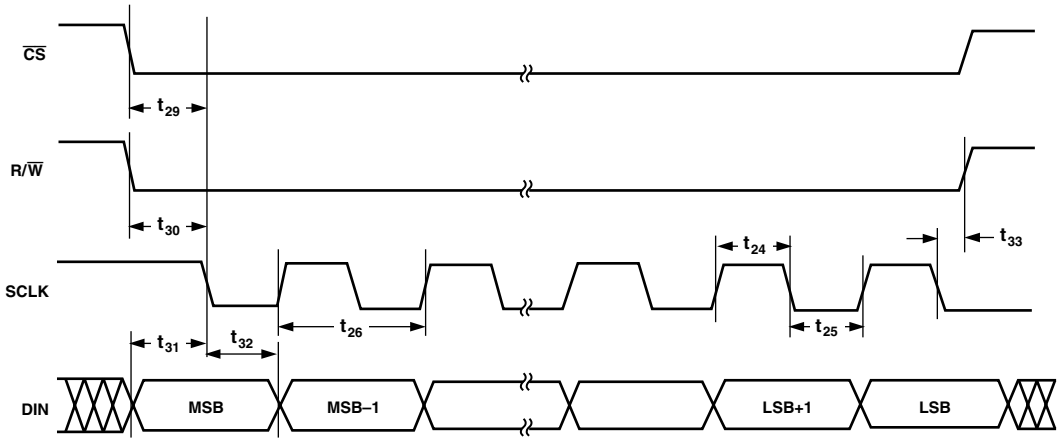


Figure 6. Serial Write Timing

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
- Pins 7, 8, 23, 24, 25, 28 ..... $-V_A$ – 0.3 V to $+V_A$ + 0.3 V
- AIN(+), AIN(–) DC Input Current ..... ±100 mA
- AIN(+), AIN(–) 2 µs Pulse Input Current ..... ±1.5 A

Supply Voltages
- $+V_A$ to $-V_A$ ..... –0.3 V to +14 V
- $+V_A$ to AGND ..... –0.3 V to +7 V
- $-V_A$ to AGND ..... –7 V to +0.3 V
- V_L to DGND ..... –0.3 V to +7 V

Ground Voltage Differences
- DGND, AGND1, AGND2, AGND3 ..... ±0.3 V

Digital Inputs ..... –0.3 V to V_L + 0.3 V

Internal Power Dissipation[2]
- AD1555 ..... 1.8 W
- AD1556 ..... 1.8 W

Junction Temperature ..... 150°C

Storage Temperature ..... –65°C to +150°C

Lead Temperature Range
- (Soldering 10 sec) ..... 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
28-lead PLCC: θ_{JA} = 36°C/W, θ_{JC} = 20°C/W
44-lead MQFP: θ_{JA} = 36°C/W, θ_{JC} = 14°C/W

ORDERING GUIDE

Model	Temperature Range*	Package Description	Package Option
AD1555AP	0°C to 85°C	Plastic Lead Chip Carrier	P-28A
AD1555APRL	0°C to 85°C	Plastic Lead Chip Carrier	P-28A
AD1555BP	–55°C to +85°C	Plastic Lead Chip Carrier	P-28A
AD1555BPRL	–55°C to +85°C	Plastic Lead Chip Carrier	P-28A
AD1556AS	–55°C to +85°C	Plastic Quad Flatpack	S-44A
AD1556ASRL	–55°C to +85°C	Plastic Quad Flatpack	S-44A
EVAL-AD1555/AD1556EB			Evaluation Board
AD1555/56-REF			Reference Design

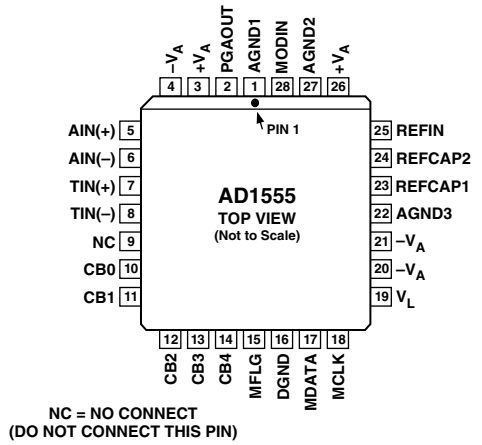
*Contact factory for extended temperature range.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1555/AD1556 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

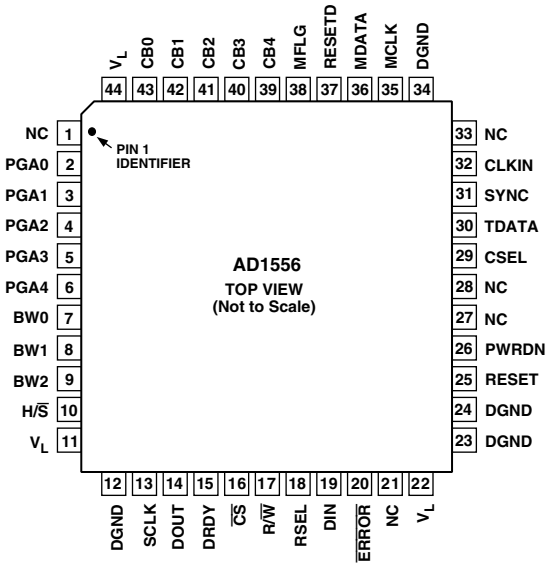
PIN CONFIGURATION

28-Lead PLCC
(P-28A)



NC = NO CONNECT
(DO NOT CONNECT THIS PIN)

44-Lead MQFP
(S-44A)



NC = NO CONNECT

AD1555 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	AGND1	Analog Ground
2	PGAOUT	Programmable Gain Amplifier Output. The output of the on-chip programmable gain amplifier is available at this pin. Refer to Table III for PGA gain settings selection.
3, 26	$+V_A$	Positive Analog Supply Voltage. +5 V nominal.
4, 20, 21	$-V_A$	Negative Analog Supply Voltage. –5 V nominal.
5	AIN(+)	Mux Input. Noninverting signal to the PGA mux input. Refer to Table III for input selection.
6	AIN(–)	Mux Input. Inverting signal to the PGA mux input. Refer to Table III for input selection.
7	TIN(+)	Mux Input. Noninverting test signal to the PGA mux input. Refer to Table III for input selection.
8	TIN(–)	Mux Input. Inverting test signal to the PGA mux input. Refer to Table III for input selection.
9	NC	Pin for Factory Use Only. This pin must be kept not connected for normal operation.
10–14	CB0–CB4	Modulator Control. These input pins control the mux selection, the PGA gain settings, and the standby modes of the AD1555. When used with the AD1556, these pins are generally directly tied to the CB0–CB4 output pins of the AD1556. CB0–CB2 are generally used to set the PGA gain or cause it to enter in the PGA standby mode (refer to Table III). CB3 and CB4 select the mux input voltage applied to the PGA as described in Table III.
15	MFLG	Modulator Error. Digital output that is pulsed high if an overrange condition occurs in the modulator.
16	DGND	Digital Ground
17	MDATA	Modulator Output. The bitstream generated by the modulator is output in a return-to-zero data format. The data is valid for approximately one-half a MCLK cycle. Refer to Figure 3.
18	MCLK	Clock Input. The clock input signal, nominally 256 kHz, provides the necessary clock for the Σ-Δ modulator. When this input is static, AD1555 is in the power-down mode.
19	V_L	Positive Digital Supply Voltage. 5 V Nominal.
22	AGND3	Analog Ground. Used as the ground reference for the REFIN pin.
23	REFCAP1	DAC Reference Filter. The reference input is internally divided and available at this pin to provide the reference for the Σ-Δ modulator. Connect an external 22 μF (5 V min) tantalum capacitor from REFCAP1 to AGND3 to filter the external reference noise.
24	REFCAP2	Reference Filter. The reference input is internally divided and available at this pin.
25	REFIN	Reference Input. This input accepts a 3 V level that is internally divided to provide the reference for the Σ-Δ modulator.
27	AGND2	Analog Ground.
28	MODIN	Modulator Input. Analog input to the modulator. Normally, this input is directly tied to PGAOUT output.

AD1556 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1, 21, 27, 28, 33	NC	No Connect
2–6	PGA0–PGA4	PGA and MUX Control Inputs. Sets the logic level of CB0-CB4 output pins respectively and the state of the corresponding bit in the configuration register upon RESET or when in hardware mode. Refer to Table III.
7–9	BW0–BW2	Output Rate Control Inputs. Sets the digital filter decimation rate and the state of the corresponding bit in the configuration register upon RESET or when in hardware mode. Refer to the Filter Specifications and Table VI.
10	H/$\overline{S}$	Hardware/Software Mode Select. Determines how the device operation is controlled. In hardware mode, H/$\overline{S}$ is high, the state of hardware pins set the mode of operation. When H/$\overline{S}$ is low, a write sequence to the Configuration Register or a previous write sequence sets the device operation.
11, 22, 44	V_L	Positive Digital Supply Voltage. 3.3 V or 5 V nominal.
12, 23, 24, 34	DGND	Digital Ground
13	SCLK	Serial Data Clock. Synchronizes data transfer to either write data on the DIN input pin or read data on the DOUT output pin.

AD1556 PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Description
14	DOUT	Serial Data Output. DOUT is used to access the conversion results or the contents of the Status Register, depending on the logic state of the RSEL pin. At the beginning of a read operation, the first data bit is output (MSB first). The data changes on the rising edge of SCLK and is valid on the SCLK falling edge.
15	DRDY	Data Ready. A logic high output indicates that data is ready to be accessed from the Output Data Register. DRDY goes low once a read operation is complete. When selected, the DRDY output pin has a type buffer that allows wired-OR connection of multiple AD1556s.
16	$\overline{CS}$	Chip Select. When set low the serial data interface pins DIN, DOUT, R/$\overline{W}$, and SCLK are active; a logic high disables these pins and sets the DOUT pin to Hi-Z.
17	R/$\overline{W}$	Read/Write. A read operation is initiated if R/$\overline{W}$ is high and $\overline{CS}$ is low. A low sets the DOUT pin to Hi-Z and allows a write operation to the device via the DIN pin.
18	RSEL	Register Select. When set high, the Conversion Data Register contents are output on a read operation. A low selects the Status Register.
19	DIN	Serial Data Input. Used during a write operation. Loads the Configuration Register via the Input Shift Register. Data is loaded MSB first and must be valid on the falling edge of SCLK.
20	$\overline{ERROR}$	Error Flag. A logic low output indicates an error condition occurred in the modulator or digital filter. When $\overline{ERROR}$ goes low the ERROR bit in the status register is set high. The $\overline{ERROR}$ output pin has an open drain type buffer with an internal 100 kΩ typical pull-up that allows wired-OR connection of multiple AD1556s.
25	RESET	Chip Reset. A logic high input clears any error condition in the status register and sets the configuration register to the state of the corresponding hardware pins. On power-up, this reset state is entered.
26	PWRDN	Power-Down Hardware Control. A logic high input powers down the filter. The convolution cycles in the digital filter and the MCLK signal are stopped. All registers retain their data and the serial data interface remains active. The power-down mode is entered on the first falling edge of CLKIN after PWRDN is taken high. When exiting the power-down mode, a SYNC must be applied to resume filter convolutions.
29	CSEL	Filter Input Select. Selects the source for input to the digital filter. A logic high selects the TDATA input, a low selects MDATA as the filter input.
30	TDATA	Test Data. Input to digital filter for user test data.
31	SYNC	Synchronization Input. The SYNC input clears the AD1556 filter in order to synchronize the start of the filter convolutions. The SYNC event is initiated on the first CLKIN rising edge after the SYNC pin goes high. The SYNC input can also be applied synchronously to the AD1556 decimation rate without resetting the convolution cycles.
32	CLKIN	Clock Input. The clock input signal, nominally 1.024 MHz, provides the necessary clock for the AD1556. This clock frequency is divided by four to generate the MCLK signal for the AD1555.
35	MCLK	Modulator Clock. Provides the modulator sampling clock frequency. The modulator always samples at one-fourth the CLKIN frequency.
36	MDATA	Modulator Data. This input receives the ones-density bit stream from the AD1555 for input to the digital filter.
37	RESETD	Decimator Reset. A logic high resets the decimator of the digital filter.
38	MFLG	Modulator Error. The MFLG input is used to detect if an overrange condition occurred in the modulator. Its logic level is sensed on the rising edge of CLKIN. When overrange condition detected, ERROR goes low and updates the status register.
43–39	CB0–CB4	Modulator Control. These output control pins represent a portion of the data loaded into the AD1556 Configuration Register. CB0–CB2 are generally used to set the PGA gain or cause it to enter in the PGA standby mode (Refer to Table III). CB3 and CB4 select the mux input voltage applied to the PGA as described in Table III.

TERMINOLOGY

DYNAMIC RANGE

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together in the bandwidth from 3 Hz to the Nyquist frequency $F_O/2$. The value for dynamic range is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the full-scale signal to the total rms noise in the bandwidth from 3 Hz to the Nyquist frequency $F_O/2$. The value for SNR is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of all the harmonic components up to Nyquist frequency $F_O/2$ to the rms value of a full-scale input signal. The value for THD is expressed in decibels.

INTERMODULATION DISTORTION (IMD)

IMD is the ratio of the rms sum of two sine wave signals of 30 Hz and 50 Hz which are each 6 dB down from full scale to the rms sum of all intermodulation components within the bandwidth from 1 Hz to the Nyquist frequency $F_O/2$. The value for IMD is expressed in decibels.

OFFSET

The offset is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code (code 000000H) at the output of the AD1556. The offset specification is referred to the output. This offset is intentionally set at a nominal value of –60 mV (see Sigma-Delta Modulator section). The value for offset is expressed in mV.

OFFSET ERROR DRIFT

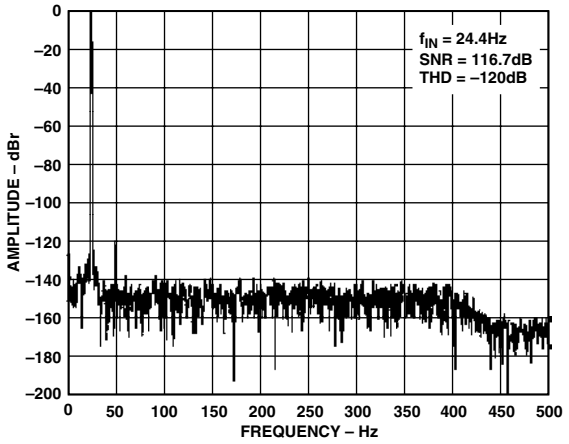
The change of the offset over temperature. It is expressed in mV.

GAIN ERROR

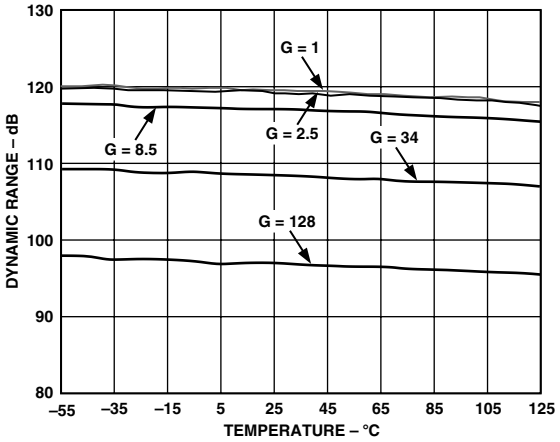
The gain error is the ratio of the difference between the actual gain and the ideal gain to the ideal gain. The actual gain is the ratio of the output difference obtained with a full-scale analog input (±2.25 V) to the full-scale span (4.5 V) after correction of the effects of the external components. It is expressed in %.

GAIN ERROR STABILITY OVER TEMPERATURE

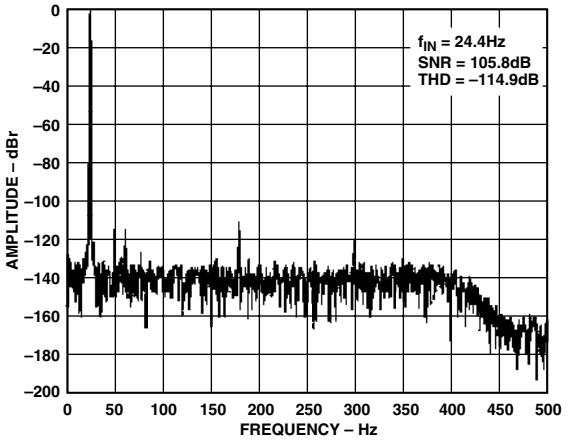
The change of the gain error over temperature. It is expressed in %.



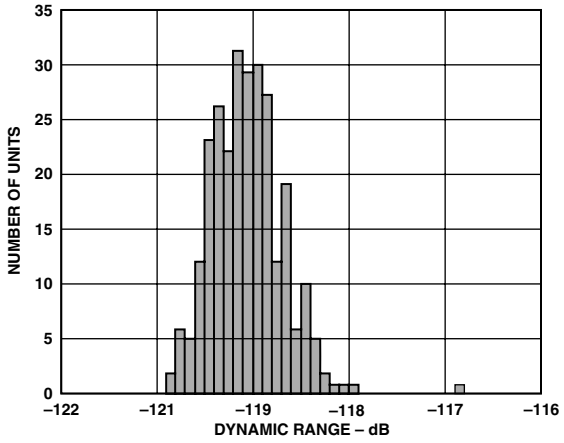
TPC 1. FFT (2048 Points) Full-Scale MODIN Input



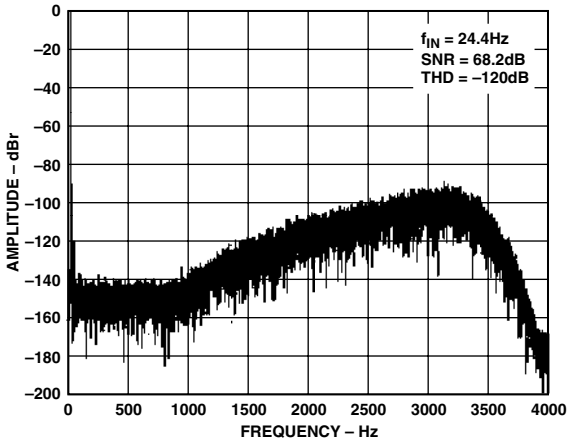
TPC 4. Dynamic Range vs. Temperature



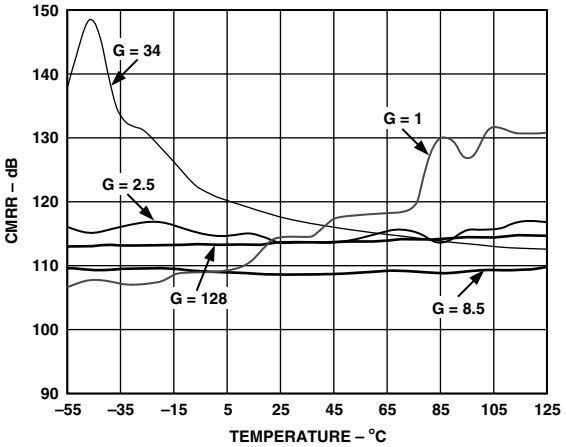
TPC 2. FFT (2048 Points) Full-Scale AIN Input, Gain of 34



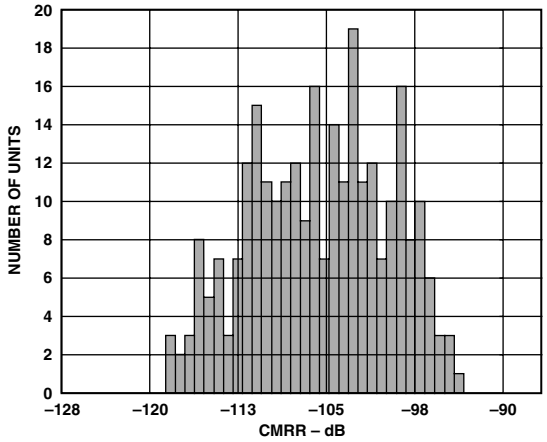
TPC 5. Dynamic Range Distribution (272 Units)



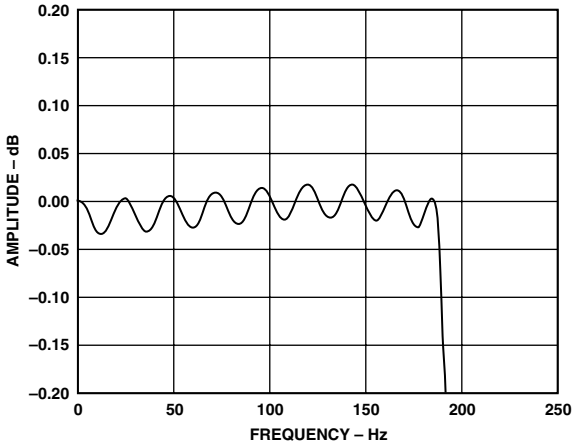
TPC 3. FFT (16384 Points) Full-Scale AIN Input, Gain of 1



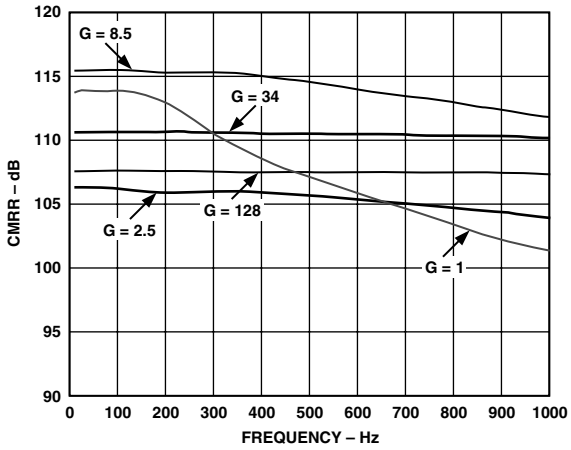
TPC 6. Common-Mode Rejection vs. Temperature



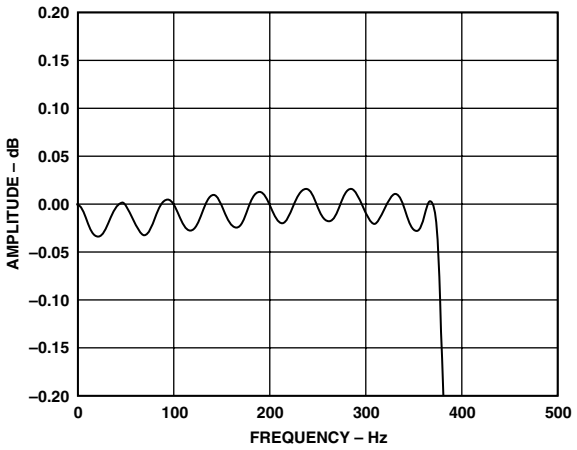
TPC 7. Common-Mode Rejection Distribution (272 Units)



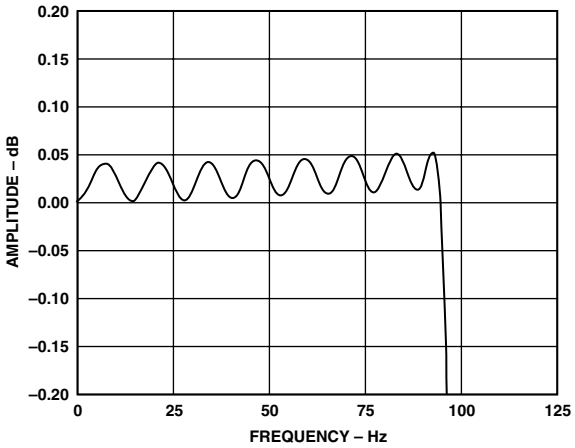
TPC 10. AD1556 Pass Band Ripple, F_O = 500 Hz (2 ms)



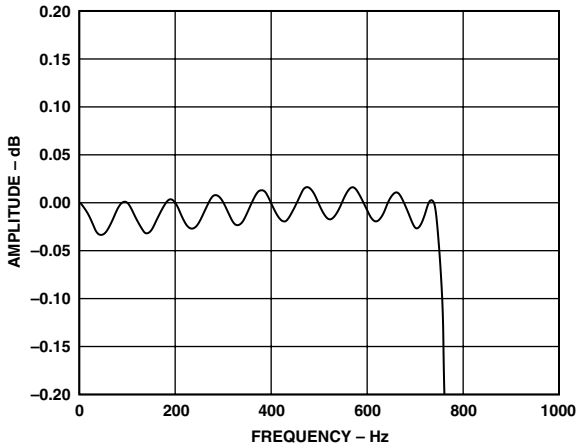
TPC 8. Common-Mode Rejection vs. Frequency



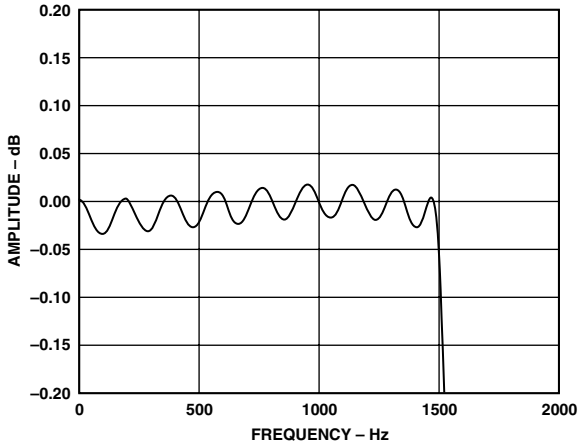
TPC 11. AD1556 Pass Band Ripple, F_O = 1 kHz (1 ms)



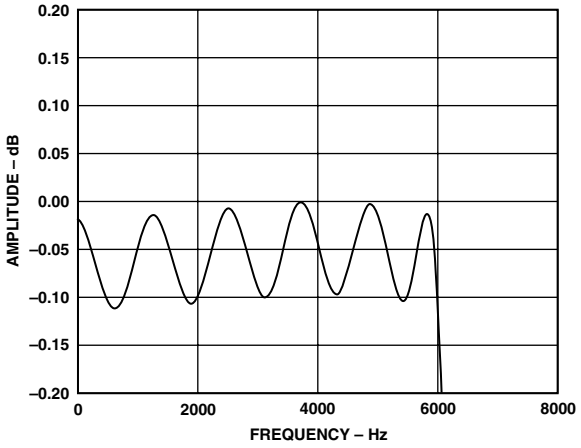
TPC 9. AD1556 Pass Band Ripple, F_O = 250 Hz (4 ms)



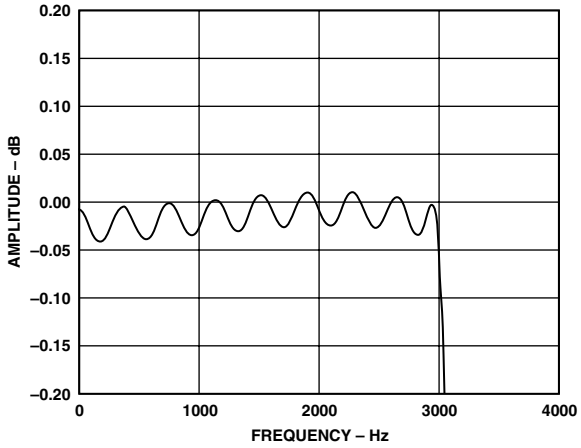
TPC 12. AD1556 Pass Band Ripple, F_O = 2 kHz (1/2 ms)



TPC 13. AD1556 Pass Band Ripple, F_O = 4 kHz (1/4 ms)



TPC 15. AD1556 Pass Band Ripple, F_O = 16 kHz (1/16 ms)



TPC 14. AD1556 Pass Band Ripple, F_O = 8 kHz (1/8 ms)

CIRCUIT DESCRIPTION

The AD1555/AD1556 chipset is a complete sigma-delta 24-bit A/D converter with very high dynamic range intended for the measurement of low frequency signals up to a few kHz such as those in seismic applications.

The AD1555 contains an analog multiplexer, a fully differential programmable gain amplifier and a fourth order sigma-delta modulator. The analog multiplexer allows selection of one fully differential input from two different external inputs, an internal ground reference or an internal full-scale voltage reference. The fully differential programmable gain amplifier (PGA) has five gain settings of 1, 2.5, 8.5, 34, and 128, which allow the part to handle a total of five different input ranges: 1.6 V rms, 636 mV rms, 187 mV rms, 47 mV rms, and 12.4 mV rms that are programmed via digital input pins (CB0 to CB4). The modulator that operates nominally at a sampling frequency of 256 kHz, outputs a bitstream whose ones-density is proportional to its input voltage. This bitstream can be filtered using the AD1556, which is a digital finite impulse low pass filter (FIR). The AD1556 outputs the data in a 24-bit word over a serial interface. The cutoff frequency and output rate of this filter can be programmed via an on-chip register or by hardware through digital input pins. The dynamic performance and the equivalent input noise vary with gain and output rate as shown in Table I. The use of the different PGA gain settings allows enhancement of the total system dynamic range up to 146 dB (gain of 34 or 128 and F_O = 250 Hz).

The AD1555 operates from a dual analog supply (±5 V), while the digital part of the AD1555 operates from a +5 V supply. The AD1556 operates from a single 3.3 V or 5 V supply. Each device exhibits low power dissipation and can be configured for standby mode.

Figure 7 illustrates a typical operating circuit.

MULTIPLEXER AND PROGRAMMABLE GAIN AMPLIFIER (PGA)

Analog Inputs

The AD1555 has two sets of fully differential inputs AIN and TIN. The common-mode rejection capability of these inputs generally surpasses the performance of conventional programmable gain amplifiers. The very high input impedance, typically higher than 140 MΩ, allows direct connection of the sensor to the AD1555 inputs, even through serial resistances. Figure 7 illustrates such a configuration. The passive filter between the sensor and the AD1555 is shown here as an example. Other filter structures could be used, depending on the specific requirements of the application. Also, the Johnson noise ($\sqrt{4\ k\ TRB}$) of the serial resistance should be taken into consideration. For instance, a 1 kΩ serial resistance reduces by approximately 1.3 dB the dynamic performance of a system using a gain setting of 128 at an output word rate F_O = 500 Hz. For applications where the sensor inputs must be protected against severe

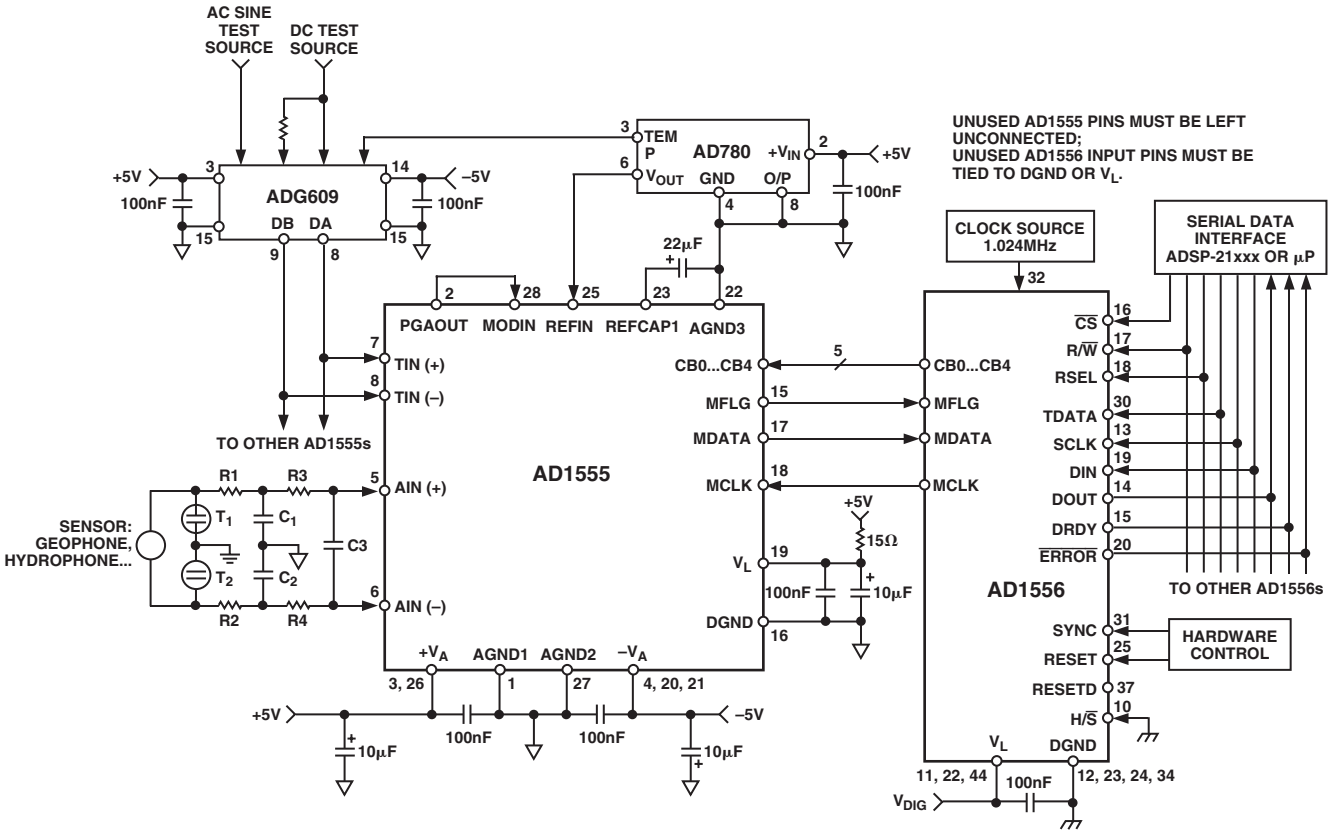


Figure 7. Typical Operating Circuit

external stresses such as lightning, the inputs AIN are specifically designed to ease the design. The external voltage spike is generally clamped by devices T1 and T2 at about hundred volts (for instance, devices T1 and T2 can be gas discharge tubes) and then generates a pulsed current in the serial resistances (R1, R3, and R2, R4). The AD1555 AIN inputs, using robust internal clamping diodes to the analog supply rails, can handle this huge pulsed input current (1.5 A during 2 μs) without experiencing any destructive damages or latch-up, whether or not the AD1555 is powered on. Meanwhile, enough time should be left between multiple spikes to avoid excessive power dissipation.

Programming the AD1555

The different hardware events of the AD1555 as multiplexer inputs selection, programmable gain settings, and power-down modes are selectable using the control pins bus CB0 to CB4 according to the Table III. This table is only valid when MCLK is toggling; otherwise, the AD1555 is powered down. When used in combination with the AD1556, this control bus could either be loaded by hardware (H/$\overline{S}$ pin high) or via the serial interface of the AD1556 (H/$\overline{S}$ pin low).

The multiplexer, which exhibits a break-before-make switching action, allows various combinations.

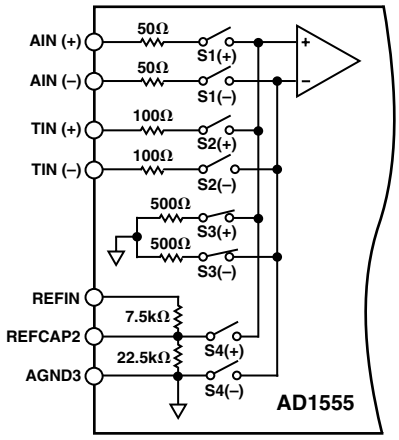


Figure 8. Simplified AD1555 Input Multiplexer

When the ground input is selected, S3(+) and S3(–) are closed, all the other switches are opened, and the inputs of the programmable gain amplifier are shorted through an accurate internal 1 kΩ resistor. This combination allows accurate calibration of the offset of the AD1555 for each gain setting. Also, a system noise calibration can be done using the internal 1 kΩ resistor as a noise reference.

Table III. PGA Input and Gain Control

CB4	CB3	CB2	CB1	CB0	Description
0	0	0	0	0	Ground Input with PGA Gain of 1
0	0	0	0	1	Ground Input with PGA Gain of 2.5
0	0	0	1	0	Ground Input with PGA Gain of 8.5
0	0	0	1	1	Ground Input with PGA Gain of 34
0	0	1	0	0	Ground Input with PGA Gain of 128
0	1	0	0	0	Test Inputs TIN(+) and TIN(–) with PGA Gain of 1
0	1	0	0	1	Test Inputs TIN(+) and TIN(–) with PGA Gain of 2.5
0	1	0	1	0	Test Inputs TIN(+) and TIN(–) with PGA Gain of 8.5
0	1	0	1	1	Test Inputs TIN(+) and TIN(–) with PGA Gain of 34
0	1	1	0	0	Test Inputs TIN(+) and TIN(–) with PGA Gain of 128
1	0	0	0	0	Signal Inputs AIN(+) and AIN(–) with PGA Gain of 1
1	0	0	0	1	Signal Inputs AIN(+) and AIN(–) with PGA Gain of 2.5
1	0	0	1	0	Signal Inputs AIN(+) and AIN(–) with PGA Gain of 8.5
1	0	0	1	1	Signal Inputs AIN(+) and AIN(–) with PGA Gain of 34
1	0	1	0	0	Signal Inputs AIN(+) and AIN(–) with PGA Gain of 128
1	1	0	0	0	V_{REF} Input with PGA Gain of 1
1	1	0	0	1	Sensor Test 1: Signal inputs AIN(+) and AIN(–) with AIN(+) and AIN(–) inputs tied respectively to TIN(+) and TIN(–) inputs and with PGA Gain of 1.
1	1	0	1	0	Sensor Test 2: Signal inputs TIN(+) and TIN(–) with AIN(–) input tied to TIN(–) input and with PGA Gain of 1.
X	X	1	0	1	PGA Powered Down
X	X	1	1	X	Chip Powered Down

When the V_{REF} input is selected, S4(+) and S4(–) are closed, all the other switches are opened, and a reference voltage (2.25 V) equal to half of the full-scale range is sampled. In this combination, the gain setting is forced to be the gain of 1.

When the signal input is selected, S1(+) and S1(–) are closed, all the other switches are opened, and the differential input signal between AIN(+) and AIN(–) is sampled. This is the main path for signal acquisition.

When the test input is selected, S2(+) and S2(–) are closed, all the other switches are opened, and the differential input signal between TIN(+) and TIN(–) is sampled. This combination allows acquisition of a test signal or a secondary channel with the same level of performance as with AIN inputs. By applying known voltages to these inputs, it is also possible to calibrate the gain for each gain setting.

When the Sensor Test 1 is selected, S1(+), S1(–), S2(+), and S2(–) are closed, all the other switches are opened, and the gain setting is forced to be the gain of 1. In this configuration, a source between TIN(+) and TIN(–) may be applied to the sensor to determine its impedance or other characteristics. The total internal serial resistance between each AIN input and the PGA inputs, nominally 66 Ω, slightly affects these measurements. The total internal serial resistance between each TIN input and the PGA inputs is nominally 116 Ω.

When the Sensor Test 2 is selected, S1(+), S2(+), and S2(–) are closed, all the other switches are opened. This configuration could be used to test the sensor isolation.

Power-Down Modes of the AD1555

The AD1555 has two power-down modes. The multiplexer and programmable gain amplifier can be powered down by the CB2–CB0 setting of "101." The entire chip is powered down by either CB2–CB1 set to "11" or by keeping the clock input MCLK at a fixed level high or low. Less shutdown current flows with MCLK low. The least power dissipation is achieved when the external reference is shut down eliminating the current through the 30 kΩ nominal load at REFIN. When in power-down, the multiplexer is switched to the "ground input."

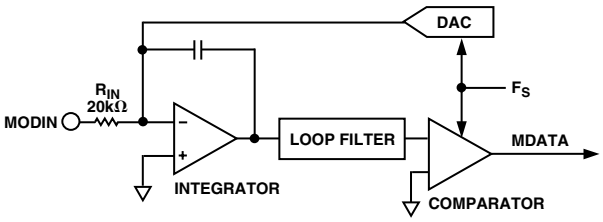


Figure 9. Sigma-Delta Modulator Block Diagram

SIGMA-DELTA MODULATOR

The AD1555 sigma-delta modulator achieves its high level of performance, notably in dynamic range and distortion, through the use of a switched-capacitor feedback DAC in an otherwise continuous-time design. Novel circuitry eliminates the subtle distortion normally encountered when these disparate types are connected together. As a result, the AD1555 enjoys many of the benefits of both design techniques.

Because of the switched-capacitor feedback, this modulator is much less sensitive to timing jitter than is the usual continuous-time design that relies on the duty cycle of the clock to control a switched-current feedback DAC.

Unlike its fully switched-capacitor counterparts, the modulator input circuitry is nonsampling, consisting simply of an internal, low temperature coefficient resistor connected to the summing node of the input integrator. Among the advantages of this continuous-time architecture is a relaxation of requirements for the antialias filter; in fact, the output of the programmable gain amplifier, PGAOUT, may be tied directly to the input of the modulator MODIN without any external filter. Another advantage is that the gain may be adjusted to accommodate a higher input range by adding an external series resistor at MODIN.

The modulator of the AD1555 is fourth order, which very efficiently shapes the quantization noise so that it is pushed toward the higher frequencies (above 1 kHz) as shown in TPC 3. This high frequency noise is attenuated by the AD1556 digital filter. However, when the output word rate (OWR) of the AD1556 is higher than 4 kHz (–3 dB frequency is higher than 1634 Hz), the efficiency of this filtering is limited and slightly reduces the dynamic range, as shown in the Table I. Hence, when possible, an OWR of 2 kHz or lower is generally preferred.

Sigma-delta modulators have the potential to generate idle tones that occur for dc inputs close to ground. To prevent this undesirable effect, the AD1555 modulator offset is set to about –60 mV. In this manner, any existing idle tones are moved out of the band of interest and filtered out by the digital filter.

Also, sigma-delta modulators may oscillate when the analog input is overranged. To avoid any instability, the modulator of the AD1555 includes circuitry to detect a string of 16 identical bits ("0" or "1"). Upon this event, the modulator is reset by discharging the integrator and loop filter capacitors and MFLG is forced high. After 1.5 MCLK cycles, MFLG returns low.

DIGITAL FILTERING

The AD1556 is a digital finite impulse response (FIR) linear phase low pass filter and serves as the decimation filter for the AD1555. It takes the output bitstream of the AD1555, filters and decimates it by a user-selectable choice of seven different filters associated with seven decimation ratios, in power of 2 from 1/16 to 1/1024. With a nominal bit rate of 256 kbits/s at the AD1556 input, the output word rate (the inverse of the sampling rate) ranges from 16 kHz (1/16 ms) to 250 Hz (4 ms) in powers of 2. The AD1556 filter achieves a maximum pass band flatness of ±0.05 dB for each decimation ratio and an out-of-band attenuation of –135 dB maximum for each decimation ratio except 1/16 (OWR = 16 kHz) at which the out-of-band attenuation is –86 dB maximum. Table II gives for each filter the pass band frequency, the –3 dB frequency, the stop-band frequency, and the group delay. The pass band frequency is 37.5% of the output word rate, and the –3 dB frequency is approximately 41% of the output word rate. The noise generated by the AD1556, even that due to the word truncation, has a negligible impact on the dynamic range performance of the AD1555/AD1556 chipset.

Although dedicated to the AD1555, the AD1556 can also be used as a very efficient and low power, low pass, digital filter of a bitstream generated by other Σ-Δ modulators.

Architecture

The functional block diagram of the filter portion of the AD1556 is given in Figure 10. The basic architecture is a two-stage filter. The second stage has a decimation ratio of 4 for all filters except at the output word rate of 250 Hz, where the decimation ratio is 8. Each filter is a linear phase equiripple FIR implemented by summing symmetrical pairs of data samples and then convoluting by multiplication and accumulation.

The input bitstream at 256 kHz enters the first filter and is multiplied by the 26-bit wide coefficients tallied in Table IV. Due to the symmetry of the filter, only half of the coefficients are stored in the internal ROM and each is used twice per convolution. Because the multiplication uses a 1-bit input data, the convolution for the first stage is implemented with a single accumulator 29-bits wide to avoid any truncation in the accumulation process. The output of the first-stage filter is decimated with the ratios given in Table IV and then are stored in an internal RAM which truncates the accumulator result to 24 bits.

The second-stage filter architecture is similar to the first stage. The main difference is the use of a true multiplier. The multiplier, the accumulator, and the output register, which are respectively 32-bits, 35-bits and 24-bits wide, introduce some truncation that does not affect the overall dynamic performance of the AD1555/AD1556 chipset.

Filter Coefficients

As indicated before, each stage for each filter uses a different set of coefficients. These coefficients are provided with the EVAL-AD1555/AD1556EB, the evaluation board for the AD1555 and the AD1556.

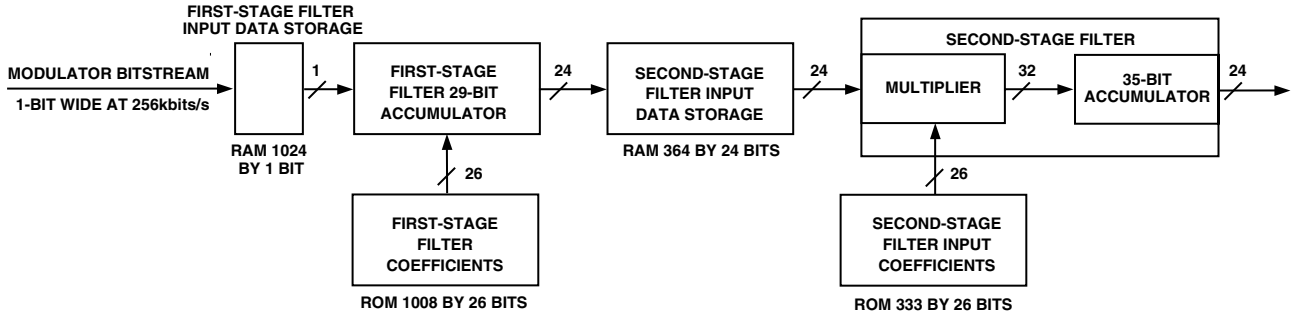


Figure 10. AD1556 Filter Functional Block Diagram

Table IV. Filter Definition

Output Word Rate F_O (Hz) (Sampling Rate [ms])	Decimation Ratio		Number of Coefficients	
	First Stage	Second Stage	First Stage	Second Stage
16000 [1/16 ms]	4	4	32	118
8000 [1/8 ms]	8	4	64	184
4000 [1/4 ms]	16	4	128	184
2000 [1/2 ms]	32	4	256	184
1000 [1 ms]	64	4	512	184
500 [2 ms]	128	4	1024	184
250 [4 ms]	128	8	1024	364

RESET Operation
The RESET pin initializes the AD1556 in a known state. RESET is active on the next CLKIN rising edge after the RESET input is brought high as shown in Figure 4. The reset value of each bit of the configuration and the status registers are indicated in Table V and Table VIII. The filter memories are not cleared by the reset. Filter convolutions begin on the next CLKIN rising edge after the RESET input is returned low. A RESET operation is done on power-up, independent of the RESET pin state.

In multiple ADCs applications where absolute synchronization—even below the noise floor—is required, RESETD, which resets the decimator, can be tied to RESET to ensure this synchronization.

Power-Down Operation
The PWRDN pin puts the AD1556 in a power-down state. PWRDN is active on the next CLKIN rising edge after the PWRDN input is brought high. While in this state, MCLK is held at a fixed level and the AD1555 is therefore powered down too. The serial interface remains active allowing read and write operations of the AD1556. The configuration and status registers maintain their content during the power-down state.

SYNC Operation
SYNC is used to create a relationship between the analog input signal and the output samples of the AD1556. The SYNC event does two things:

- It synchronizes the AD1555 clock, MCLK, to the AD1556 clock, CLKIN, as shown in Figure 3.
- It clears the filter and then initiates the filter convolution. Exactly one sampling rate delay later, the DRDY pin goes high. A SYNC event occurs on the next CLKIN rising edge after the SYNC input is brought high as shown in Figure 3. The DRDY output goes high on the next falling edge of CLKIN. SYNC may be applied once or kept high, or applied synchronously at the output word rate, all with the same effect.

Configuring and Interfacing the AD1556
The AD1556 configuration can be loaded either by hardware (H/$\overline{S}$ pin high) or via the serial interface of the AD1556 (H/$\overline{S}$ pin low). To operate with the AD1556, the CLKIN clock must be kept running at the nominal frequency of 1.024 MHz. Table V gives the description of each bit of the configuration register and Table VI defines the selection of the filter bandwidth. When the software mode is selected (H/$\overline{S}$ pin low), the configuration register is loaded using the pins DIN, SCLK, $\overline{CS}$, and R/$\overline{W}$. In this mode, when RESET is active, the configuration register mimics the selection of the hardware pins. The AD1556 and the AD1555 can be put in power-down by software.

The DRDYBUF bit controls the operating mode of the DRDY output pin. When the DRDYBUF bit is low, the DRDY is a conventional CMOS push-pull output buffer as shown in Figure 11. When the DRDYBUF bit is high, the DRDY output pin is an open drain PMOS pull-up as shown in Figure 11. Many DRDY pins may be connected with an external pull-down resistor in a wired OR to minimize the interconnection between the AD1556s and the microprocessor in multichannel applications. The DRDY pin is protected against bit contention.

By connecting DRDY to RSEL directly, and applying 48 SCLK cycles, both data and status can be read sequentially, data register first.

Table VI. Filter Bandwidth Selection

BW2	BW1	BW0	Output Rate (ms)
0	0	0	4
0	0	1	2
0	1	0	1
0	1	1	1/2
1	0	0	1/4
1	0	1	1/8
1	1	0	1/16
1	1	1	Reserved

Table V. Configuration Register Data Bits

Bit Number	Name	Description	RESET State
DB15 (MSB)	X		X
DB14	X		X
DB13	X		X
DB12	X		X
DB11	PWRDN	Power-Down Mode	PWRDN
DB10	CSEL	Select TDATA Input	CSEL
DB9	X		X
DB8	BW2	Filter Bandwidth Selection	BW2
DB7	BW1	Filter Bandwidth Selection	BW1
DB6	BW0	Filter Bandwidth Selection	BW0
DB5	DRDYBUF	DRDY Output Mode	0 (Push-Pull)
DB4	CB4	PGA Input Select	PGA4
DB3	CB3	PGA Input Select	PGA3
DB2	CB2	PGA Gain Select	PGA2
DB1	CB1	PGA Gain Select	PGA1
DB0 (LSB)	CB0	PGA Gain Select	PGA0

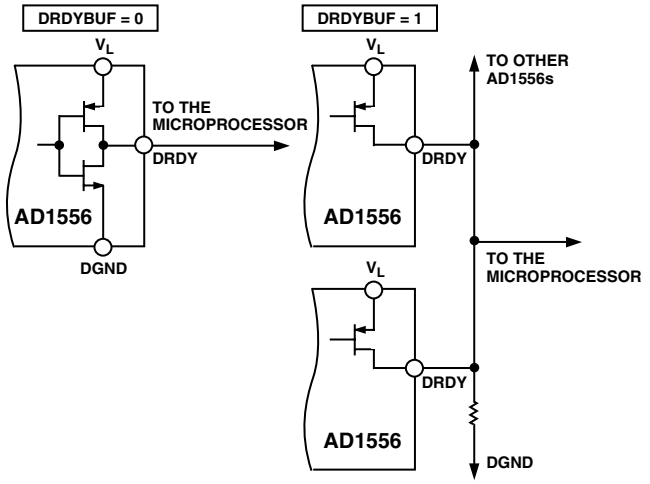


Figure 11. DRDY Output Pin Configuration

Analog Input and Digital Output Data Format

When operating with a nominal MCLK frequency of 256 kHz, the AD1555 is designed to output a ones-density bitstream from 0.166 to 0.834 on its MDATA output pin corresponding to an input voltage from –2.25 V to +2.25 V on the MODIN pin.

The AD1556 computes a 24-bit two's complement output whose codes range from decimal –6,291,456 to +6,291,455 as shown in Table VII.

Table VII. Output Coding

Analog Input MODIN	Output Code Hexa	Decimal
~ +2.526 V*	5FFFFF	+6291455
~ +2.25 V	558105	+5603589
~ +2 V	4C00E8	+4980968
~ 0 V	000000	0
~ –2 V	B3FF17	–4980969
~ –2.25 V	AA7EFA	–5603590
~ –2.526 V*	A00000	–6291456

*Input out of range.

STATUS Register

The AD1556 status register contains 24 bits that capture potential error conditions and readback the configuration settings. The status register mapping is defined in Table VIII.

The $\overline{\text{ERROR}}$ bit is the logical OR of the other error bits, OVWR, MFLG, and ACC. $\overline{\text{ERROR}}$ and the other error bits are reset low after completing a status register read operation or upon RESET. The $\overline{\text{ERROR}}$ bit is the inverse of the $\overline{\text{ERROR}}$ output pin.

The OVWR bit indicates if an unread conversion result is overwritten in the output data register. If a data read was started but not completed when new data is loaded into the output data register, the OVWR bit is set high.

The MFLG status bit is set to the state of the MFLG input pin on the rising edge of CLKIN. MFLG will remain set high as long as the MFLG bit is set. The MFLG status bit will not change during power-down or RESET.

The ACC bit is set high and the data output is clipped to either +FS (0111 . . .) or –FS (1000 . . .) if an underflow or overflow has occurred in the digital filter.

The FLSTL bit indicates the digital filter has settled and the conversion results are an accurate representation of the analog input. FLSTL is set low on RESET, at power-up, and upon exiting the power-down state. FLSTL also goes low when SYNC sets the start of the filter's convolution cycle, when changes are made to the device setting with the hardware pins CB0–CB4, BW0–BW2, or CSEL, and when the MFLG status bit is set high. When FLSTL is low the OVWR, MFLG, ACC, and DRNG status bits will not change.

The DRNG bit is used to indicate if the analog input to the AD1555 is outside its specified operating range. The DRNG bit is set high whenever the AD1556 digital filter computes four consecutive output samples that are greater than decimal +6,291455 or all less than –6,291456.

Layout

The AD1555 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD1555 and the AD1556 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD1555, or at least as close as possible to the AD1555. If the AD1555 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD1555.

It is recommended to avoid running digital lines under the device since these will couple noise onto the die. The analog ground plane should be allowed to run under the AD1555 to avoid noise coupling. Fast switching signals such as MDATA and MCLK should be shielded with digital ground to avoid radiating noise to other sections of the board and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supply lines to the AD1555 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance resent to the AD1555 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on power supply pins $+V_A$, $-V_A$, and V_L close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The V_L supply of the AD1555 can either be a separate supply or come from the analog supply V_A. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended, if no separate supply is available, to connect the V_L digital supply to the analog supply V_A through an RC filter as shown in Figure 7.

Table VIII. Status Register Data Bits

Bit Number	Name	Description	RESET State
DB23 (MSB)	ERROR	Detects One of the Following Errors	0
DB22	OVWR	Read Sequence Overwrite Error	0
DB21	MFLG	Modulator Flag Error	MFLG
DB20	X		X
DB19	ACC	Accumulator Error	0
DB18	DRDY	Data Ready	0
DB17	FLSTL	Filter Settled	0
DB16	DRNG	Output Data Not within AD1555 Range	0
DB15	X		X
DB14	X		X
DB13	X		X
DB12	X		X
DB11	PWRDN	Power-Down Mode	PWRDN
DB10	CSEL	Select TDATA Input	CSEL
DB9	X		X
DB8	BW2	Filter Bandwidth Selection	BW2
DB7	BW1	Filter Bandwidth Selection	BW1
DB6	BW0	Filter Bandwidth Selection	BW0
DB5	X		X
DB4	CB4	PGA Input Select	PGA4
DB3	CB3	PGA Input Select	PGA3
DB2	CB2	PGA Gain Select	PGA2
DB1	CB1	PGA Gain Select	PGA1
DB0 (LSB)	CB0	PGA Gain Select	PGA0

The AD1555 has three different ground pins: AGND1, AGND2, and AGND3 plane, depending on the configuration. AGND1 should be a star point and be connected to the analog ground point. AGND2 should be directly tied to AGND1. A low impedance trace should connect in the following order: AGND3, the low side of the reference decoupling capacitor on REFCAP1, the ground of the reference voltage, and return to AGND1.

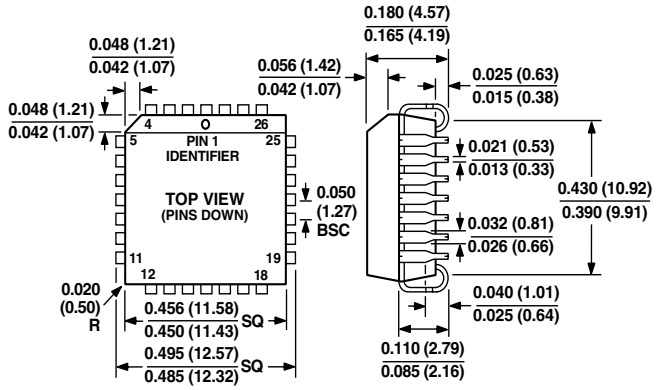
Evaluating the AD1555/AD1556 Performance

Performances of the AD1555/AD1556 can be evaluated with the evaluation board EVAL-AD1555/AD1556EB. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the PC printer port.

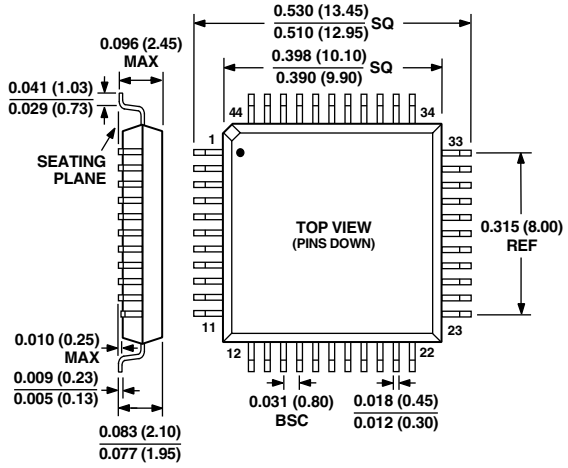
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

28-Lead PLCC
(P-28A)



44-Lead MQFP
(S-44A)



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