AS3421/22

Low Power Ambient Noise-Cancelling Speaker Driver

1 General Description

The AS3421/22 are speaker driver with Ambient Noise Cancelling function for headsets, headphones or ear pieces. It is intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphone gain calibration settings as well as all application specific settings.

The AS3421/22 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.

The simpler feed-forward topology is used to effectively reduce frequencies typically up to 2-3kHz. The feed-back topology with either 1 or 2 filtering stages has it strengths especially at very low frequencies. The typical bandwidth for feedback system is from 20Hz up to 1kHz which is a little bit lower than with feed forward systems.

The filter loop for both systems is determined by measurements, for each specific headset individually, and depends very much on mechanical designs. The gain and phase compensation filter network is implemented with cheap resistors and capacitors for lowest system costs.

AS3421/22 features also an audio playback only mode which allows the user to easily switch between ANC on and off mode. In ANC off mode unused blocks are automatically switch off to guaranty lowest power consumption in each operating mode.

2 Key Features

Microphone Input

- 128 gain steps @ 0.375dB and MUTE with AGC
- Differential, low noise microphone amplifier
- Single ended or differential mode
- Improved supply for electret microphone
- MIC gain OTP programmable

High Efficiency Headphone Amplifier

- 2x23mW, 0.1% THD+N @ 32Ω, 1.5V supply, 100dB SNR
- Bridged mode for e.g. 300Ω loads
- Click and pop less start-up and mode switching

Line Input

- Volume control via serial interface or push buttons
- 64 steps @ 0.75dB and MUTE, pop-free gain setting
- Fully differential stereo line inputs

ANC processing

- Feed-forward cancellation
- Feed-back cancellation with filter loop transfer function definable via simple RC components
- Simple in production SW calibration
- 12-30dB noise reduction (headset dependent)
- 10-3000Hz wide frequency active noise attenuation (headset dependent)

Monitor Function

- For assisted hearing, i.e. to monitor announcements
- Fixed (OTP prog.) ambient sound amplification to compensate headphone passive attenuation

Incremental Functions

- ANC with or without music on the receiving path
- Music Playback mode for lowest power consumption
- OTP ROM for automatic trimming during production (4 times programmable)

Performance Parameter

- 7mA @ 1.5V stereo ANC; <1µA quiescent
- Extended PSRR for 217Hz
- Increased TDMA noise immunity

Interfaces

- 2-wire serial control mode & volume inputs
- Calibration via Line-In or 2-wire serial interface
- Fixed 1.0-1.8V supply with internal CP

Package

- AS3421 QFN24 [4x4mm] 0.5mm pitch
- AS3422 QFN32 [5x5mm] 0.5mm pitch

3 Applications

The devices are ideal for wireless devices like stereo Bluetooth headsets as well as stereo wireless headsets.

Figure 1. AS3421 Feed Forward ANC Block Diagram

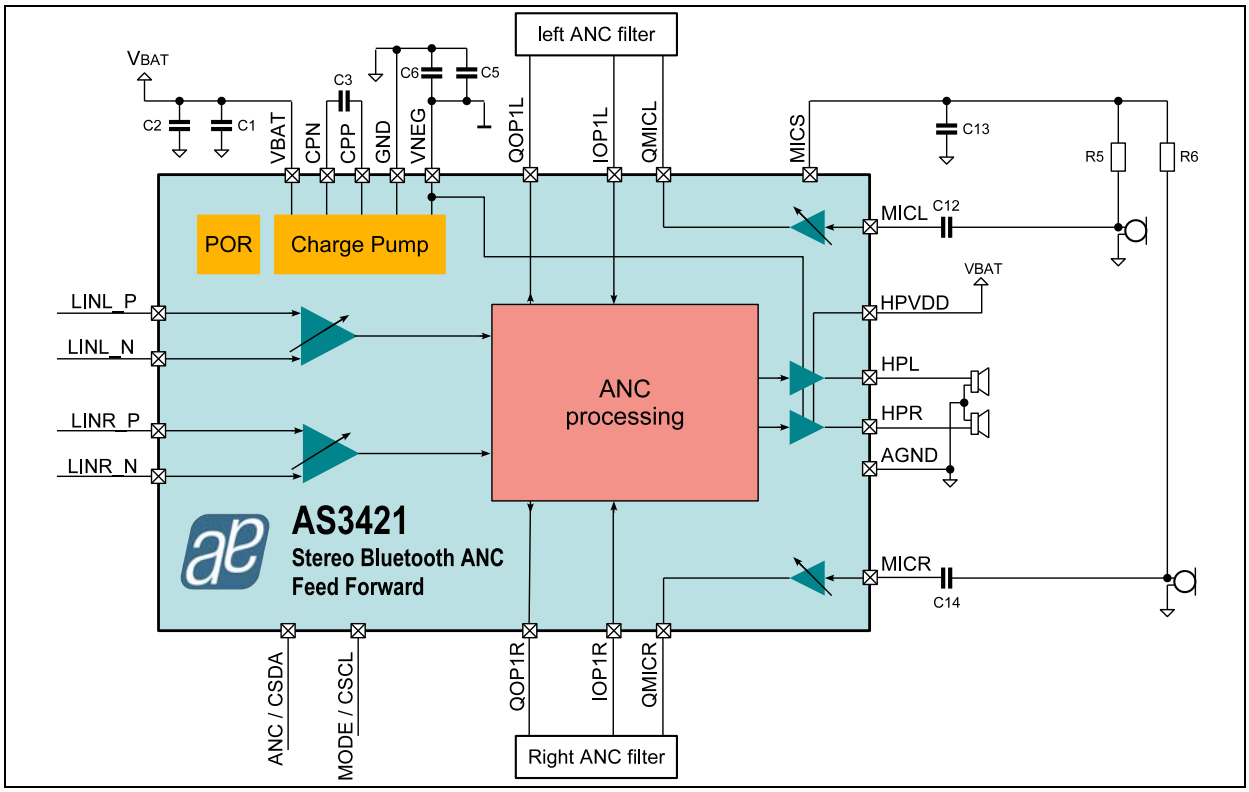
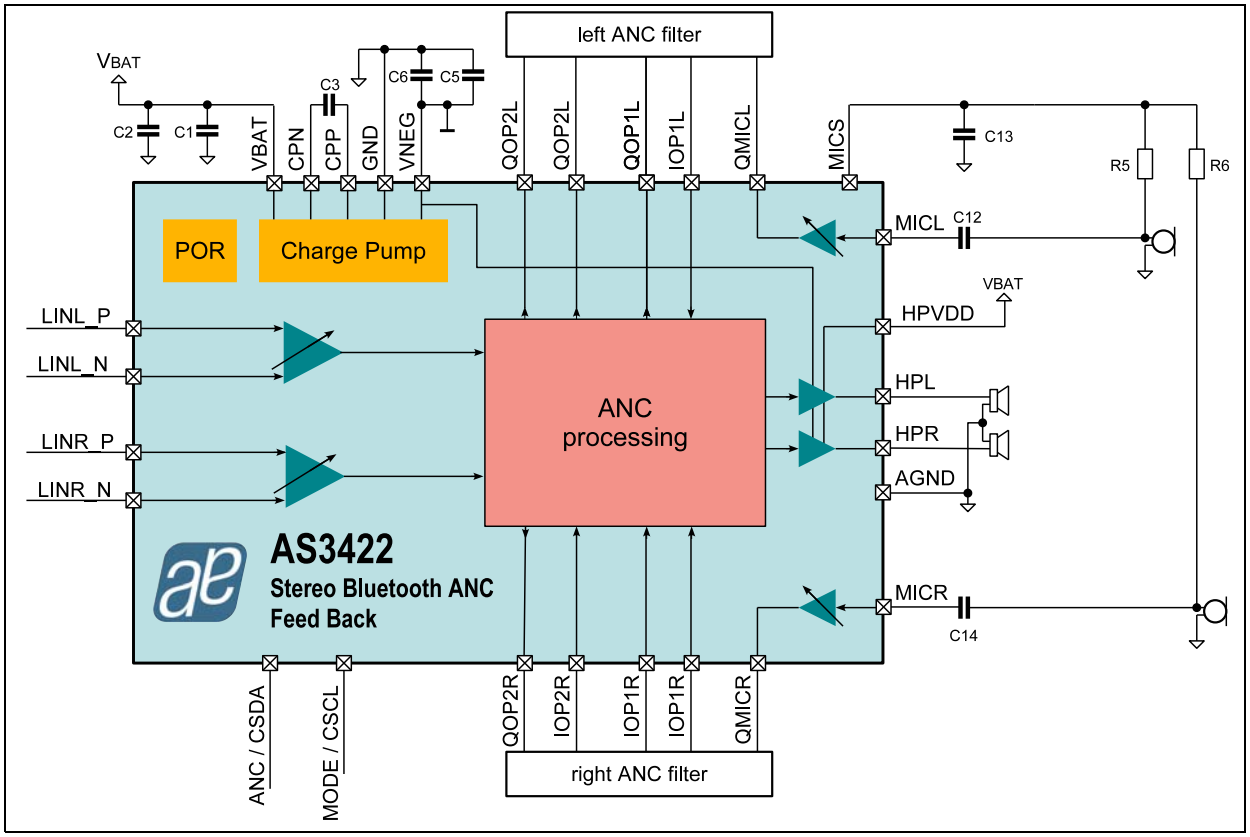


Figure 2. AS3422 Feed-Back Block Diagram

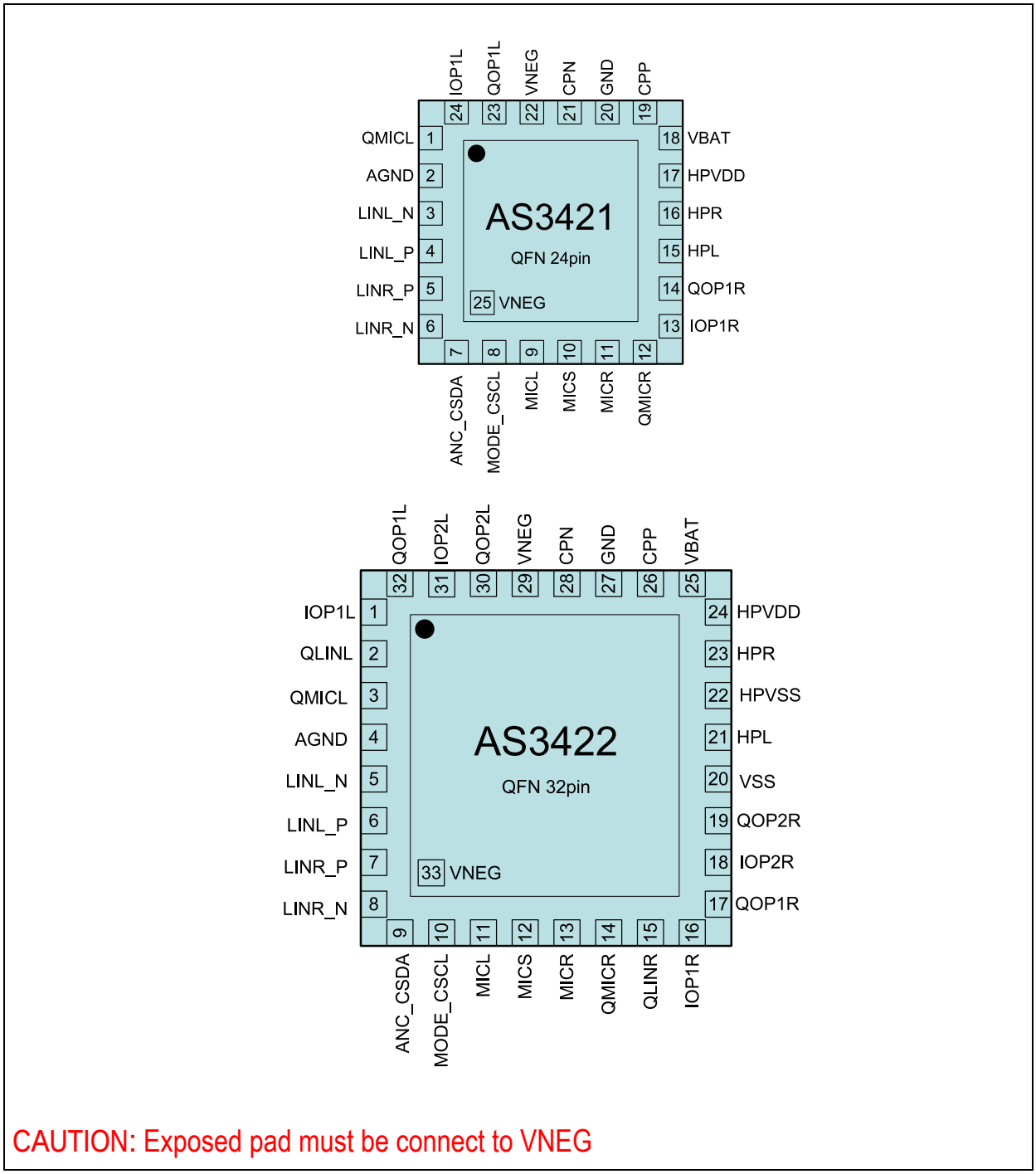


4 Contents

5 Pin Assignments

Note: Pin assignment may change in preliminary data sheets.

Figure 3. Pin Assignments (Top View)



CAUTION: Exposed pad must be connect to VNEG

5.1 Pin Descriptions

Note: Pin description may change in preliminary data sheets.

Table 1. Pin Description for AS3421 AS3422

Pin Name	Pin Number		Type	Description
	AS3421	AS3422		
IOP1L	24	1	ANA IN	Filter OpAmp1 Input Left Channel
QLINL		2	ANA OUT	Line In Gain Stage Output Left Channel
QMICL	1	3	ANA OUT	MIC Gain Stage Output Right Channel
AGND	2	4	ANA IN	Analog Reference
LINL_N	3	5	ANA IN	Negative Line In pin of Left Channel
LINL_P	4	6	ANA IN	Positive Line In pin of Left Channel
LINR_P	5	7	ANA IN	Positive Line In pin of Right Channel
LINR_N	6	8	ANA IN	Negative Line In pin of Right Channel
ANC_CSDA	7	9	MIXED IO	Serial Interface Data ANC Pin (Enable/Disable ANC function)
MODE_CSCL	8	10	DIG IN	Mode Pin (Power Up/Down, Monitor) Serial Interface Clock
MICL	9	11	ANA IN	Microphone In Left Channel
MICS	10	12	ANA OUT	Microphone Supply
MICR	11	13	ANA IN	Microphone Input Right Channel
QMICR	12	14	ANA OUT	MIC Gain Stage Output Right Channel
QLINR		15	ANA OUT	Line In Gain Stage Output Right Channel
IOP1R	13	16	ANA IN	FilterOpAmp1 Input Right Channel
QOP1R	14	17	ANA IN	Filter OpAmp1 Output Right Channel
IOP2R		18	ANA IN	Filter OpAmp2 Input Right Channel
QOP2R		19	ANA OUT	Filter OpAmp2 Output Right Channel
VSS		20	SUP IN	VSS supply terminal
HPL	15	21	ANA OUT	Headphone Output Left Channel
HPVSS		22	SUP IN	Headphone amplifier VSS supply terminal
HPR	16	23	ANA OUT	Headphone Output Right Channel
HPVDD	17	24	SUP IN	Headphone VDD Supply
VBAT	18	25	SUP IN	Positive supply terminal of IC
CPP	19	26	ANA OUT	VNEG ChargePump Flying Capacitor Positive Terminal
GND	20	27	GND	VNEG ChargePump Negative Supply
CPN	21	28	ANA OUT	VNEG ChargePump Flying Capacitor Negative Terminal
VNEG	22	29	SUP IO	VNEG ChargePump Output
QOP2L		30	ANA OUT	Filter OpAmp2 Output Left Channel
IOP2L		31	ANA IN	Filter OpAmp2 Input Left Channel
QOP1L	23	32	ANA OUT	Filter OpAmp1 Output Right Channel
VNEG	25	33	SUP IN	Exposed Pad: Connect to VNEG

6 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Reference Ground				Defined as in GND
Supply terminals	-0.5	2.0	V	Applicable for pin VBAT, HPVDD
Ground terminals	-0.5	0.5	V	Applicable for pins AGND
Negative terminals	-2.0	0.5	V	Applicable for pins VNEG, VSS, HPVSS
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, HPVSS
Pins with protection to VBAT	VNEG -0.5	5.0 VBAT+0.5	V	Applicable for pins CPP, CPN
Pins with protection to HPVDD	VSS -0.5	5.0 HPVDD+0.5	V	Applicable for pins LINL_P/N, LINR_P/N, MICL/R, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx
other pins	VSS -0.5	5		Applicable for pins MICS, ANC_CSDA, MODE_CSCL
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous Power Dissipation	-	200	mW	P_T[1] for QFN16/24/32 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-2	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	3			Represents a max. floor life time of 168h
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

1. Depending on actual PCB layout and PCB used

7 Electrical Characteristics

VBAT = 1.0V to 1.8V, T_A = -20ºC to +85ºC. Typical values are at VBAT = 1.5V, T_A = +25ºC, unless otherwise specified. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
T_A	Ambient Temperature Range		-20	+85	°C
Supply Voltages					
GND	Reference Ground		0	0	V
VBAT, HPVDD	Battery Supply Voltage	normal operation with MODE pin high	1.0	1.8	V
		Two wire interface operation	1.4	1.8	V
VNEG	ChargePump Voltage		-1.8	-0.7	V
VSS	Analog neg. Supply Voltages HPVSS, VSS, VNEG		-1.8	-0.7	V
V_{DELTA-}	Difference of Ground Supplies GND, AGND	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1	0.1	V
$V_{DELTA--}$	Difference of Negative Supplies VSS, VNEG, HPVSS	Charge pump output or external supply	-0.1	0.1	V
V_{DELTA+}	Difference of Positive Supplies	VBAT-HPVDD	-0.25	0.25	V
Other pins					
V_{MICS}	Microphone Supply Voltage	MICS	0	3.6	V
V_{HPVDD}	Pins with diode to HPVDD	MICL/R, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx	VSS	3.6	V
V_{VBAT}	Pins with diode to VBAT	CPP, CPN	VNEG	VBAT	V
$V_{CONTROL}$	Control Pins	MODE_CSCL, ANC_CSDA	VSS	3.7	V
V_{TRIM}	Line Input & Application Trim Pins	LINL_P, LINL_N, LINR_P, LINR_N	VNEG -0.5 or -1.8	HPVDD +0.5 or 1.8	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{leak}	Leakage current	VBAT<0.8V			20	µA
		VBAT<0.6V			10	µA
Block Power Requirements @ 1.5V VBAT						
I_{OFF}	Off mode current	MODE pin low, device switched off		1		µA
I_{SYS}	Reference supply current	Bias generation, oscillator, ADC6, VNEG		0.25		mA
I_{LIN}	LineIn gain stage current	no signal, stereo		0.5		mA
I_{MIC}	Mic gain stage current	no signal, stereo		2.10		mA
I_{HP}	Headphone stage current	no signal		1.70		mA
I_{MICS}	MICS charge pump current	no load		30		µA
I_{MIN}	Minimal supply current	Sum of all above blocks		4.6		mA
I_{OP1}	OP1 supply current	no load		0.64		mA
I_{OP2}	OP2 supply current	no load		0.64		mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{MICB}	Microphone bias current	200µA per microphone via charge pump		0.9		mA
I_{PB}	Low Power Playback Mode	V_{BAT} = 1.8V		2,8		mA
		V_{BAT} = 1.5V		2,5		mA
		V_{BAT} = 1.0V		2		mA

8 Typical Operating Characteristics

V_{BAT} = +1.5V, C_1=100nF, C_2=10µF, C_3=1µF, C_6=100nF, C_5=10µF, C_{13}=10µF, C_{12}=2.2µF, C14=2.2µF T_A = +25ºC and HP_MUX_OTP set to '3' unless otherwise specified.

Figure 4. THD+N vs. Pout; Line to HPH; 16Ω single ended stereo

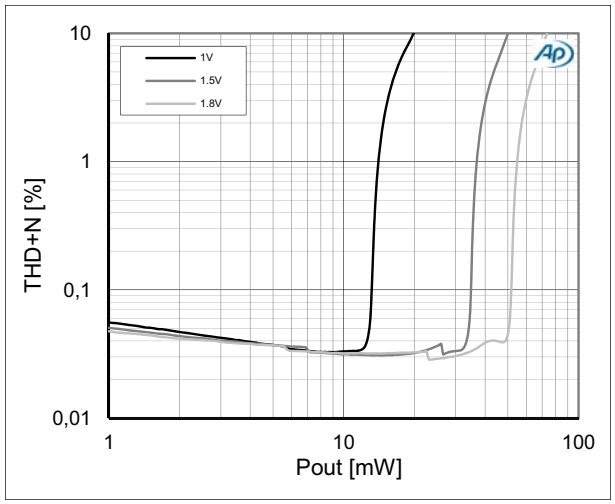


Figure 5. THD+N vs. Pout; Line to HPH; 32Ω single ended stereo

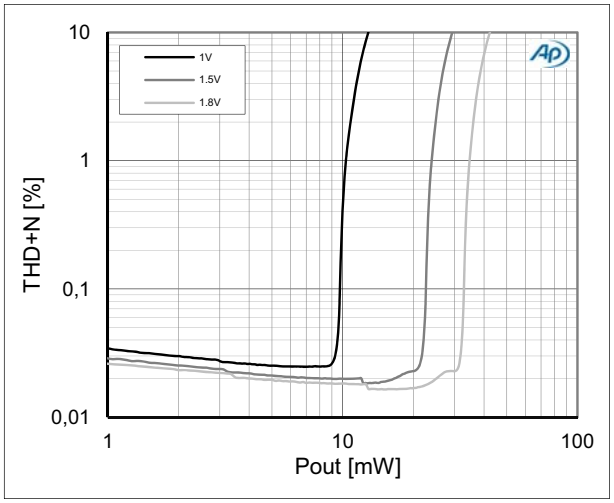


Figure 6. THD+N vs. f; Line to HPH; 1mW load per channel

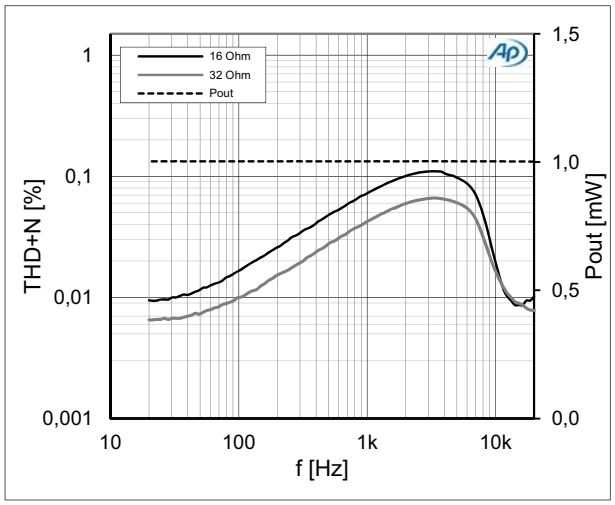


Figure 7. THD+N vs. f; Line to HPH; 10mW load per channel

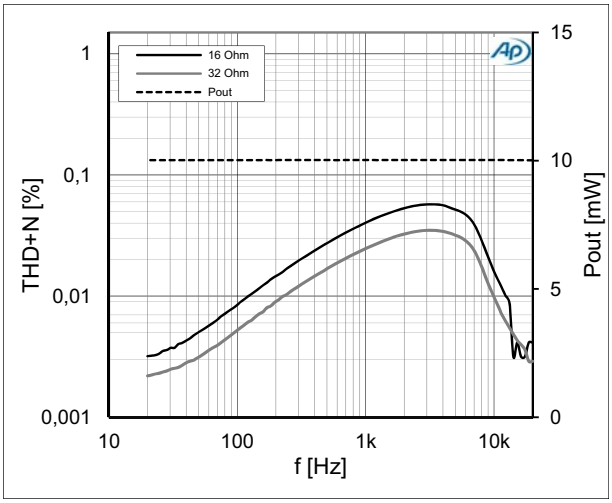


Figure 8. THD+N vs. f; 20mW and 30mW per channel

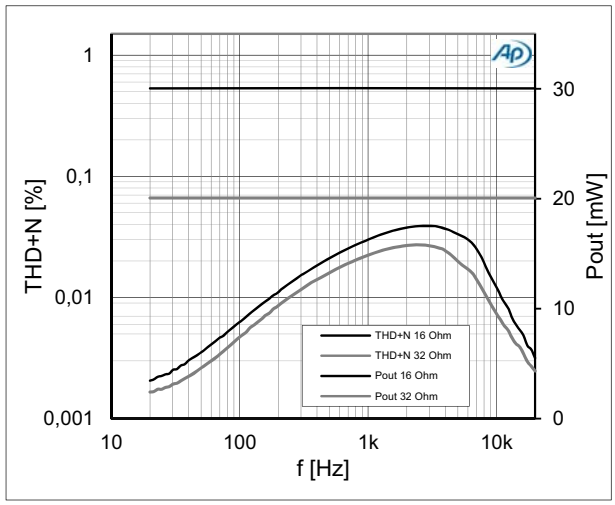


Figure 9. Frequency Response 30mW@16Ω, Line to HPH

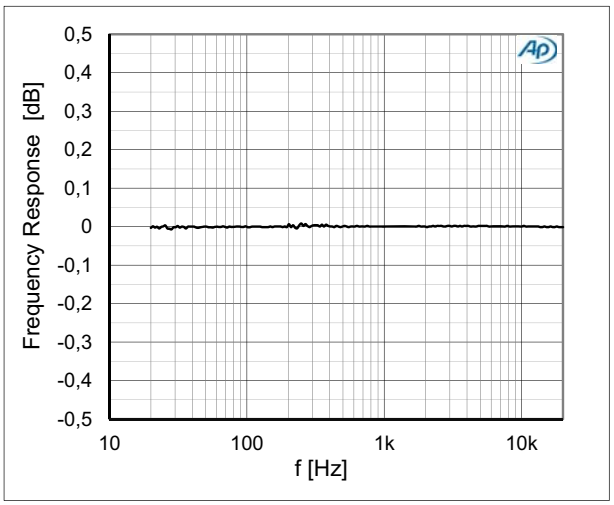


Figure 10. Frequency Response 20mW@32Ω, Line to HPH

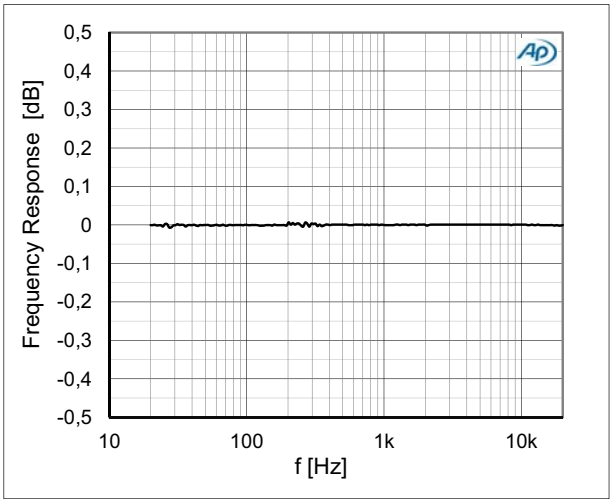


Figure 11. Microphone Supply FFT

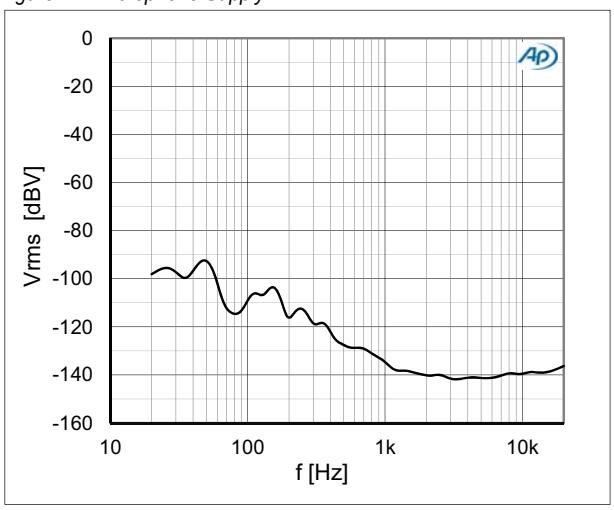


Figure 12. VNEG CP Voltage vs. CP load current with different VBAT supply voltages

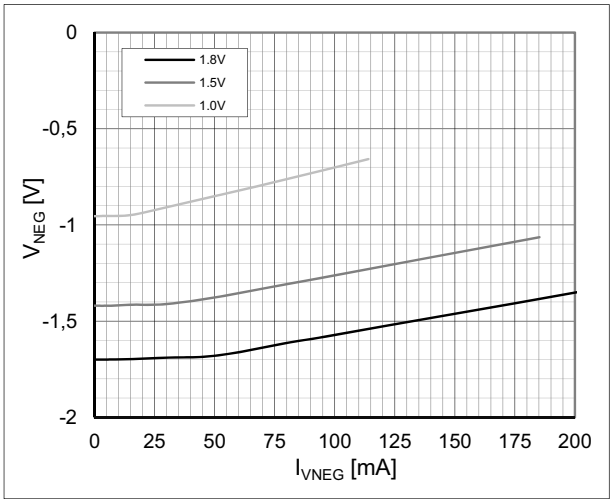


Figure 13. VNEG Efficiency vs.IVNEG with different VBAT supply voltages

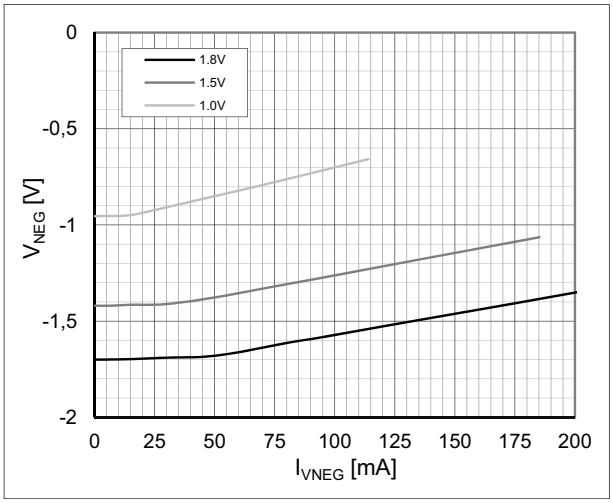


Figure 14. VMIC_OUT vs. IMIC_OUT

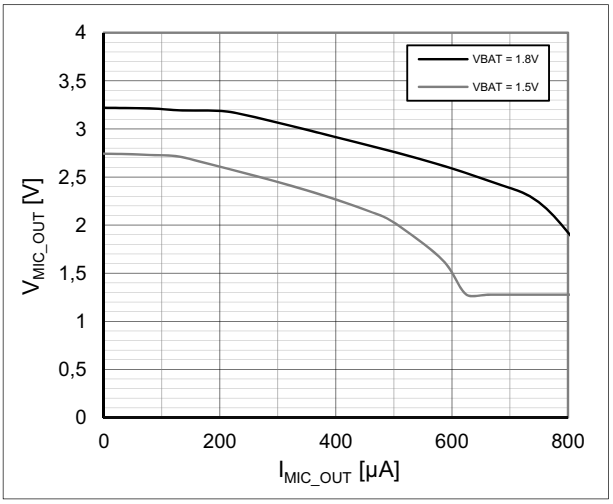


Figure 15. Typical Performance Data, Feed Forward configuration with an over the ear headset

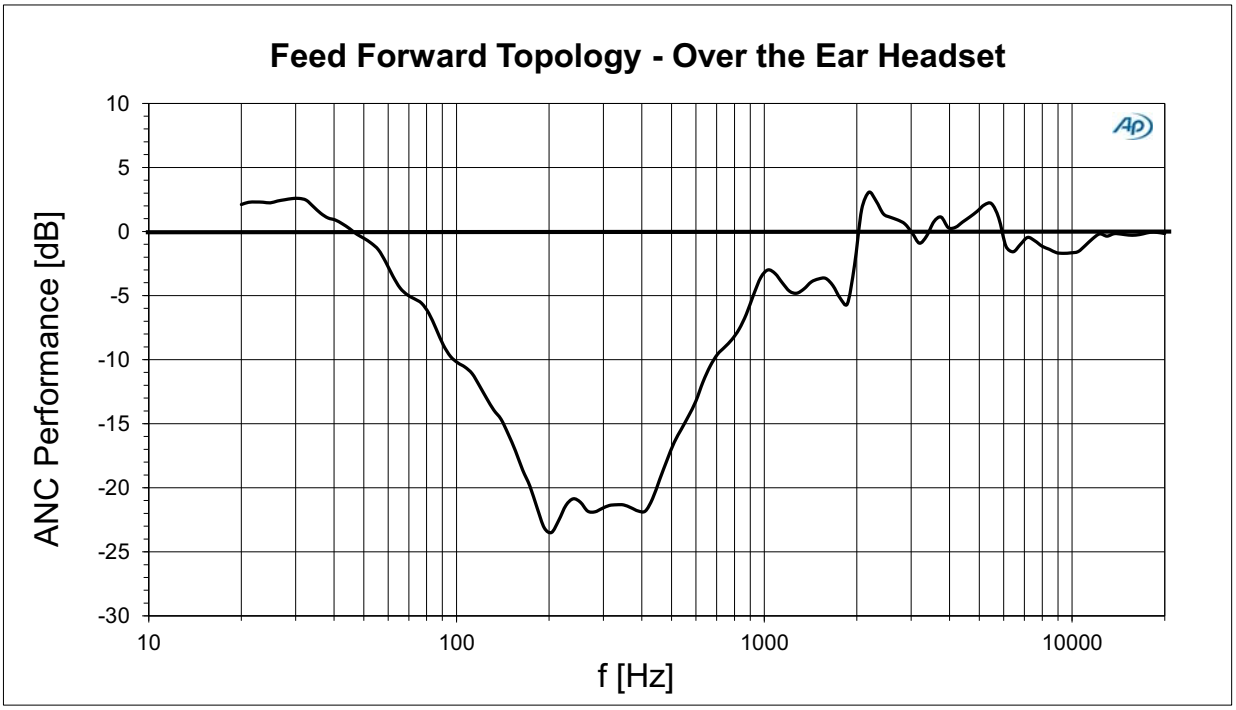
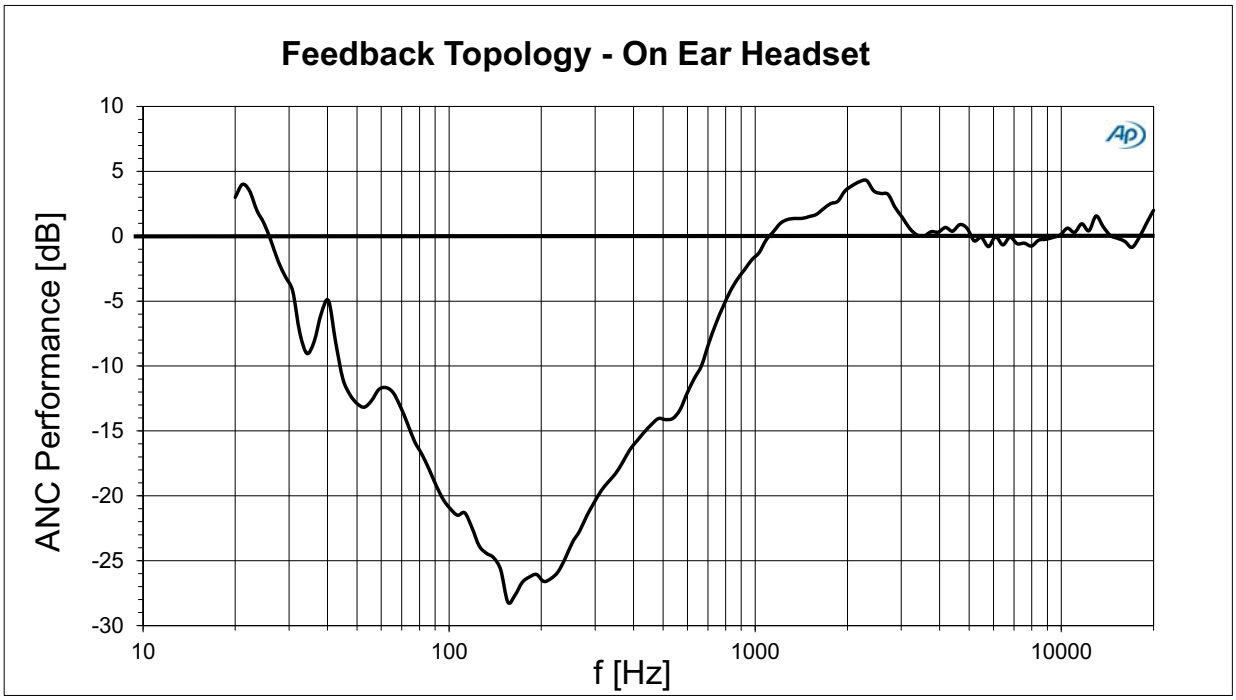


Figure 16. Typical Performance Data, Feedback configuration with an on ear headset



9 Detailed Description

This section provides a detailed description of the device related components.

9.1 Audio Line Input

The chip features one line input. The blocks can work in mono differential or in stereo single ended mode.

In addition to the 12.5-25kΩ input impedance, LineIn has a termination resistor of 10kΩ which is also effective during MUTE to charge eventually given input capacitors.

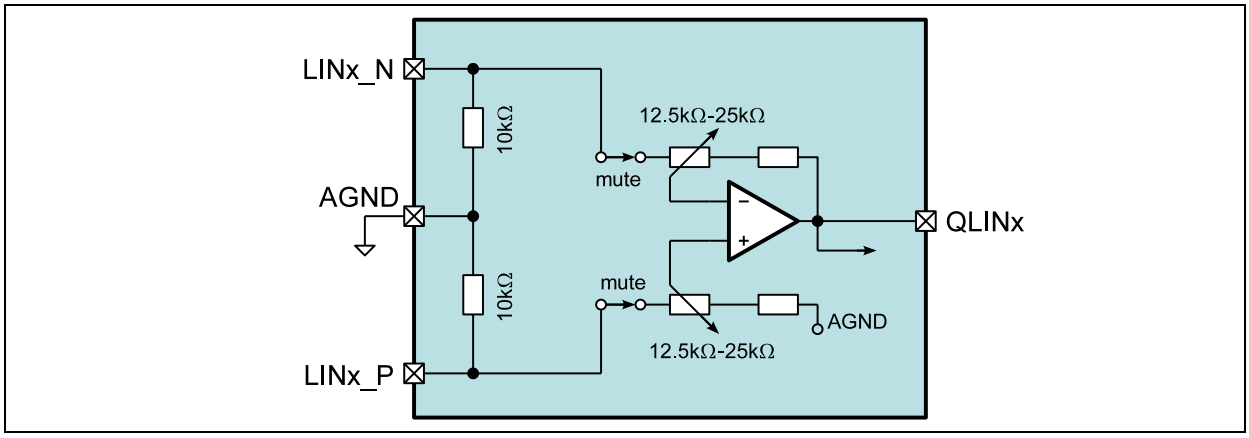
9.1.1 Gain Stage

The Line In gain stage is designed to have 63 gain steps of 0.75dB with a max gain of 0dB plus MUTE per default. By setting the bit Line Gain +3dB in register 0x33 the gain range can be changed from -46.5dB....0dB to -43.5dB ....+3dB.

In default, the gain will be ramped up from MUTE to 0dB during startup. There is a possibility to make the playback volume user controlled by the VOL pin with an ADC converted VOL voltage or UP/DOWN buttons. If the device is configured to control the line input volume via push-buttons the device ramps the gain from -46.5dB to 0dB if no button is pressed. If a user presses a button while ramping up the ramping mechanism will be stopped automatically.

In monitor mode, the gain stage can be set to an fixed default attenuation level for reducing the loudness of the music. To avoid unwanted pop noise in this special mode the internal state machine support very smooth gain fading to avoid unwanted acoustic effects.

Figure 17. Fully Differential Stereo Line Inputs



9.1.2 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 4. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level			0.6* VBAT	VBAT	V_{PEAK}
R_{LIN}	Input Impedance	0dB gain (12.5k // 10k)		5.6		kΩ
		-46.5dB gain (25k // 10k)		7.2		kΩ
		MUTE		10		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-46.5		+0	dB
	Gain Steps	Discrete logarithmic gain steps		0.75		dB
	Gain Step Accuracy			0.5		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB

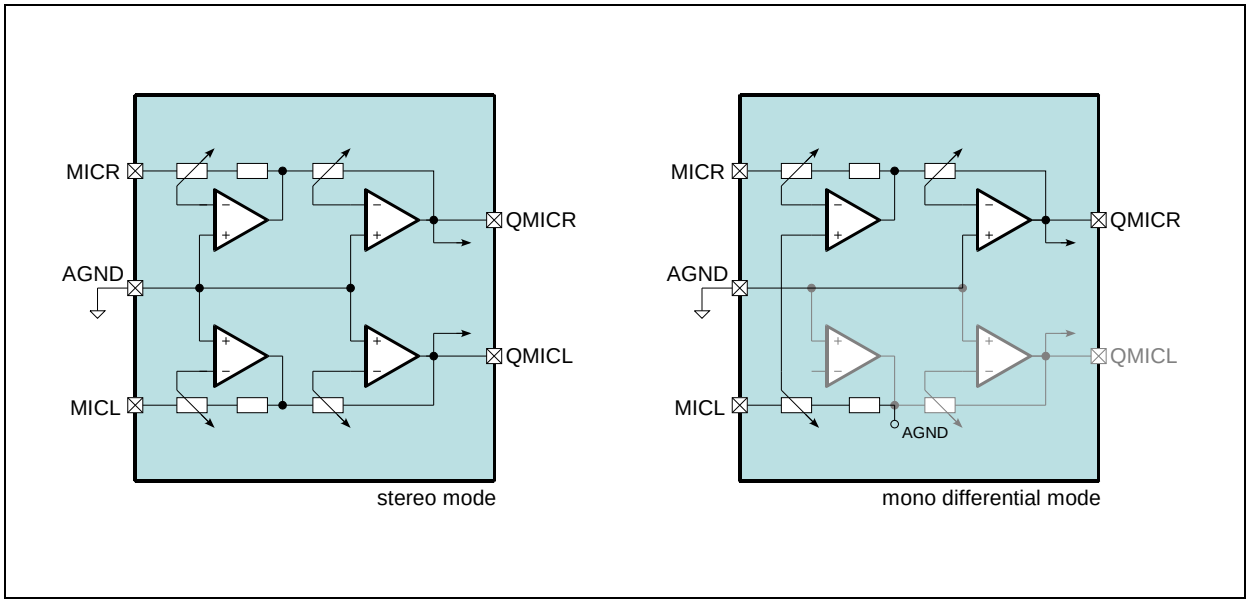
Table 4. Line Input Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Δ_{ALIN}	Gain Ramp Rate	Button Mode, Tinit=400ms		80		ms/step
		Monitor Mode		8		
V_{ATTACK}	Limiter Activation Level	HPL/R start of neg. clipping				V_{PEAK}
V_{DECAY}	Limiter Release Level	HPL/R		VNEG +0.3		V_{PEAK}
t_{ATTACK}	Limiter Attack Time			4		µs
t_{DECAY}	Limiter Decay Time			8		ms

9.2 Microphone Input

The AFE offers two microphone inputs and one low noise microphone voltage supply (microphone bias). The inputs can be switched to single ended or differential mode.

Figure 18. Microphone Input



9.2.1 Gain Stage & Limiter

The Mic Gain Stage has programmable Gain within -11.25dB…+36dB in 128 steps of 0.375dB.

As soft-start function is implemented for an automatic gain ramping implemented with steps of 4ms to fade in the audio at the end of the start-up sequence.

A limiter automatically attenuates high input signals. The AGC has 127 steps with 0.375dB with a dynamic range of the full gain stage. In some design it is necessary to switch of the AGC functionality. This can be done in register 0x17 by setting bit '1'.

In monitor mode, the gain stage can be set to an fixed (normally higher) gain level or be controlled by the VOL pin.

9.2.2 Microphone Supply

The MICS charge pump is providing a proper microphone supply voltage for low supply voltage supply. The integrated microphone supply supports basically 3 different modes.

The first mode, also called SWITCH-MODE, for 1.8V supply is to have a direct connection with an integrated switch from VBAT to MICS. The microphone supply pin of AS3421/22 is in this mode directly connected to V_{BAT}. For some applications a 1.8V microphone supply is high enough to operate a microphone properly. This mode is more commonly used in devices with a fixed power supply like in Bluetooth headsets. The internal microphone charge pump is switched off in this mode. This can help also reducing the external filter capacitors for the microphone supply. Please mind that the sensitivity of your microphone can be reduced in this mode.

The second mode, with the name CHAREGPUMP_MODE, is the most commonly used mode which is per default enabled. In this mode the internal charge pump is enabled. The charge pump doubles the supply voltage of AS3421/22 with a high output impedance of the charge pump in order to make external passive filters more effective. If doubling the supply voltage is not enough the microphone supply can be switched to a special regulated mode which increases the output voltage but with a little bit higher output noise. This setting can be found in register 0x35.

The third mode is the OFF MODE. This mode allows the user to switch of the microphone supply if not needed (e.g. playback without ANC)

9.2.3 Parameter

VBAT=1.5V, T_A= 25ºC unless otherwise specified.

Table 5. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MIC} = 24dB		40		mV_P
$V_{MICIN}1$		A_{MIC} = 30dB		20		mV_P
$V_{MICIN}2$		A_{MIC} = 36dB		10		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			5		pF
A_{MIC}	Programmable Gain		-11.25		+36	dB
	Gain Steps	Discrete logarithmic gain steps		0.375		dB
	Gain Step Precision			0.15		dB
Δ_{AMIC}	Gain Ramp Rate	Tinit=64ms		4		ms/step
V_{ATTACK}	Limiter Activation Level	V_{PEAK} related to VBAT or VNEG		0.67		1
V_{DECAY}	Limiter Release Level			0.4		1
$A_{MICLIMIT}$	Limiter Gain Overdrive	127 @ 0.375dB		36		dB
t_{ATTACK}	Limiter Attack Time			5		µs/step
$t_{DECAY-DEB}$	Limiter Decay Debouncing Time			64		ms
t_{DECAY}	Limiter Decay Time			4		ms/step
V_{MICS}	Microphone Output Voltage	no output load		2.7		V
I_{MICS}	Microphone Supply Current	no output load		30		µA
R_{OUT_CP}	CP Output Resistance	400µA load		900		Ω
I_{MIC_MIN}	Microphone Output Current	Recommended minimum microphone output current @ Vbat = 1.5V		170		µA
		Recommended minimum microphone output current @ Vbat = 1.8V		300		µA
I_{MIC_MAX}	Microphone Output Current	Recommended maximum microphone output current @Vbat = 1.5V		500		µA
		Recommended maximum microphone output current @Vbat = 1.8V		700		µA

9.3 Headphone Output

The headphone output is a true ground output using VNEG as negative supply, designed to provide the audio signal with 2x12mW @ 16Ω-64Ω, which are typical values for headphones. It is also capable to operate in bridged mode for higher impedance (e.g. 300Ω) headphone. In this mode the left output is carrying the inverted signal of the right output shown in Figure 20.

Figure 19. Headphone Output Single Ended Mode

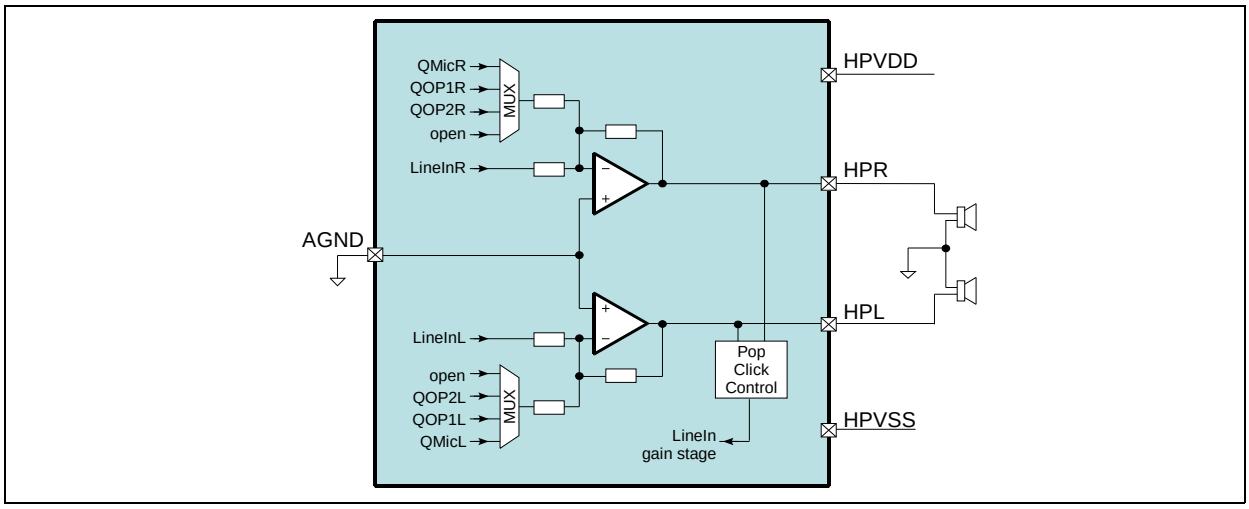
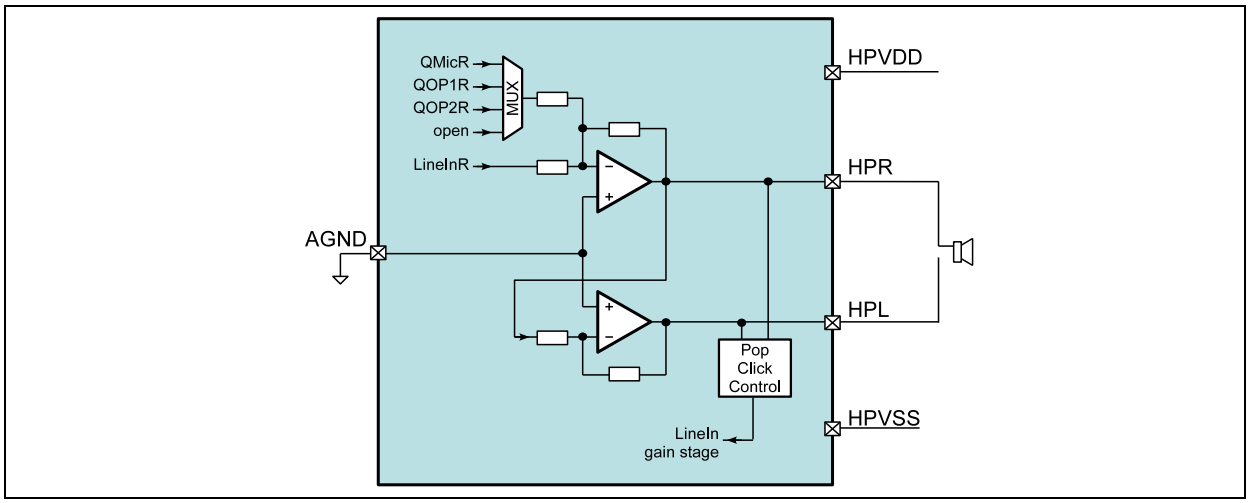


Figure 20. Headphone Output Differential Mode



9.3.1 Input Multiplexer

The signal from the line-input gain stage gets summed at the input of the headphone stage with the microphone gain stage output, the first filter opamp output or the second filter opamp output. The microphone gain stage output is used per default. It is also possible to playback without ANC by only using the line-input gain stage with no other signal on the multiplexer.

For the monitor mode, the setting of this input multiplexer can be changed to another source, normally to the microphone.

9.3.2 No-Pop Function

The No-Pop startup of the headphone stage takes 60ms to 120ms dependent on the supply voltage.

9.3.3 No-Clip Function

The headphone output stage gets monitored by comparator stages which detect if the output signal starts to clip.

This signal is used to reduce the LineIn gain to avoid distortion of the output signal. A hystereses avoids jumping between 2 gain steps for a signal with constant amplitude.

9.3.4 Over-Current Protection

The over-current protection has a threshold of 150-200mA and a debouncing time of 8µs. The stage is forced to OFF mode in an over-current situation. After this, the headphone stage tries to power up again every 8ms as long as the over-current situation still exists or the stage is turned off manually.

9.3.5 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 6. Headphone Output Parameter

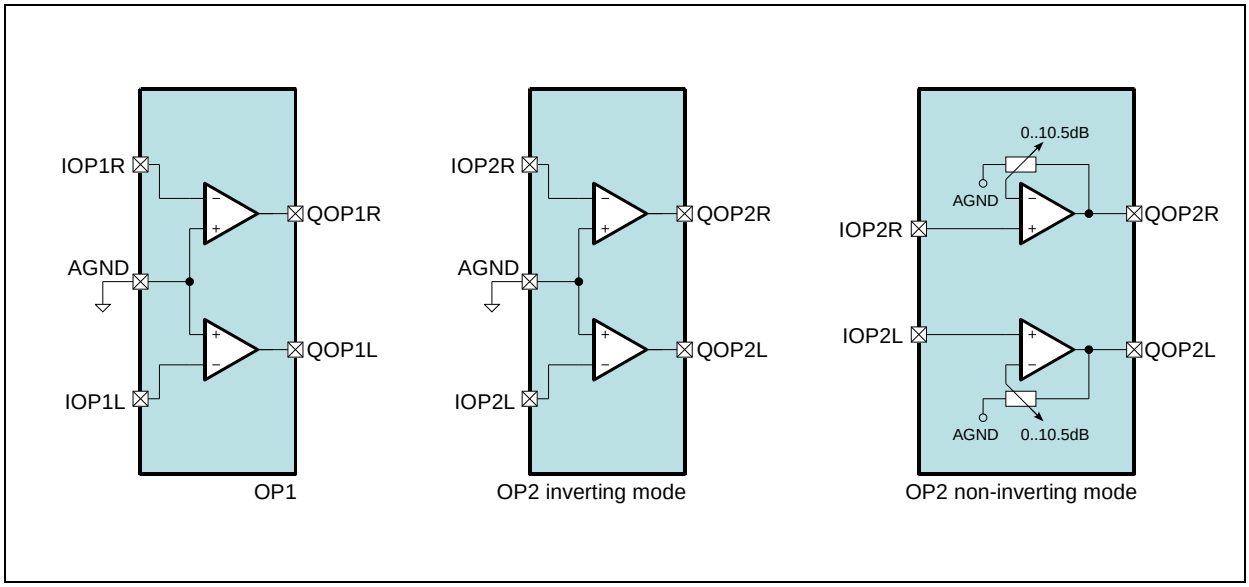
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	Stereo mode	16			Ω
C_{L_HP}	Load Capacitance	Stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=64Ω	12			mW
		RL=32Ω	24			mW
		RL=16Ω	34			mW
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB

9.4 Operational Amplifier

While AS3421 offers only one operational amplifier for feed-forward ANC, AS3422 features an additional operational amplifier stage to support feed-back ANC or any other additional needed filtering.

Both operational amplifiers stages can be activated and used individually. While OP1 stage is always configured as inverting amplifier, OP2 stage can be also switched to a non-inverting mode with an adjustable gain of 0...+10.5dB.

Figure 21. Operational Amplifiers



9.4.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 7. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_OP}	Load Impedance	Single ended	1			kΩ
C_{L_OP}	Load Capacitance	Single ended			100	pF
GBW_{OP}	Gain Band Width			4.3		MHz
V_{OS_OP}	Offset Voltage				6	mV
V_{EIN_HP}	Equivalent Input Noise	200Hz-20kHz		2.6		µV

9.5 SYSTEM

The system block handles the power up and power down sequencing, as well as, the mode switching.

9.5.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Table 8. Power UP Conditions

#	Source	Description
1	MODE_CSCL pin	In stand-alone mode, MODE pin has to be driven high to turn on the device
2	I2C start	In I2C mode, a I2C start condition turns on the device

The chip automatically shuts off if one of the following conditions arises:

Table 9. Power DOWN Conditions

#	Source	Description
1	MODE pin	Power down by driving MODE_CSCL pin to low
2	SERIF	Power down by SERIF writing 0h to register 20h bit <0>
3	Low Battery	Power down if VBAT is lower than the supervisor off-threshold
4	VNEG CP OVC	Power down if VNEG is higher than the VNEG off-threshold

9.5.2 Start-up Sequence

The start-up sequence depends on the used mode.

In stand-alone mode the sequence runs automatically, in I2C mode(I2C MODE bit has to be pre-trimmed) the sequence runs till a defined state and waits then for an I2C command. Either the automatic sequence is started by setting the CONT_PWRUP bit in addition to the PWR_HOLD bit. If only the PWR_HOLD is set all enable bits for headphone, microphone, etc have to be set manually.

Figure 22. Stand-Alone Mode Start-Up Sequence

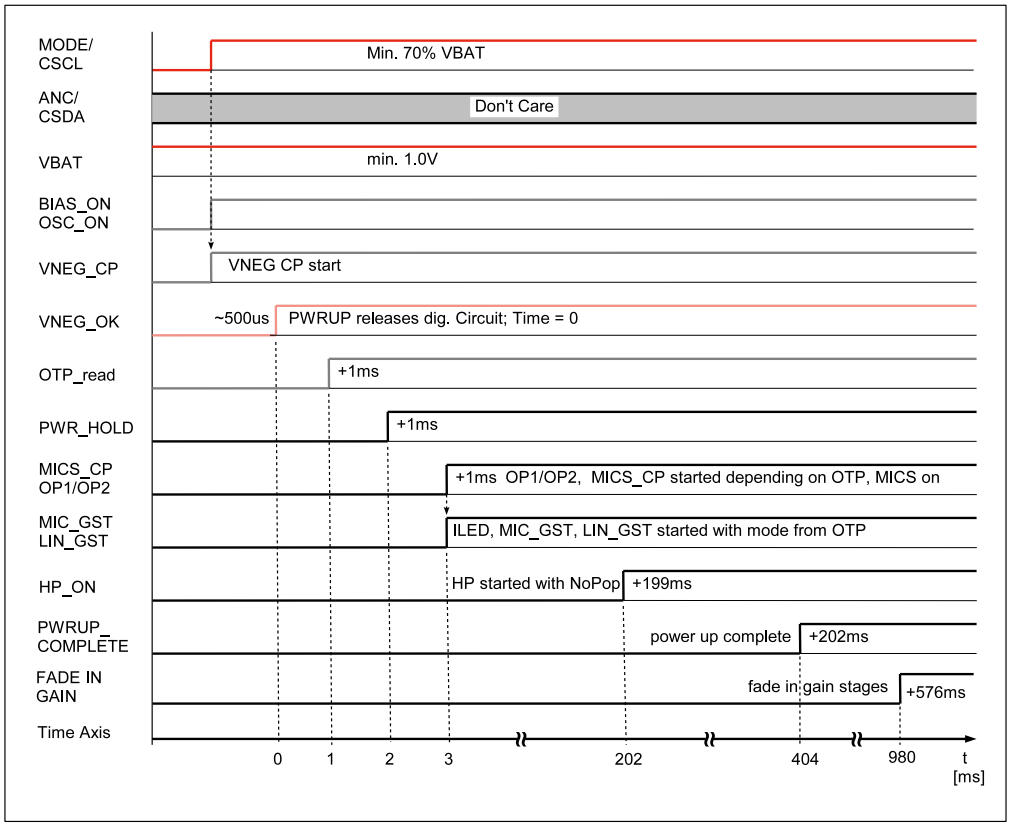
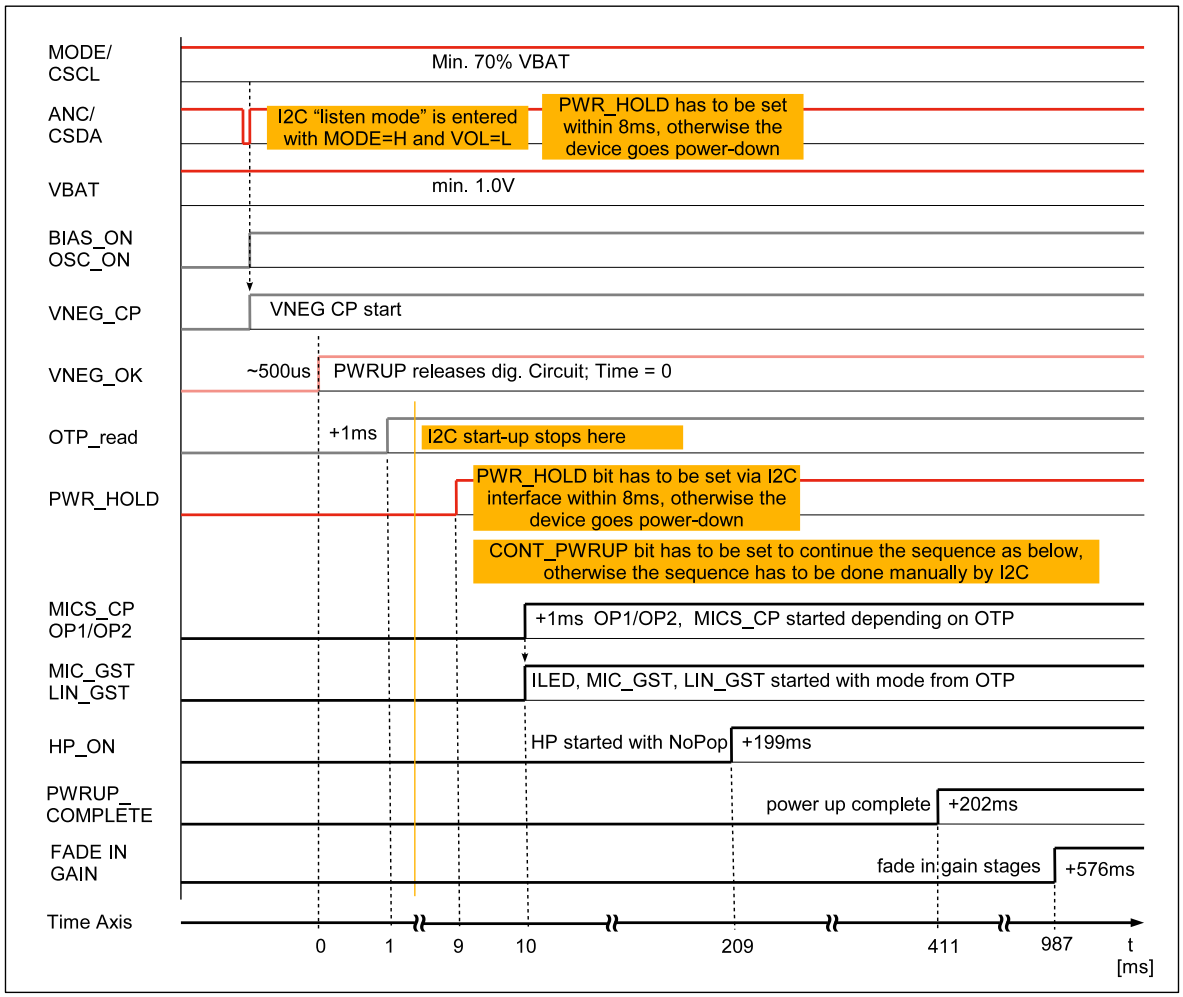


Figure 23. I2C Mode Start-Up Sequence



The total start-up time (including fade-in of the gain stages) can be reduced to 600ms by OTP setting.

9.5.3 MODE_CSCL Switching

When the chip is in stand-alone mode (no I2C control), the mode can be switched with different levels on the MODE pin.

Table 10. MODE_CSCL Operation Modes

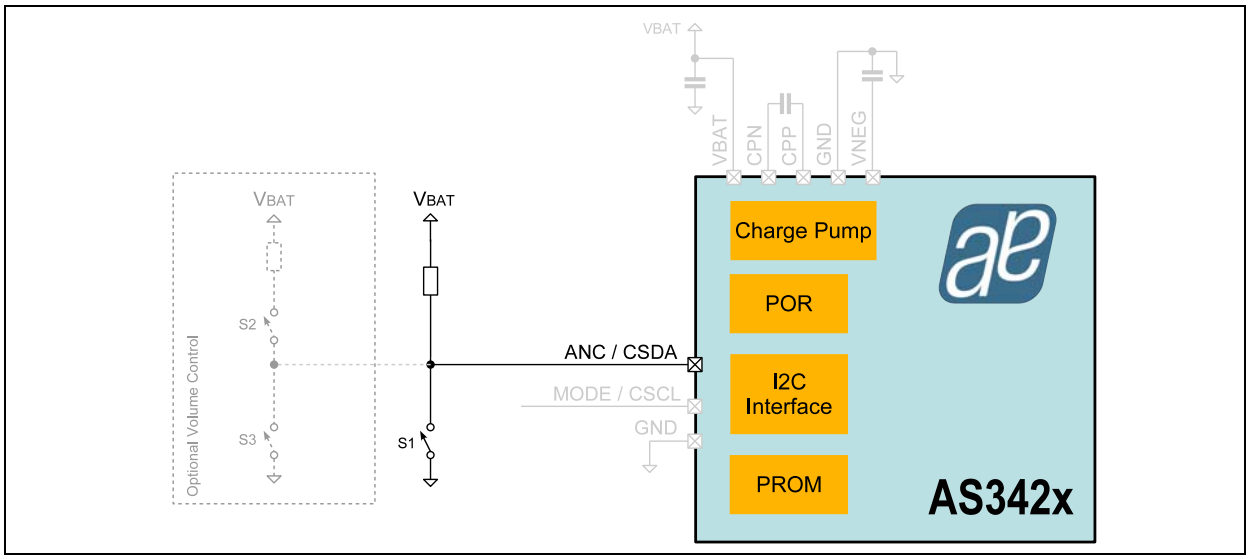
MODE	MODE_CSCL pin	Description
OFF	LOW (VSS)	Chip is turned off
ANC	HIGH (VBAT)	Chip is turned on and active noise cancellation is active
MONITOR	VBAT/2	Chip is turned on and monitor mode is active In Monitor mode, a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. This volume can be either fixed or be controlled by the VOL input. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source. In addition, the LineIn gain can be lowered to reduce the loudness of the music currently played back.

In I2C mode, the monitor mode can be activated be setting the corresponding bit in the system register.

9.5.4 ANC_CSDA Switching

For Bluetooth applications it is sometimes a requirement to switch off the ANC function while listening to music or having a phone call. Because the fully differential audio outputs of the Bluetooth chip are directly connected to the line input of the AS3421/22 it is not possible to simply switch off the ANC chip to do music playback without ANC.In order to avoid an expensive bypass path with mechanical or electrical switches the AS3421/22 features a special low power audio playback mode. In this mode the device enters a low power mode where the ANC function is disabled and the blocks which are not necessary in this mode are automatically switched off to safe system power. This audio playback mode can be entered by simply pulling the ANC_SCDA pin to low.

Figure 24. ANC / CSDA Switching



An example how to implement this feature is shown in Figure 24. In default operation (ANC enabled) the ANC_CSDA pin is pulled high. If the device should enter the low power playback mode the pin is pulled low with the switch S1. Once the pin is pulled low the device enters after 200ms the playback mode. As long as the pin is low the device stays in the playback only mode. If the feature is for some reason not required it can also be disabled by setting the bit NO_PB_MODE_OTP in register 0x33. Once this bit is set to '1' the status of pin ANC_CSDA has no influence on the device any more.

Besides the low power playback mode the ANC_CSDA pin supports also volume control via push buttons. In order to enable this feature the corresponding bit VOL_BUTTON_MODE_OTP is register 0x33 has to be set to '1'. Once this bit is set, the device can not support the low power playback mode via ANC_CSDA pin any more. An example on how to connect the push buttons for volume control is shown in Figure 24 with the push buttons S2 and S3.

Table 11. ANC_CSDA Operation Modes

NO_PB_MODE_OTP Bit	VOL_BUTTON_MODE_OTP Bit	ANC_CSDA Pin	Description
0	0	high	Normal ANC operation
0	0	high -> low	Device enters low power playback mode
0	0	low -> high	Device returns to normal ANC operation
1	0	X	Normal ANC operation. No influence on operation via ANC_CSDA pin.
X	1	high	Volume Control Mode via Button - Volume up
X	1	High Imp.	Volume Control Mode via Button - No Volume change
X	1	low	Volume Control Mode via Button - Volume down

9.6 VNEG Charge Pump

The VNEG charge pump uses one external 1uF capacitor to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external dc-decoupling capacitors.

9.6.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 12. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	VBAT	1.0	1.5	1.8	V
V_{OUT}	Output voltage	VNEG	-0.7	-1.5	-1.8	V
C_{EXT}	External flying capacitor			1		µF

9.7 OTP Memory & Internal Registers

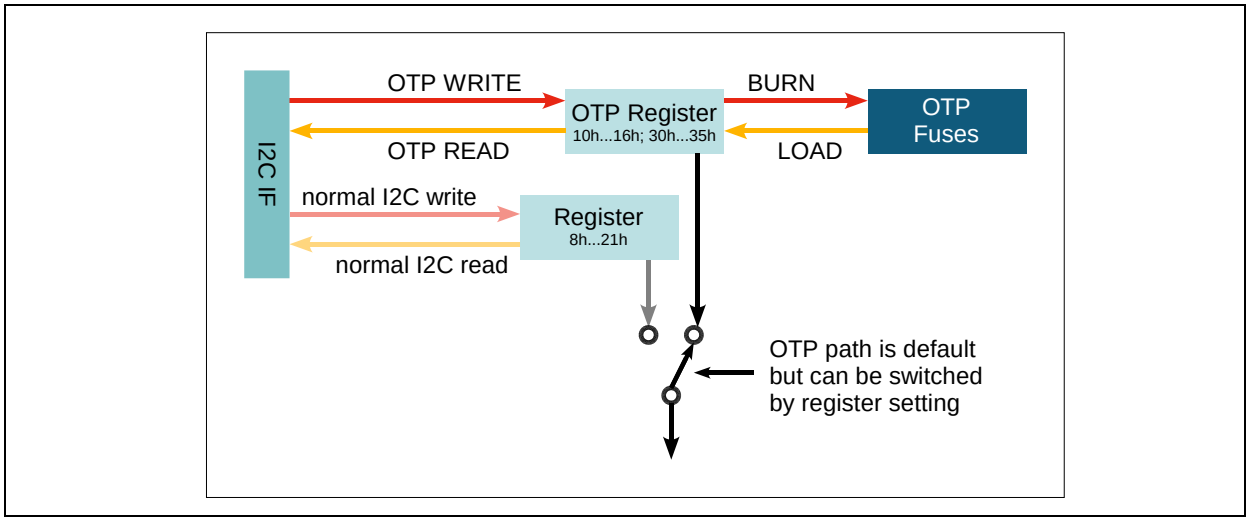
The OTP memory consists of OTP register and the OTP fuses.The OTP register can be written as often as wanted but will lose the content on power off. The OTP fuses are intended to store basic chip configurations as well as the microphone gain settings to optimize the ANC performance and get rid of sensitivity variations of different microphones. Burning the fuses can only be done once and is a permanent change, which means the fuses keep the content even if the chip is powered down. This AS3421/22 offers 4 register set for storing the microphone gain making it possible to change the gain 3 times for re-calibration or other purposes.

When the chip is controlled by a microcontroller via I2C, the OTP memory don't has to be used. The chip configuration can be stored in the flash memory of the Bluetooth- or wireless chipset.

9.7.1 Register & OTP Memory Configuration

Figure 25 is showing the principal register interaction.

Figure 25. Register Access



Registers 0x8, 0x9, 0xA, 0xB, 0xC and 0x21 have only effect when the corresponding "REG_ON" bit is set, otherwise the chip operates with the OTP Register settings which are loaded from the OTP fuses at every start-up.

All registers settings can be changed several times, but will loose the content on power off. When using the I2C mode, the chip configuration has to be loaded from the micro controller after every start-up. In stand alone mode the OTP fuses have to be programmed for a permanent change of the chip configuration.

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, but only additional unprogrammed "0"-bits can be programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation.

The OTP memory can be accessed in the following ways:

LOAD Operation. The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.

WRITE Operation. The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.

READ Operation. The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

BURN Operation. The BURN operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for burning the fuses.

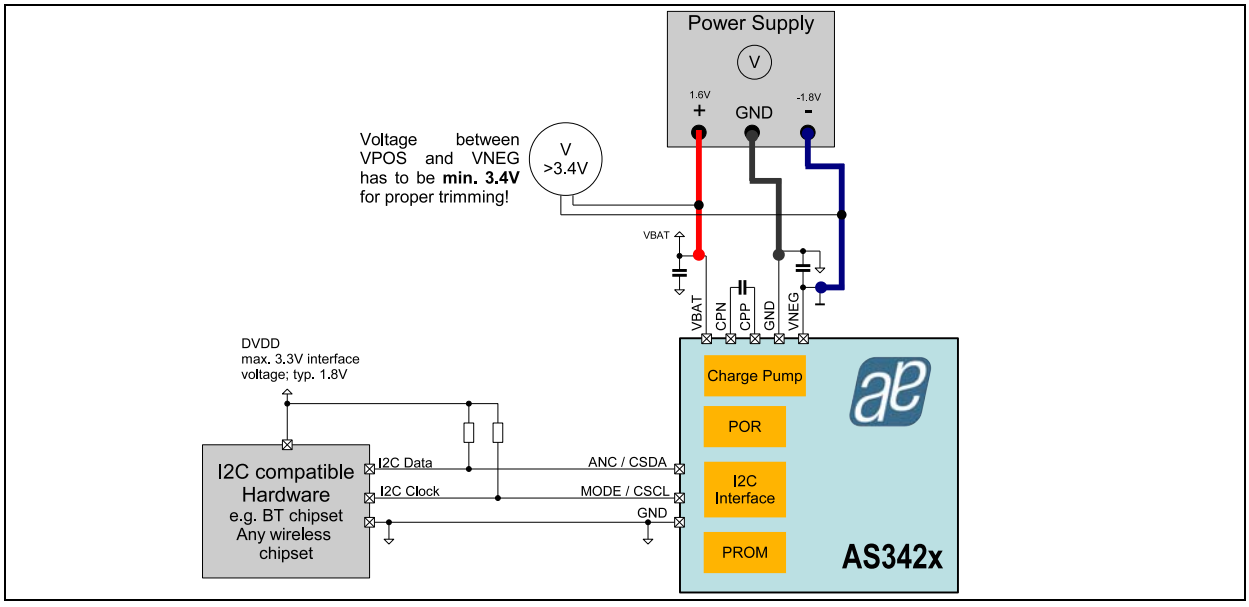
Attention: If you once burn the OTP_LOCK bit, no further programming, e.g. setting additional "0" to "1", of the OTP can be done.

For production, the OTP_LOCK bit must be set to avoid an unwanted change of the OTP content during the lifetime of the product.

9.7.2 OTP Fuse Burning

As many wireless applications like Bluetooth single chip solutions support programmable solutions as well as ROM versions it is in ROM versions necessary to store microphone gain compensation data and the general ANC configuration inside the ANC chip because there is not other way to configure the ANC chip during startup. In order to guaranty successful trimming of AS3421/22 it is necessary to provide a decent environment for the trimming process. In Figure 26 a principal block diagram is shown for trimming the AS3421/22 properly in production.

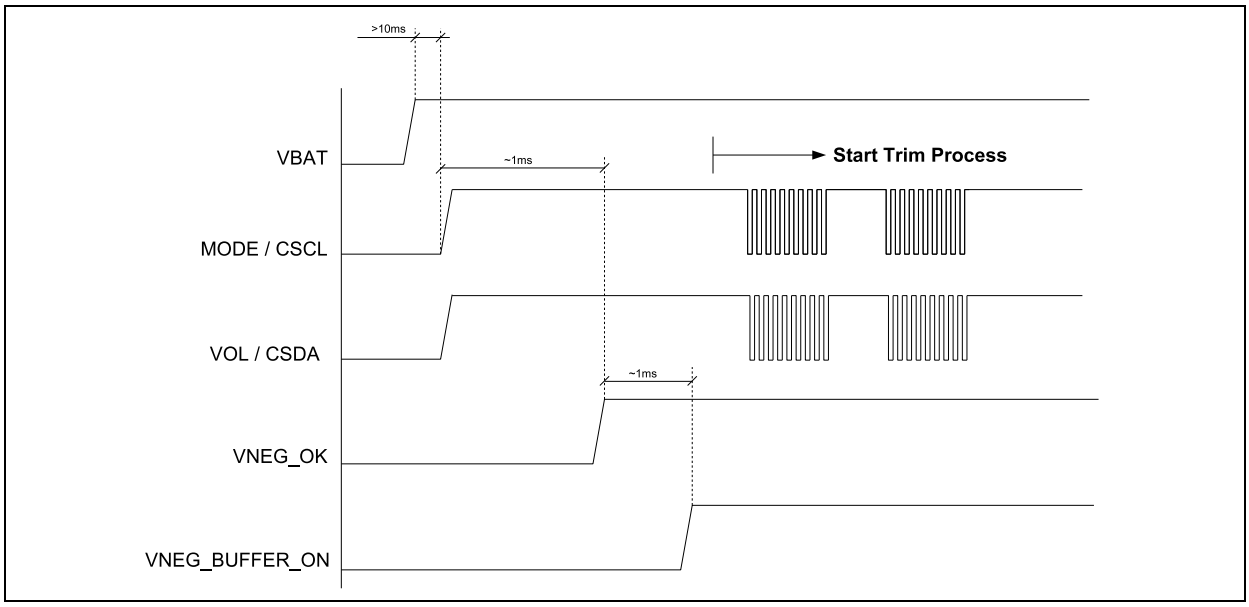
Figure 26. Block Diagram for Production Environment



The most important block is the external power supply. Usually it is possible to trim the AS3421/22 with a single supply voltage of min. 1.7V in laboratory environment but as soon as it comes to mass production we highly recommend buffering also VNEG supply of the chip. As highlighted in the block diagram it is mandatory to get a voltage difference between VPOS and VNEG of min. 3.4V to guaranty proper trimming of the device. no current sink capability, therefore it is possible to buffer it external with a negative power supply. The VNEG voltage applied to VNEG pin must be lower than the voltage created with the charge pump. This means if the typical VNEG output voltage is -1.5V you can easily apply externally -1.7V. The charge pump switches then automatically into skip mode.

Important for applying an external buffer and switching on the ANC device is the timing in order to avoid latch up on the ANC device. The timing diagram in Figure 2 shows clearly that it is important that there is a certain delay between VBAT and the MODE /CSCL pin necessary. This delay is mandatory in order to guaranty that the device starts up properly. In case AS350x is used the delay between VBAT and MODE/CSCL is not necessary. The MODE /CSCL pin powers the ANC device up and the whole sequence to power up the internal charge pump of AS34x0 and AS350x takes approximately 1ms. Once VNEG is settled the external VNEG buffer (e.g. power supply) can be enabled in order to support the charge pump especially during the trim process which can now be started.

Figure 27. Timing Diagram for VNEG Buffering

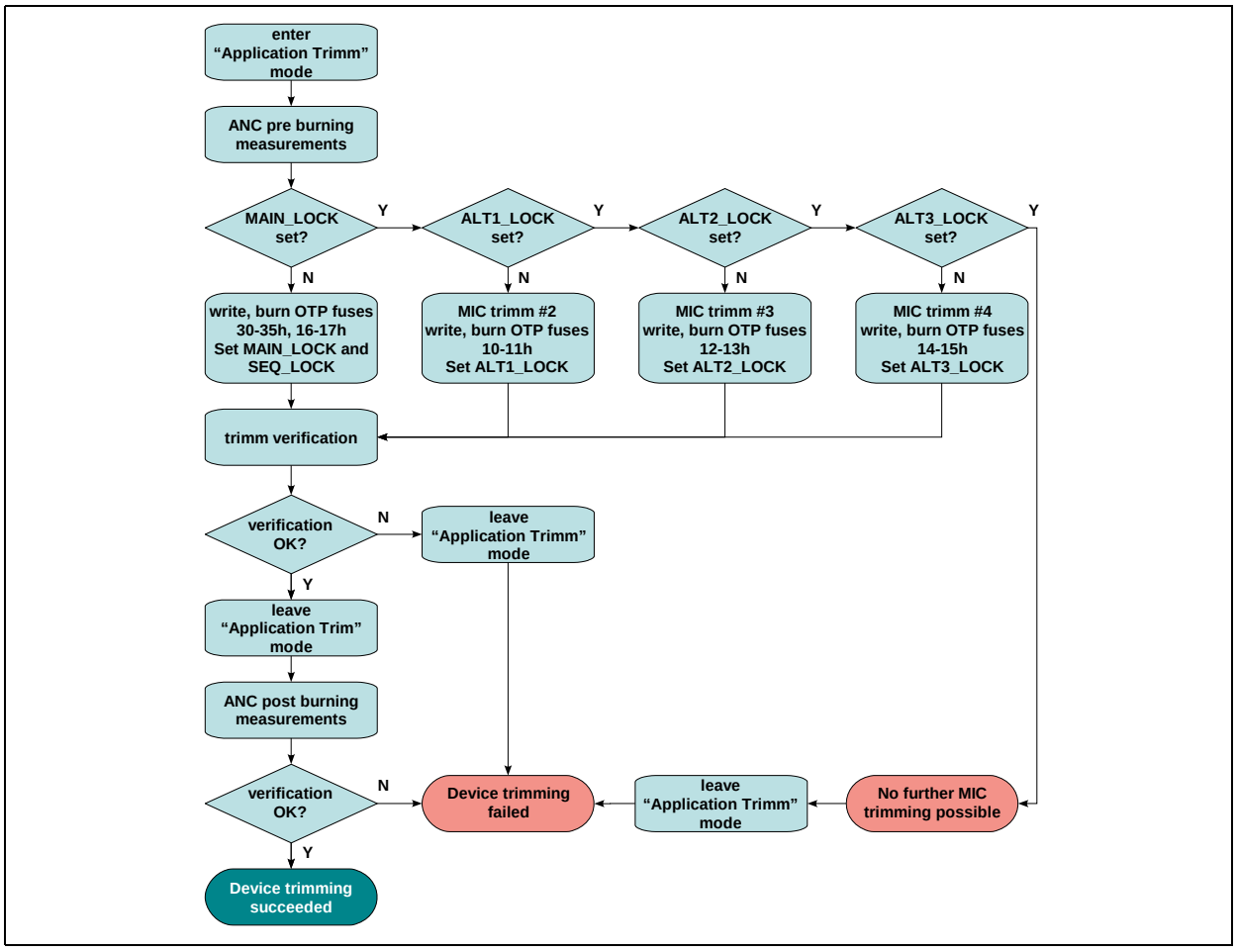


To guaranty a successful trimming process it is important to follow exactly the predefined trimming sequence shown inFigure 28. As a first step it is important to do a register dump of all OTP registers. This register backup in your system memory is a backup of all register setting and is necessary for the verification after the trim process to make sure that all bits are trimmed correctly. Once the register dump has been done it is important to check the OTP_LOCK in register 0x35. This register indicates if the device is already trimmed or not. In case this bit is set to '1' there is no more trimming possible. The device has obviously already been trimmed before. In case the bit is '0' there is initial or further trimming of the device possible. You enter the trim mode and start the trimming process. Once the trimming is done the most important step is comparing the values trimmed to the device with the original register dump we did right before we started with the actual trimming process. If the verification was successful we know that all bits have been trimmed correctly to AS3501/AS3502. What is important to mention is that the AS3502 and AS3501 have a couple of test bits inside which are per default set to '1'. We do not recommend overwriting these bytes.

Furthermore it is important to know that it is not possible to change bits once they are trimmed. With AS3501 and AS3502 it is possible to trim the device again if the MAIN_LOCK bit is not set to '1'. What is not possible is, is changing a bit from '1' back to zero. If an additional trimming is done it is only possible to change bits from '0' to '1'. An example would be the following. A register contains a value of 0x41. If the MAIN_LOCK bit is not set to '1' you can basically re-trim the part but it doesn't work to change the value from 0x41 to 0x40. What is possible would be a change from 0x41 to 0x43. It is important that all necessary bits are trimmed exactly like in the block diagram shown in Figure 28. The internal state machine needs the MAIN_LOCK bit as well as the ALTx_LOCK bits to determine the right microphone register at start-up of the device. If the MAIN_LOCK bit and the ALTx_LOCK bits are not set correctly the result can be malfunction of the device.

for detailed implementation of the I2C trimming there is also an application note available which describes the whole process in more detail and includes also some code examples.

Figure 28. OTP Burning Process



9.8 2-Wire-Serial Control Interface

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Eh_write
- 8Fh_read

9.8.1 Protocol

Table 13. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1110b (8Eh)
DR	Device address for read	R	1000 1111b (8Fh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit

Table 13. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3421 AS3422 (=slave) receives data		
	AS3421 AS3422 (=slave) transmits data		

Figure 29. Byte Write

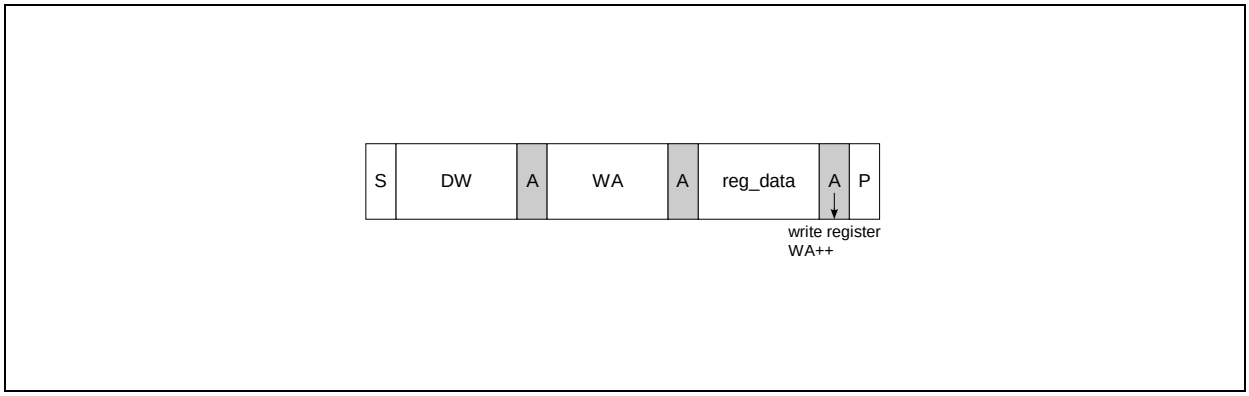
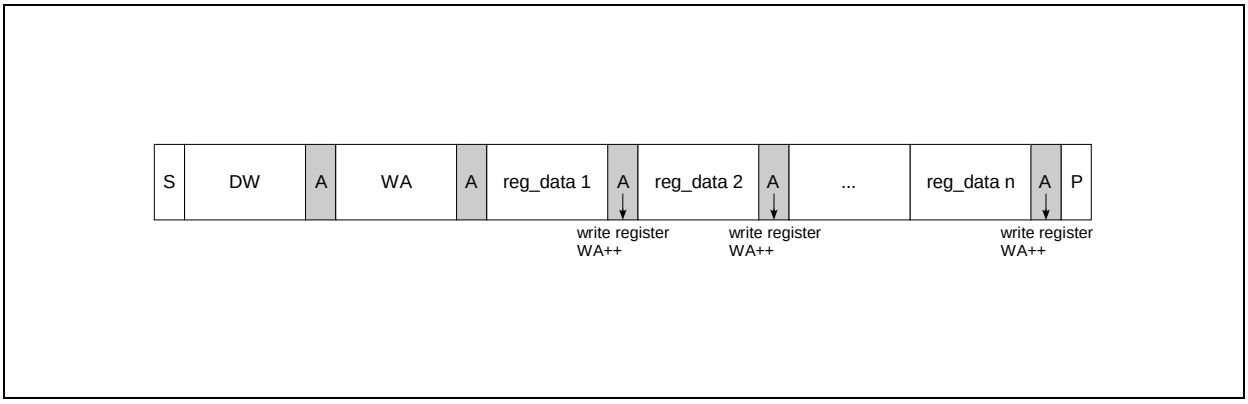


Figure 30. Page Write

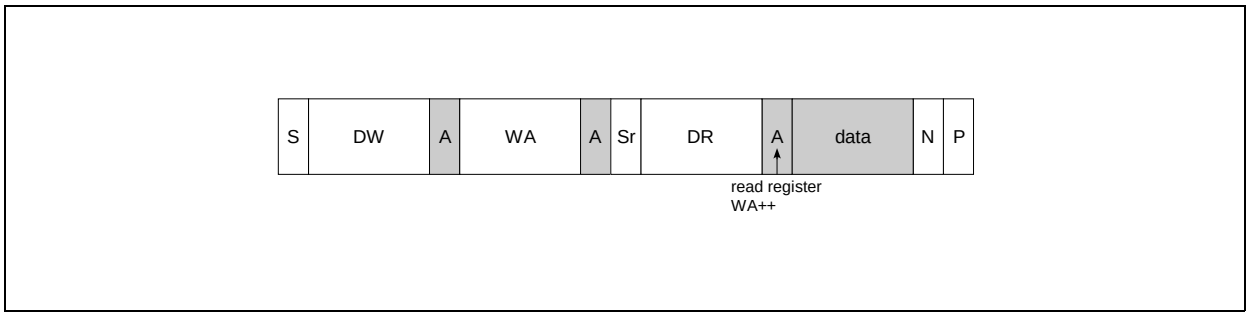


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 31. Random Read

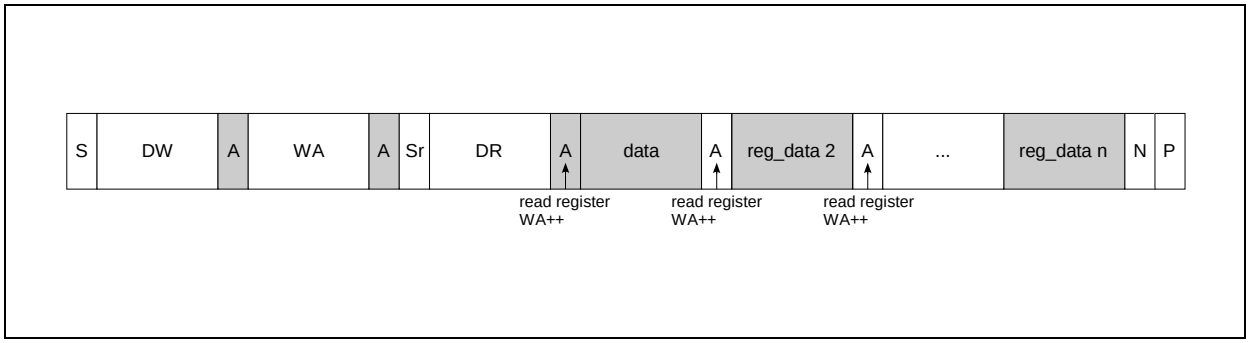


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

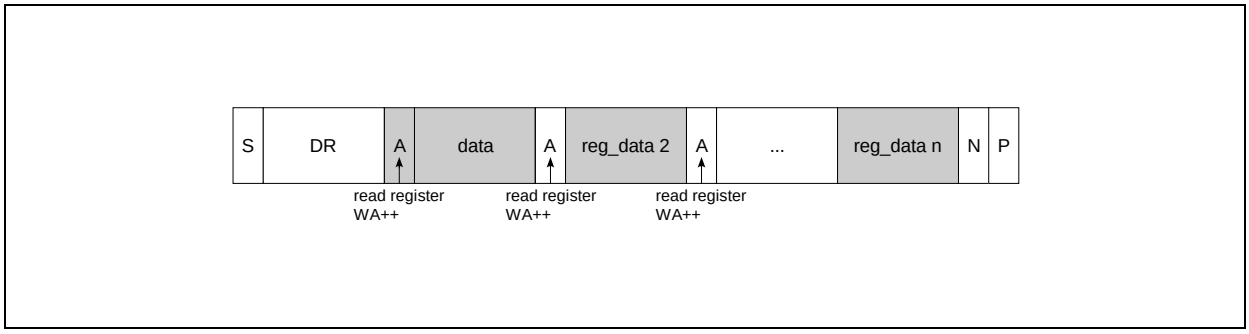
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 32. Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

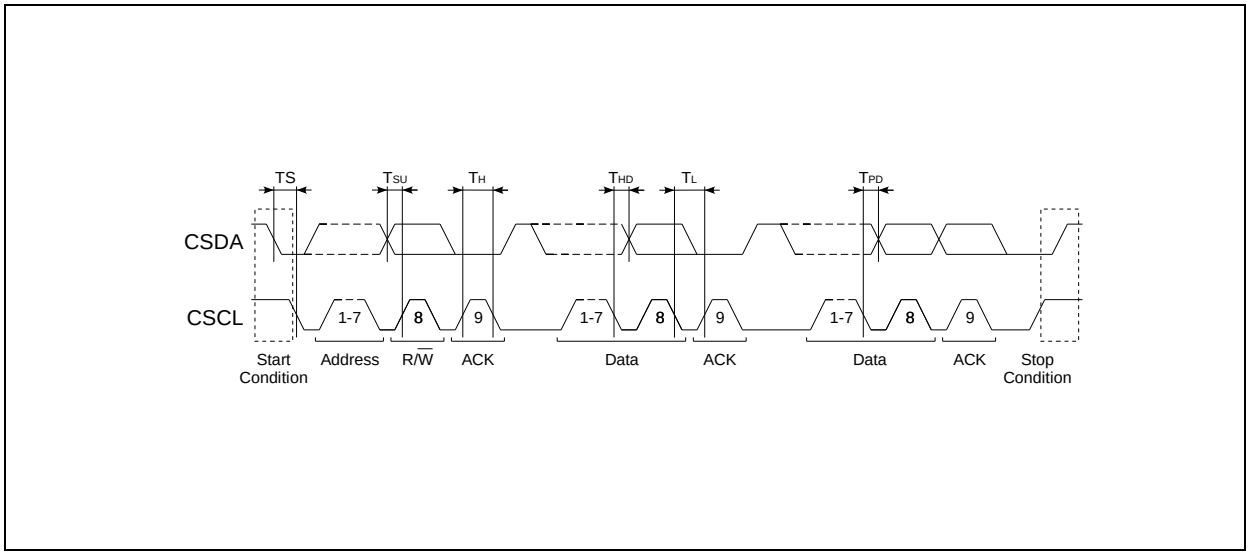
Figure 33. Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

9.8.2 Parameter

Figure 34. 2-Wire Serial Timing



VBAT >=1.4V[1], T_A=25ºC, unless otherwise specified.

Table 14. 2-Wire Serial Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%VBAT)	0	-	0.42	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%VBAT)	0.98	-		V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to low going edge of CSCL		50		ns

1. Serial interface operates down to VBAT = 1.0V but with 100kHz clock speed and degraded parameters.

10 Register Description

Table 15. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Audio Registers									
00-07h	reserved								
08h	MIC_L	MIC_MODE 0: StereoSingleEnd 1: MonoDiff	MICL_VOL<6:0> Gain from MICL to QMICL or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
09h	MIC_R	MIC_REG_ON 0: use reg 30h & 31h 1: use reg 08h & 09h	MICR_VOL<6:0> Gain from MICR to QMICR or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
0Ah	LINE_IN	LIN_REG_ON 0: use reg 33h and VOL pin 1: use reg 0Ah	LIN_GAIN_+3dB 0: 0dB max. Line Gain 1: +3dB max. Line Gain	LIN_VOL<5:0> 0: MUTE; 0x01..0x3F: Gain from LINR/L to QLINR/L or Mixer = -46.5dB...+0dB; 63 steps of 0.75dB with LIN_GAIN_+3dB bit set to '0' 0x01..0x3F: Gain from LINR/L to QLINR/L or Mixer = -43.5dB...+3dB; 63 steps of 0.75dB with LIN_GAIN_+3dB bit set to '1'				
0Bh	GP_OP_L	HP_MUX<1:0> 0: MIC; 1: OP1; 2: OP2; 3: open		OP2L<3:0> 0: OP2L inverting mode; 0x1..0xF: OP2L non inverting mode gain = 0...10.5dB; 15 steps of 0.75dB				OP2L_ON	OP1L_ON
0Ch	GP_OP_R	OP_REG_ON 0: use reg 34h 1: use reg 0Bh & 0Ch	HP_MODE 0: StereoSingleEnd 1: MonoDiff	OP2R<3:0> 0: OP2R inverting mode; 0x1..0xF: OP2R non inverting mode gain = 0...10.5dB; 15 steps of 0.75dB				OP2R_ON	OP1R_ON
0Dh-0Fh	reserved								
18h-1Fh	reserved								
System Register									
20h	SYSTEM	Design_Version<3:0> 1001				REG3F_ON	MONITOR_ON	CONT_PWRUP	PWR_HOLD
21h	PWR_SET	PWR_REG_ON 0: use reg 0x35 1: use reg 0x21h			HP_ON	MIC_ON	LIN_ON	MICS_CP_ON	MICS_ON
			LOW_BAT	PWRUP_ COMPLETE					
22h-2Fh	reserved								

Table 15. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
OTP Register									
10h	ANC_L2	TEST_BIT_5	MICL_VOL_OTP2<6:0> Gain from MICL to QMICL or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
11h	ANC_R2	ALT1_LOCK	MICR_VOL_OTP2<6:0> Gain from MICR to QMICR or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
12h	ANC_L3	TEST_BIT_6	MICL_VOL_OTP3<6:0> Gain from MICL to QMICL or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
13h	ANC_R3	ALT2_LOCK	MICR_VOL_OTP3<6:0> Gain from MICR to QMICR or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
14h	ANC_L4	TEST_BIT_7	MICL_VOL_OTP4<6:0> Gain from MICL to QMICL or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
15h	ANC_R4	ALT3_LOCK	MICR_VOL_OTP4<6:0> Gain from MICR to QMICR or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
16h	MICS_CNTR						LowBat + 100mV		DEL_ ANC_MUX
17h	PWRUP	SEQ_LOCK	FAST_START<4:0> 0: ~900ms; 0Eh: ~600ms					LIN_AGC_OFF	MIC_AGC_OFF
30h	ANC_L	TEST_BIT_1	MICL_VOL_OTP<6:0> Gain from MICL to QMICL or Mixer = MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
31h	ANC_R	TEST_BIT_2	MICR_VOL_OTP<6:0> Gain from MICR to QMICR or Mixer =MUTE, -11.25dB...+36dB; 127 steps of 0.375dB						
32h	MIC_MON	MON_MODE 0: fixed volume 1: adj. volume	MIC_MON_OTP<6:0> Gain from MICl/R to QMICL/R or Mixer = MUTE, -5.625dB...+41.6dB; 0.375dB steps, if MON_MODE is set to 0 Gain from MICl/R to QMICL/R or Mixer = MUTE, -5.625dB...+41.6dB; 0.375dB steps, adjustable by VOL pin if MON_MODE is set to 1						
33h	AUDIO_SET	NO_PB_MODE_OTP 0: PB mode enabled 1: PB mode disabled	VOL_BUTTON_ MODE_OTP 0: Volume Mode disabled 1: Volume Mode enabled	LINE_GAIN_+3dB OTP 0: 0dB max. Line Gain 1: +3dB max. Line Gain	MIC_MODE_ OTP 0: StereoSingleEnd 1: MonoDiff	HP_MODE_ OTP 0: StereoSingleEnd 1: MonoDiff	LIN_MON_ATTEN<2:0> 0: no attenuation; 1..6: LIN_VOL<6:0> shift by -6dB...-36dB 7: MUTE		
34h	GP_OP	HP_MUX_OTP<1:0> 0: MIC; 1: OP1; 2: OP2; 3: -		OP2_OTP<3:0> 0: OP2 inverting mode; 0x1..0xF: OP2 non inverting mode gain = 0...10.5dB; 15 steps of 0.75dB				OP2_ON_OTP	OP1_ON_OTP
35h	OTP_SYS	MAIN_LOCK 0: write reg 30h.. 35h 1: lock reg 30h..35h	TEST_BIT_3	MON_HP_MUX<1:0> 0: MIC; 1: OP1; 2: OP2; 3: -			CP_MODE 0: Low noise, low voltage 1: High output voltage;	MICS_CP_OFF	I2C_MODE
3Eh	CONFIG_1					EXTBURNCLK			
3Fh	CONFIG_2			TM34	BURNSW	TM_REG34-35	TM_REG30-33	OTP_MODE<1:0> 0: READ; 1: LOAD; 2: WRITE; 3: BURN	

Table 16. MIC_L Register

Name		Base		Default
MIC_L		2-wire serial		00h
Offset: 08h		Left Microphone Input Register		
		Configures the gain for the left microphone input and defines the microphone operation mode. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MIC_MODE	0	R/W	Selects the microphone input mode 0: single ended stereo mode 1: mono differential mode
6:0	MICL_VOL<6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25 dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625 dB gain 11 1111: 36 dB gain

Table 17. MIC_R Register

Name		Base		Default
MIC_R		2-wire serial		00h
Offset: 09h		Right Microphone Input Register		
		Configures the gain for the right microphone input and enables register 08h & 09h. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MIC_REG_ON	0	R/W	Defines which registers are used for the microphone settings. 0: settings of register 30h and 31h are used 1: settings of register 08h and 09h are used
6:0	MICR_VOL<6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25B gain 00 0010: -10.875 dB gain .. 11 1110: 35.625 dB gain 11 1111: 36 dB gain

Table 18. LINE_IN Register

Name		Base		Default
LINE_IN		2-wire serial		00h
Offset: 0Ah		Line Input Register		
		Configures the attenuation for the line input, defines the line input operation mode and enables register 0Ah. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LIN_REG_ON	0	R/W	Defines which source is used for the line input settings. 0: settings of register 33h and VOL pin are used 1: register 0Ah is used
6	LINE_GAIN_+3dB	0	R/W	Selects the line input operating gain range. If this bit is set the gain range of the line input amplifiers is shifted by +3dB. 0: Line Input gain range from -46.5dB...0dB 1: Line Input gain range from -43.5dB...+3dB
5:0	LIN_VOL<5:0>	00 0000	R/W	Volume settings for line input, adjustable in 63 steps of 0.75dB. the following gain settings are valid if LINE_GAIN_+3dB bit is set to '0'. 00 0000: MUTE 00 0001:-46.5dB gain 00 0010:-45.75dB gain .. 11 1110:-0.75dB gain 11 1111:.0 dB gain
				Volume settings for line input, adjustable in 63 steps of 0.75dB. the following gain settings are valid if LINE_GAIN_+3dB bit is set to '1'. 00 0000: MUTE 00 0001:-43.5dB gain 00 0010:-42.75dB gain .. 11 1110:+2.25dB gain 11 1111:+3 dB gain

Table 19. GP_OP_L Register

Name		Base		Default
GP_OP_L		2-wire serial		00h
Offset: 0Bh		Left General Purpose Operational Amplifier Register		
		Enables the left opamp stages, defines opamp 2 mode and gain and sets the HP input multiplexer. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	HP_MUX<1:0>	00	R/W	Multiplexes the analog audio signal to HP amp 00: MIC: selects QMICL/R output 01: OP1: selects QOP1L/R outputs 10:OP2: selects QOP2L/R output 11: open: no signal mixed together with the line input signal
5:2	OP2L<3:0>	0000	R/W	Mode and volume settings for left OP2, adjustable in 15 steps of 0.75dB 0000: OP2L in inverting mode 0001: 0 dB gain, OP2L in non inverting mode 0001: 0.75 dB gain, non inverting .., 1110: 9.75dB gain, non inverting 1111:.10.5 dB gain, non inverting

Table 19. GP_OP_L Register

Name		Base		Default
GP_OP_L		2-wire serial		00h
Offset: 0Bh		Left General Purpose Operational Amplifier Register		
		Enables the left opamp stages, defines opamp 2 mode and gain and sets the HP input multiplexer. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	OP2L_ON	0	R/W	Enables left OP 2 0: left OP2 is switched off 1: left OP2 is enabled
0	OP1L_ON	0	R/W	Enables left OP 1 0: left OP1 is switched off 1: left OP1 is enabled

Table 20. GP_OP_R Register

Name		Base		Default
GP_OP_R		2-wire serial		00h
Offset: 0Ch		Right General Purpose Operational Amplifier Register		
		Enables the right opamp stages, defines opamp 2 mode and gain and sets the HP mode. This register is reset at POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OP_REG_ON	0	R/W	Defines which register is used for the opamp and HP settings. 0: settings of register 33h and 34h are used 1: register 0B and 0Ch are used
6	HP_MODE	0	R/W	Selects the line input mode 0: single ended stereo mode 1: mono differential mode
5:2	OP2R<3:0>	0000	R/W	Mode and volume settings for right OP2, adjustable in 15 steps of 0.75dB 0000: OP2R in inverting mode 0001: 0 dB gain, OP2R in non inverting mode 0001: 0.75 dB gain, non inverting .., 1110: 9.75dB gain, non inverting 1111:.10.5 dB gain, non inverting
1	OP2R_ON	0	R/W	Enables right OP 2 0: right OP2 is switched off 1: right OP2 is enabled
0	OP1R_ON	0	R/W	Enables right OP 1 0: right OP1 is switched off 1: right OP1 is enabled

Table 21. SYSTEM Register

Name		Base		Default
SYSTEM		2-wire serial		31h
Offset: 20h		SYSTEM Register		
		This register is reset at a POR.		
Bit	Bit Name	Default	Access	Bit Description
7:4	Design_Version<3:0>	1001	R	AFE number to identify the design version 1001: for chip version 1v1
3	TESTREG_ON	0	R/W	0: normal operation 1: enables writing to test register 3Eh & 3Fh to configure the OTP and set the access mode.
2	MONITOR_ON	0	R/W	Enables the monitor mode 0: normal operation 1: monitor mode enabled
1	CONT_PWRUP	0	R/W	Continues the automatic power-up sequence when using the I2C mode 0: chip stops the power-up sequence after the supplies are stable, switching on individual blocks has to be done via I2C commands 1: automatic power-up sequence is continued
0	PWR_HOLD	1	R/W	0: power up hold is cleared and AFE will power down 1: is automatically set to on after power on

Table 22. PWR_SET Register

Name		Base		Default
PWR_SET		2-wire serial		0x11 1111b (stand alone mode) 0x00 0000b (I2C mode)
Offset: 21h		Power Setting Register		
		Please be aware that writing to this register will enable/disable the corresponding blocks, while reading gets the actual status. It is not possible to read back e.g ILED settings. This register is reset at POR.		
Bit	Bit Name	Default	Access	Bit Description
7	PWR_REG_ON	0	R/W	Defines which register is used for the power settings. 0: all blocks stay on as defined in the start-up sequence 1: register 21h is used
6	LOW_BAT	x	R	VBAT supervisor status 0: VBAT is above brown out level 1: BVDD has reached brown out level
5	PWRUP_COMPLETE	x	R	Power-Up sequencer status 0: power-up sequence incomplete 1: power-up sequence completed
4	HP_ON	0	W	0: switches HP stage off 1: switches HP stage on
		x	R	0: HP stage not powered 1: normal operation
3	MIC_ON	0	W	0: switches microphone stage off 1: switches microphone stage on
		x	R	0: microphone stage not powered 1: normal operation

Table 22. PWR_SET Register

Name		Base		Default
PWR_SET		2-wire serial		0x11 1111b (stand alone mode) 0x00 0000b (I2C mode)
Offset: 21h		Power Setting Register		
		Please be aware that writing to this register will enable/disable the corresponding blocks, while reading gets the actual status. It is not possible to read back e.g ILED settings. This register is reset at POR.		
Bit	Bit Name	Default	Access	Bit Description
2	LIN_ON	0	W	0: switches line input stage off 1: switches line input stage on
		x	R	0: line input stage not powered 1: normal operation
1	MICS_CP_ON	0	W	0: switches microphone supply charge pump off 1: switches microphone supply charge pump on
		x	R	0: microphone supply charge pump not powered 1: normal operation
0	MICS_ON	0	W	0: switches microphone supply off 1: switches microphone supply on
		x	R	0: microphone supply not enabled 1: normal operation

Table 23. ANC_L2 Register

Name		Base		Default
ANC_L2		2-wire serial		80h (OTP)
Offset: 10h		Left OTP Microphone Input Register (2nd OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_5	1	R	for testing purpose only
6:0	MICL_VOL_OTP2 <6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 24. ANC_R2 Register

Name		Base		Default
ANC_R2		2-wire serial		00h (OTP)
Offset: 11h		Right OTP Microphone Input Register (2nd OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	ALT1_LOCK	0	R/W	0: additional bits can be fused inside register 10h & 11h 1: OTP fusing for register 10h & 11h gets locked, no more changes can be done.
6:0	MICR_VOL_OTP2 <6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 25. ANC_L3 Register

Name		Base		Default
ANC_L3		2-wire serial		80h (OTP)
Offset: 12h		Left OTP Microphone Input Register (3rd OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_6	1	R	for testing purpose only
6:0	MICL_VOL_OTP3 <6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 26. ANC_R3 Register

Name		Base		Default
ANC_R3		2-wire serial		00h (OTP)
Offset: 13h		Right OTP Microphone Input Register (3rd OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	ALT2_LOCK	0	R/W	0: additional bits can be fused inside register 12h & 13h 1: OTP fusing for register 12h & 13h gets locked, no more changes can be done.
6:0	MICR_VOL_OTP3 <6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 27. ANC_L4 Register

Name		Base		Default
ANC_L4		2-wire serial		80h (OTP)
Offset: 14h		Left OTP Microphone Input Register (4th OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_7	1	R	for testing purpose only
6:0	MICL_VOL_OTP4 <6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 28. ANC_R4 Register

Name		Base		Default
ANC_R4		2-wire serial		00h (OTP)
Offset: 15h		Right OTP Microphone Input Register (4th OTP option)		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	ALT3_LOCK	0	R/W	0: additional bits can be fused inside register 14h & 15h 1: OTP fusing for register 14h & 15h gets locked, no more changes can be done.
6:0	MICR_VOL_OTP4 <6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 29. MICS_CNTR Register

Name		Base		Default
MICS_CNTR		2-wire serial		00h (OTP)
Offset: 16h		Microphone Supply Regsiter		
		Configures the low battery threshold value		
Bit	Bit Name	Default	Access	Bit Description
3	LowBat	0	R/W	0: default LowBat value 1: 100mV increase of LowBat threshold
0	DEL_ ANC_MUX	0	R/W	0: default startup timing of AS3421/22 1: HP_MUX_OTP is set to OTP value 0.8s after device startup

Table 30. PWRUP_CNTR Register

Name		Base		Default
PWRUP_CNTR		2-wire serial		00h (OTP)
Offset: 17h		PowerUp Control Register		
		Configures chip start-up speed. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	SEQ_LOCK	0	R/W	0: additional bits can be fused inside register 16h & 17h 1: OTP fusing for register 16h & 17h gets locked, no more changes can be done.
6:2	FAST_START <4:0>	0 0000	R/W	0h: ~900ms start-up time 0Eh: ~600ms start-up time
1	LIN_AGC_OFF	0	R/W	0: Line Input AGC enabled 1: Line Input AGC switched off
0	MIC_AGC_OFF	0	R/W	0:Microphone Input AGC enabled 1: Microphone Input AGC switched off

Table 31. ANC_L Register

Name		Base		Default
ANC_L		2-wire serial		80h (OTP)
Offset: 30h		Left OTP Microphone Input Register		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_1	1	R	for testing purpose only
6:0	MICL_VOL_OTP <6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 32. ANC_R Register

Name		Base		Default
ANC_R		2-wire serial		80h (OTP)
Offset: 31h		Right OTP Microphone Input Register		
		Configures the gain for the left microphone input. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	TEST_BIT_2	1	R	for testing purpose only
6:0	MICR_VOL_OTP <6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 127 steps of 0.375dB 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 33. MIC_MON Register

Name		Base		Default
MIC_MON		2-wire serial		00h (OTP)
Offset: 32h		OPT Microphone Monitor Mode Register		
		Configures the gain for the microphone input in monitor mode. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MON_MODE	0	R/W	0: monitor mode is working with fixed microphone gain 1: monitor mode uses adjustable gain via the VOL pin
6:0	MIC_MON_OTP <6:0>	000 0000	R/W	Volume settings for microphone input during monitor mode, adjustable in 127 steps of 0.375dB. If MON_MODE bit is set to 1 the gain can be further adjusted via the VOL pin. 00 0000: MUTE 00 0001: -11.25dB gain 00 0010: -10.875 dB gain .. 11 1110: 35.625dB gain 11 1111: 36 dB gain

Table 34. AUDIO_SET Register

Name		Base		Default
AUDIO_SET		2-wire serial		00h (OTP)
Offset: 33h		OPT Audio Setting Register		
		Configures the audio settings. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	NO_PB_MODE	0	R/W	This bit defines if the low power music playback mode is enabled or not. In case the bit is set to '0', music playback mode can be entered by pulling the ANC_CSDA pin low. In case the bit is set to '1' the music playback mode is disabled. Pulling the ANC_CSDA pin low has no influence. 0: Music playback mode enabled 1: Music playback mode disabled
6	VOL_BUTTON_MODE	0	R/W	If bit is set to '1' the ANC_CSDA pin allows the user to control the line input gain via push-buttons. If bit is set to '0', the volume control is disabled. Please mind that if VOL_BUTTON_MODE bit is set to '1' entering music playback mode via ANC_CSDA pin is not possible any more. 0: Volume mode via push-button disabled 1: Volume mode via push-button enabled
5	LINE_GAIN_+3dB_OTP	0	R/W	Selects the line input operating gain range. If this bit is set the gain range of the line input amplifiers is shifted by +3dB. 0: Line Input gain range from -46.5dB...0dB 1: Line Input gain range from -43.5dB...+3dB
4	MIC_MODE_OTP	0	R/W	0: microphone input stage operating in single ended mode 1: normal operating in mono balanced

Table 34. AUDIO_SET Register

Name		Base		Default
AUDIO_SET		2-wire serial		00h (OTP)
Offset: 33h		OPT Audio Setting Register		
		Configures the audio settings. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	HP_MODE_OTP	0	R/W	0: headphone stage operating in single ended mode 1: normal operating in mono balanced
2:0	LIN_MON_ATTEN <6:0>	000	R/W	Volume settings for line input during monitor mode, adjustable in 7 steps of 6dB and mute. 000: 0dB gain 001: -6dB gain .. 110: -36dB gain 111: MUTE

Table 35. GP_OP Register

Name		Base		Default
GP_OP		2-wire serial		00h (OTP)
Offset: 34h		OTP General Purpose Operational Amplifier Register		
		Enables the opamp stages, defines opamp 2 mode and gain and sets the HP input multiplexer. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	HP_MUX_OTP<1:0>	00	R/W	Multiplexes the analog audio signal to HP amp 00: MIC: selects QMICL/R output 01:OP1: selects QOP1L/R outputs 10:OP2: selects QOP2L/R output 11: open: no signal mixed together with the line input signal
5:2	OP2_OTP<3:0>	0000	R/W	Mode and volume settings for OP2, adjustable in 15 steps of 0.75dB 0000: OP2L in inverting mode 0001: 0 dB gain, OP2L in non inverting mode 0001: 0.75 dB gain, non inverting .., 1110: 9.75dB gain, non inverting 1111:.10.5 dB gain, non inverting
1	OP2_ON	0	R/W	0: OP2 is switched off 1: left OP2 is enabled
0	OPL_ON	0	R/W	0: OP1 is switched off 1: OP1 is enabled

Table 36. OTP_SYS Register

Name		Base		Default
OTP_SYS		2-wire serial		40h (OTP)
Offset: 35h		OTP System Settings Register		
		Defines several system settings for OTP operation. This is a special register, writing needs to be enabled by writing 10b to Reg 3Fh first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MAIN_LOCK	0	R/W	0: additional bits can be fused inside the OTP 1: OTP fusing gets locked, no more changes can be done
6	TEST_BIT_3	1	R	for testing purpose only
5:4	MON_HP_MUX <1:0>	00	R/W	Multiplexes the analog audio signal to HP amp in monitor mode 00: MIC: selects QMICL/R output 01: OP1: selects QOP1L/R outputs 10:OP2: selects QOP2L/R output 11: open: no signal mixed together with the line input signal
2	CP_MODE_OTP	0	R/W	This bit controls the operating mode of the microphone supply charge pump. 0: Standard low noise operation 1: Increased output voltage
1	MICS_CP_OFF	0	R/W	0: MICS charge pump is enabled 1: MICS charge pump is switched off
0	I2C	0	R/W	0: I2C and stand alone mode start-up possible 1: chip starts-up in I2C mode only

Table 37. CONFIG_1 Register

Name		Base		Default
CONFIG_1		2-wire serial		00h
Offset: 3Eh		OTP Configuration Register		
		Controls the clock configuration. This is a special register, writing needs to be enabled by writing 9h to Reg 20h first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7:4	-	0000	n/a	
3	EXTBURNCLK	0	n/a	0: ext. clock for OTP burning disabled 1: ext. clock for OTP burning enabled
2:0	-	000	n/a	

Table 38. CONFIG_2 Register

Name		Base		Default
CONFIG_2		2-wire serial		00h
Offset: 3Fh		OTP Access Configuration Register		
		Controls the OTP access. This is a special register, writing needs to be enabled by writing 9h to Reg 20h first. This register is reset at POR and gets loaded with the OTP fuse contents.		
Bit	Bit Name	Default	Access	Bit Description
7:6	-	000	n/a	
5	TM34	0	n/a	This Register defines the Register bank selection for Register TM_REG34-35 and TMREG30-33. Depending on TM34 you can select either between Register bank 14h-17h and 10h-13h enabled or 30h-33h and 34h-37h enabled. 0: test mode Registers 14h-17h and 10h-13h disabled test mode Registers 30h-33h and 34h-37h enabled 1: test mode Registers 14h-17h and 10h-13h enabled test mode Registers 30h-33h and 34h-37h disabled
4	BURNSW	0	n/a	0: BURN switch from LINL to VNEG is disabled 1: BURN switch from LINL to VNEG is enabled
3	TM_REG34-35	0	n/a	0: test mode for Register 34h-35h disabled test mode for Register 14h-17h disabled 1: test mode for Register 34h-35h enabled test mode for Register 14h-17h enabled
2	TM_REG30-33	0	n/a	0: test mode for Register 30h-33h disabled test mode for Register 10h-13h disabled 1: test mode for Register 30h-33h enabled test mode for Register 10h-13h enabled
1:0	OTP_MODE<1:0>	00	R/W	Controls the OTP access 00: READ 01: LOAD 10: WRITE 11: BURN

11 Application Information

11.1 AS3422 Feedback Application Examples

Figure 35. AS3422 Feedback Application Example with Bluetooth I2C Control

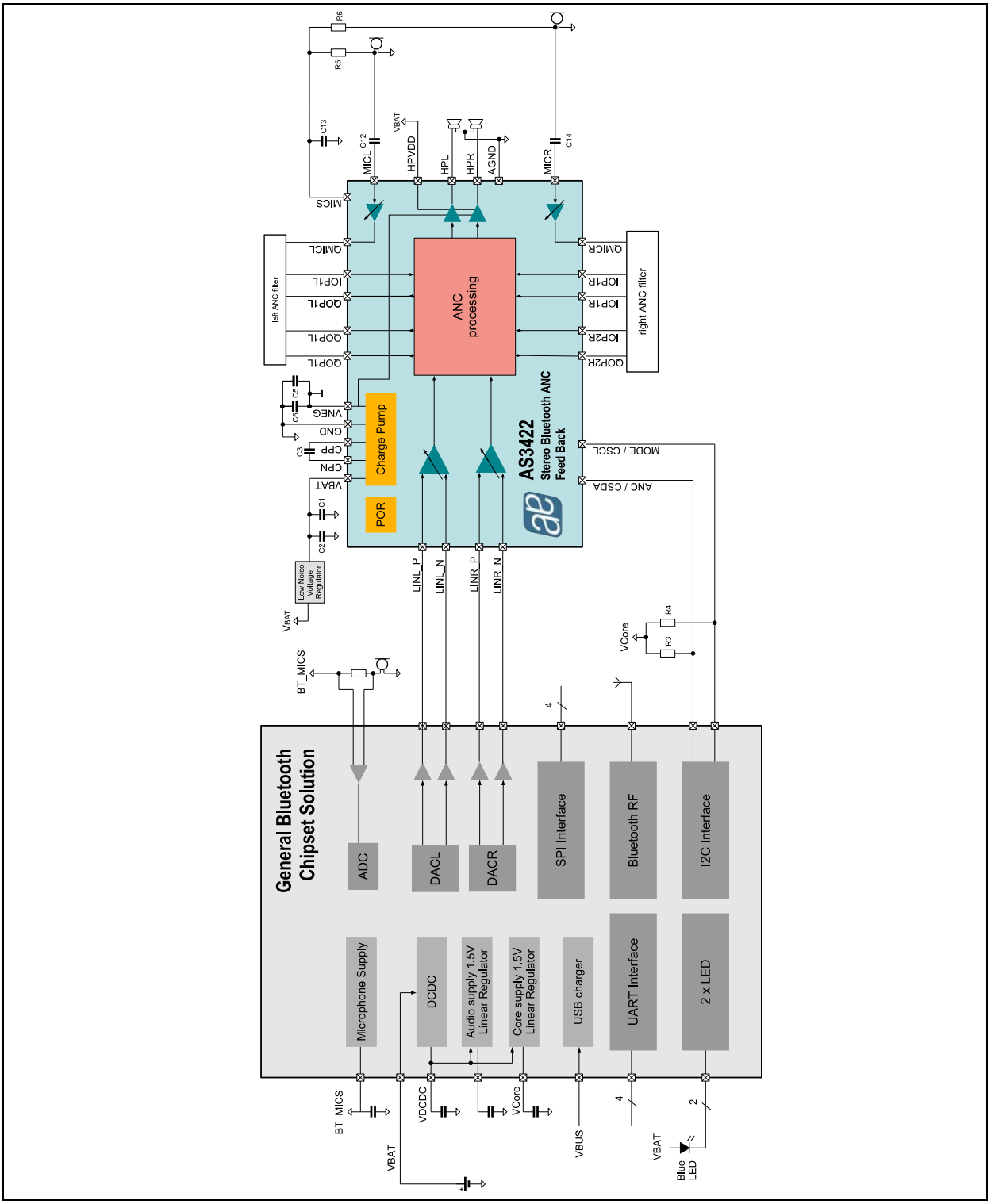


Figure 36. AS3422 Feedback Application Example with Bluetooth ROM Version (No I2C Control)

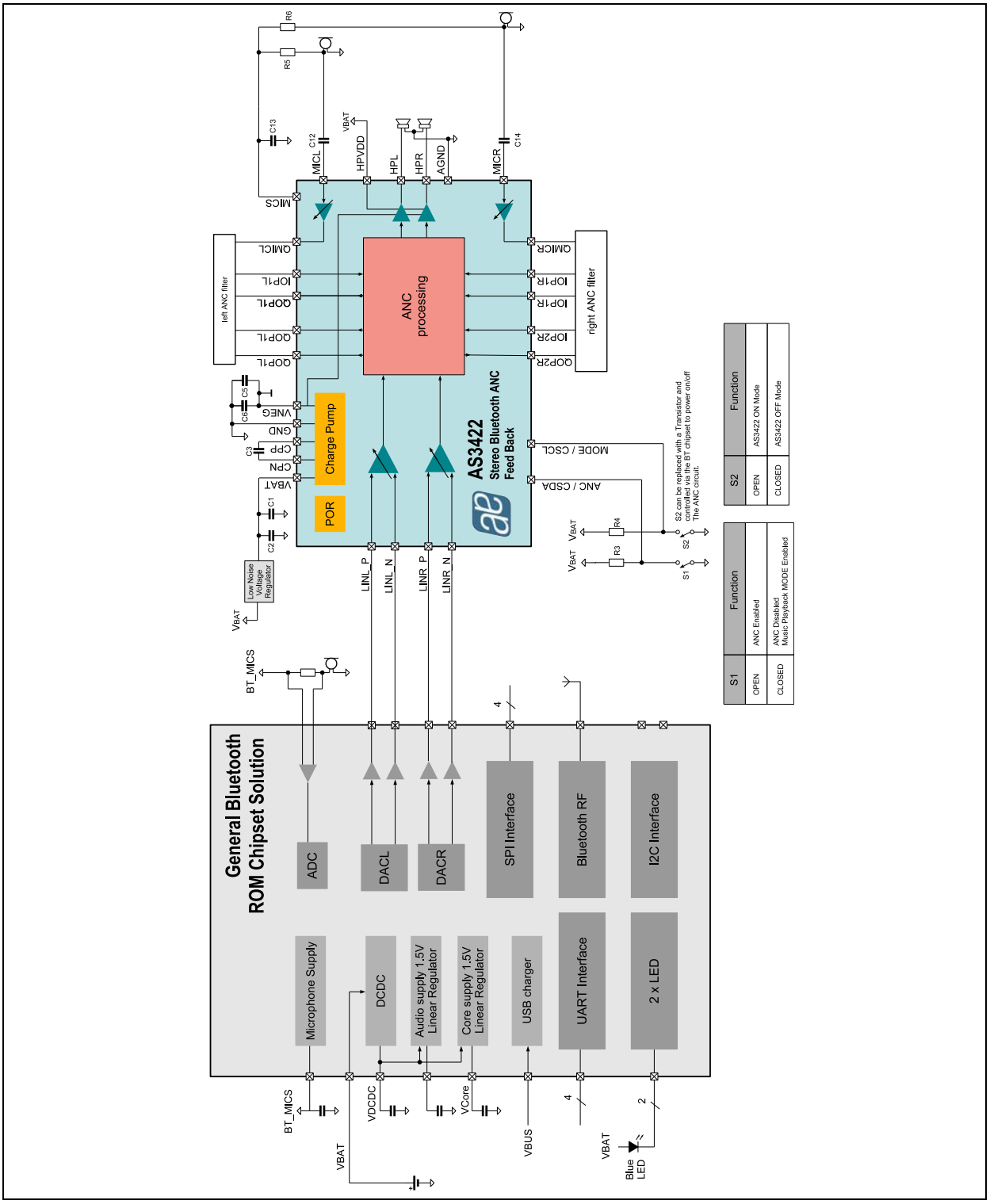


Figure 37. AS3422 Schematic - Stereo Bluetooth Feedback Application with I2C Control

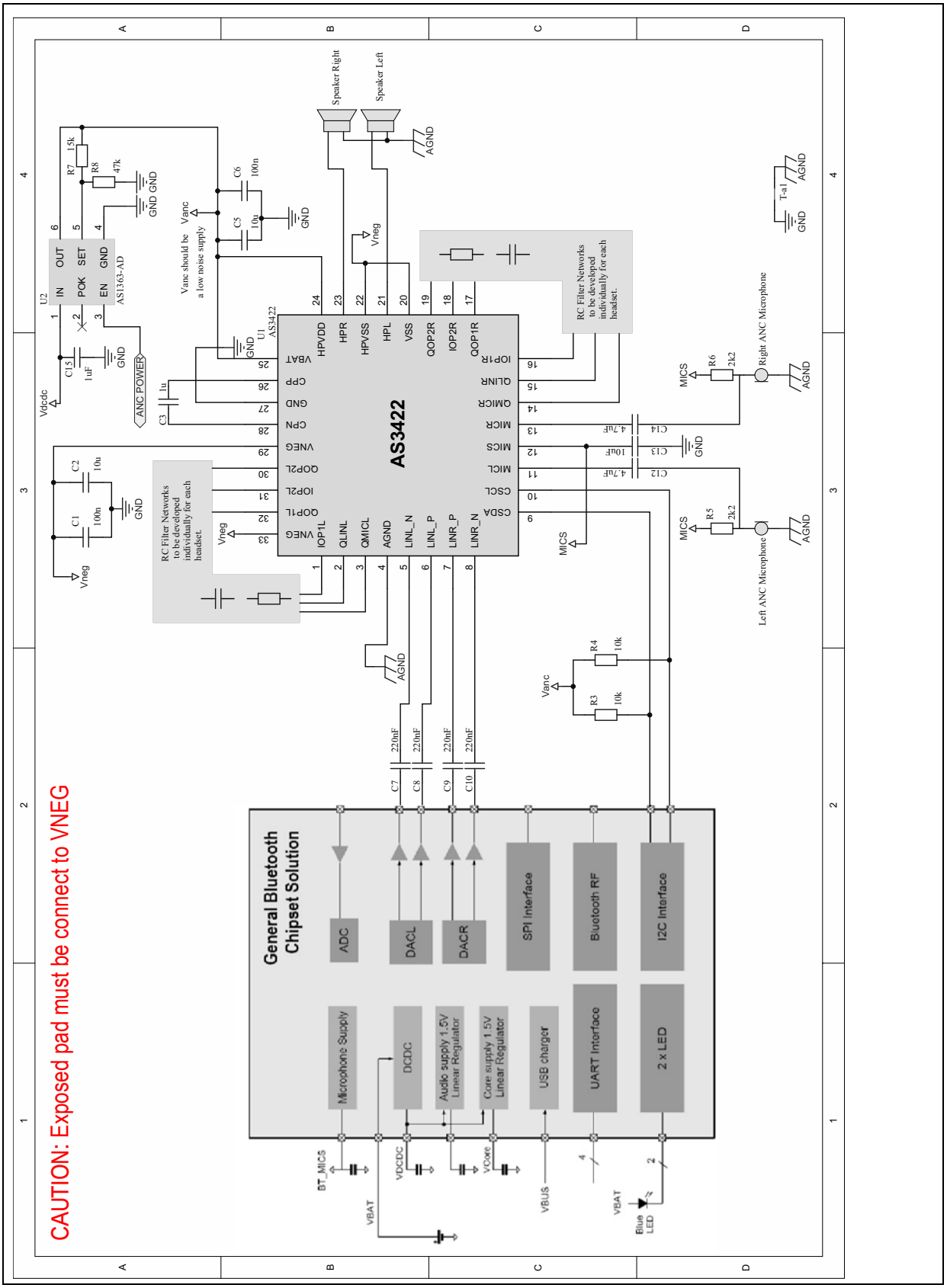
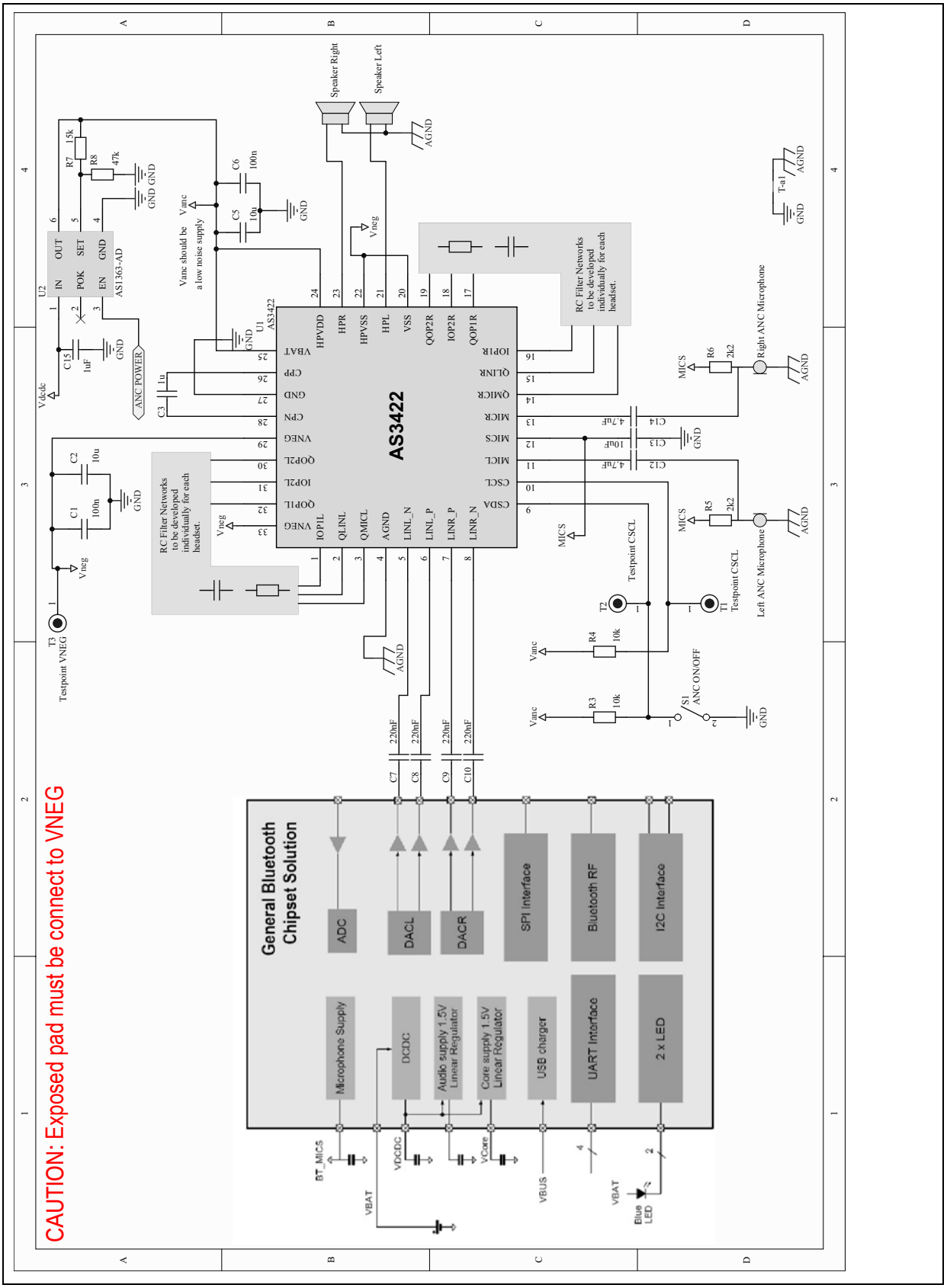


Figure 38. AS3422 Schematic - Stereo Bluetooth Feedback Application with ROM Version (No I2C Control)



11.2 AS3421 Feed Forward Application Examples

Figure 39. AS3421 Feed-Forward Application Example with Bluetooth I2C Control

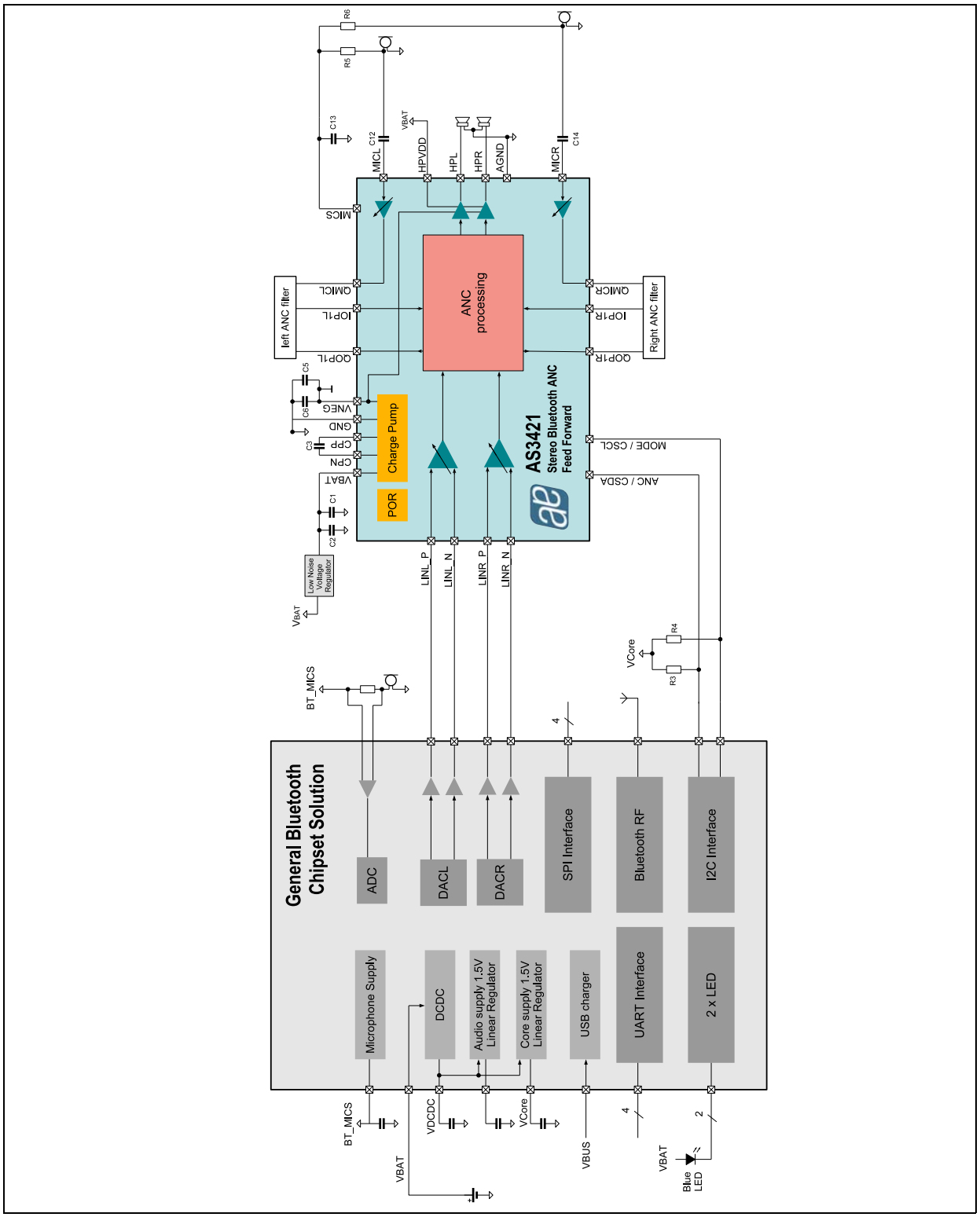


Figure 40. AS3421 Feed-Forward Application Example with Bluetooth ROM Version (No I2C Control)

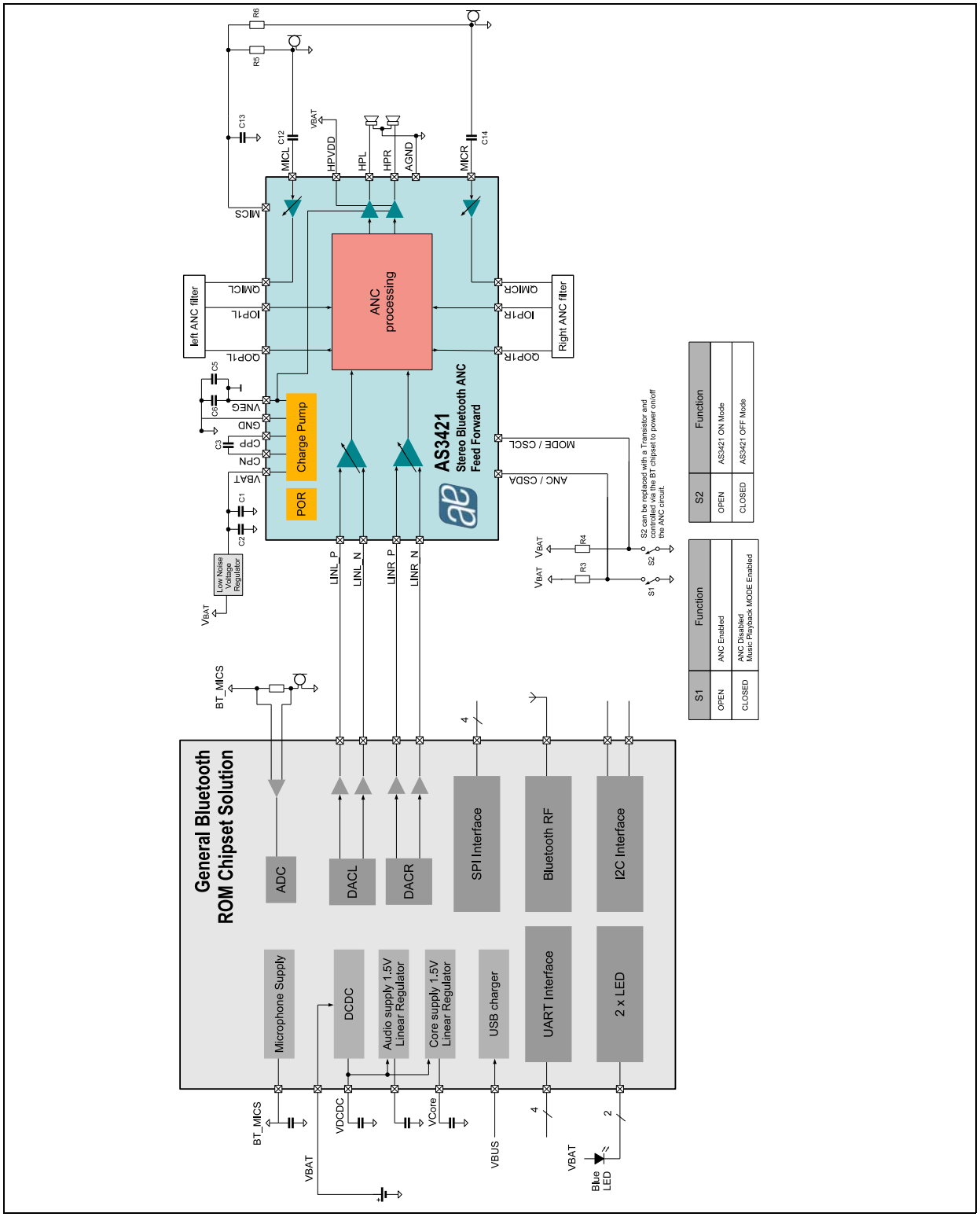


Figure 41. AS3421 Schematic - Stereo Feed-Forward Bluetooth Application with I2C Control

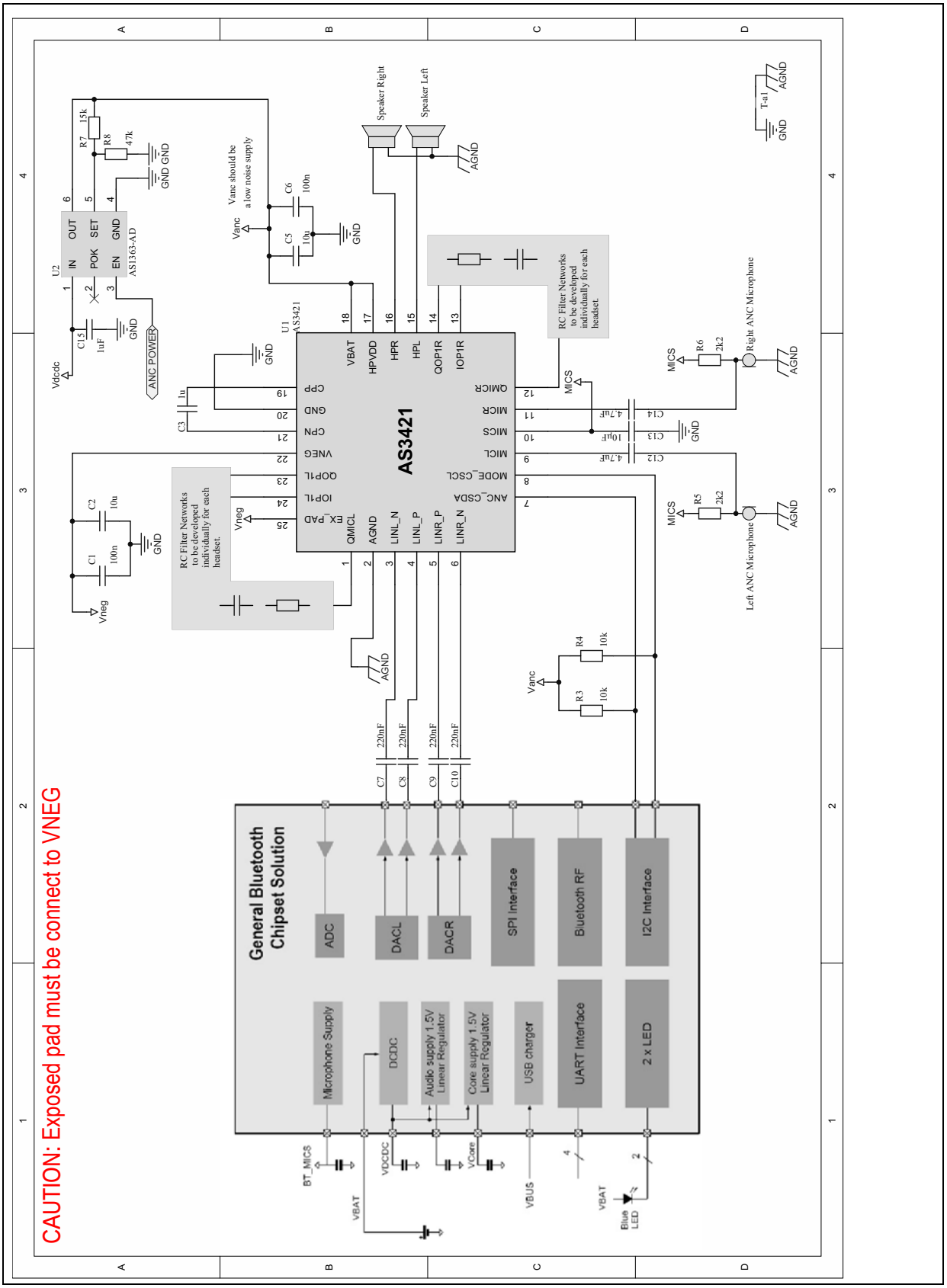
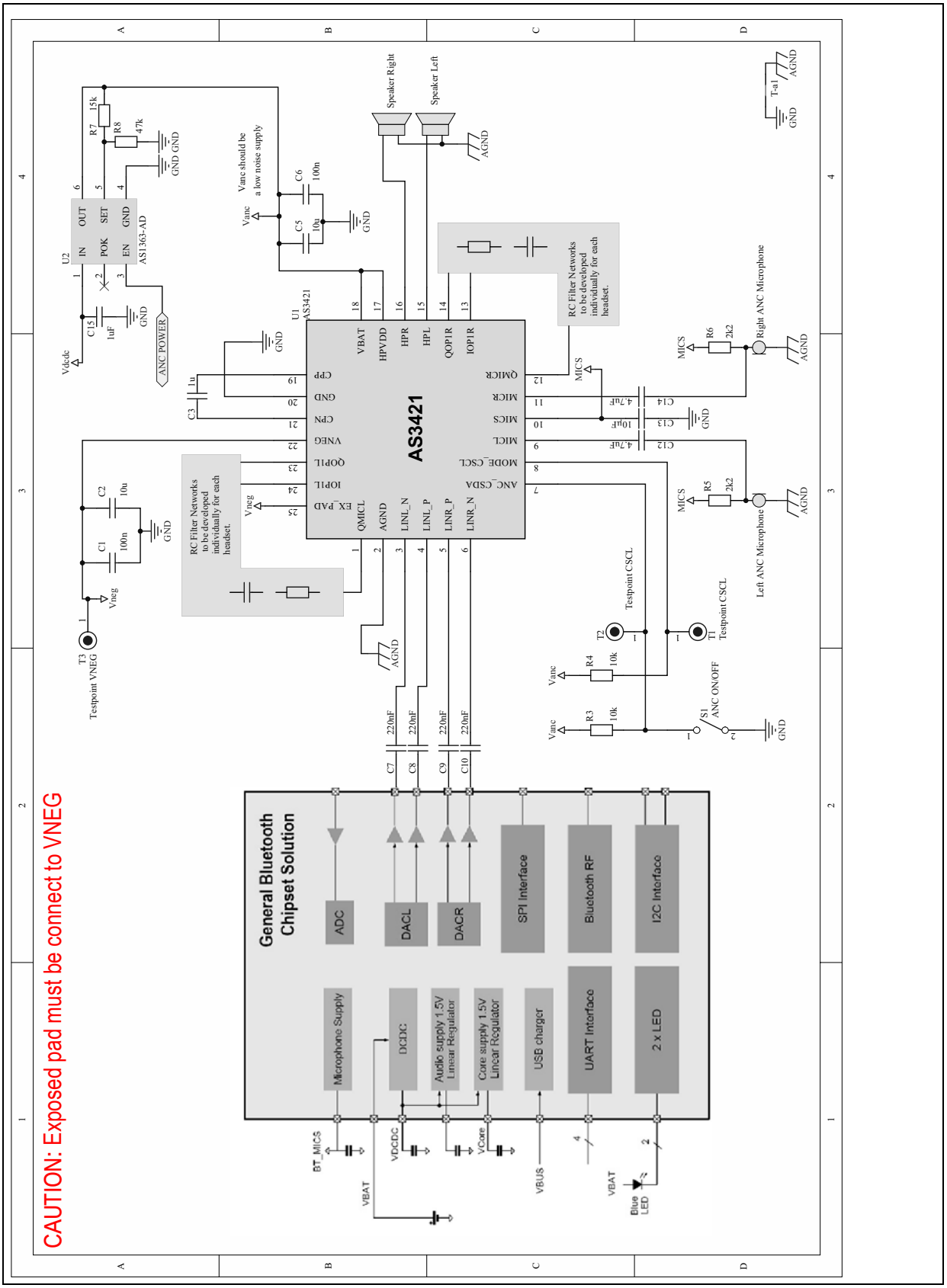


Figure 42. AS3421 Schematic - Stereo Feed-Forward Bluetooth Application ROM Version (No I2C Control)

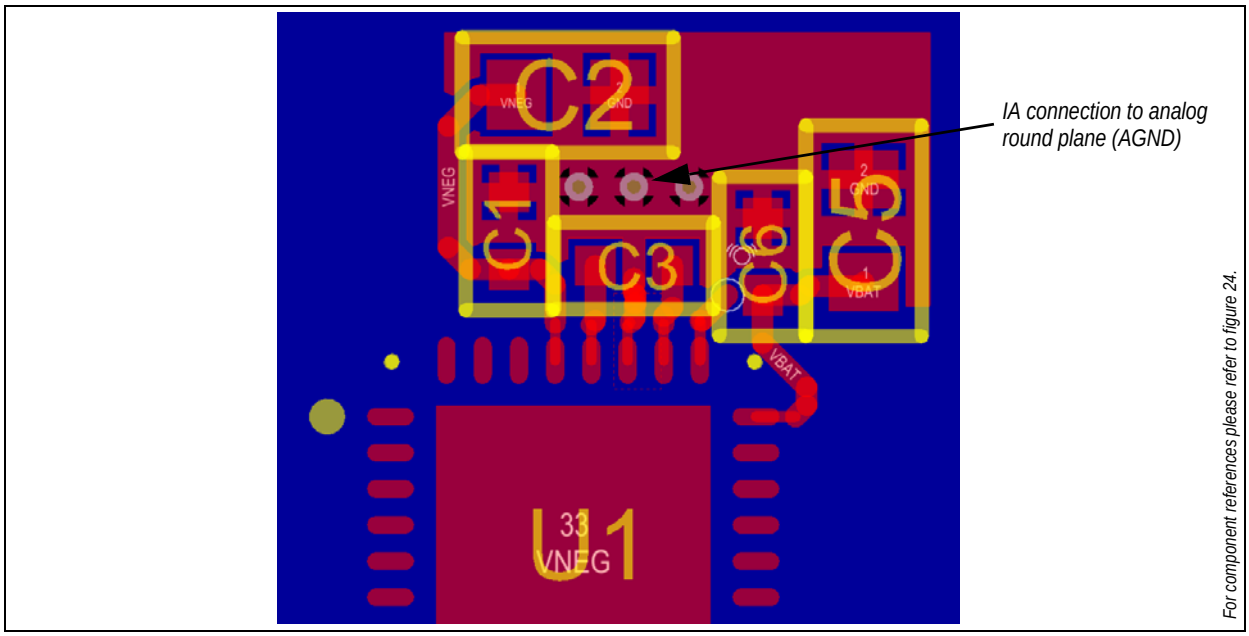


11.3 Layout Recommendation

Whereever you have audio circuits mixed with power management layout of the blocks is a critical issue. The AS3421/22 has an integrated charge pump which operates at a frequency of 1Mhz. If the layout of the PCB is not done properly the charge pump can directly influence the audio performance of the device. Therefore it is very important to make sure that the layout of the charge pump is done properly.

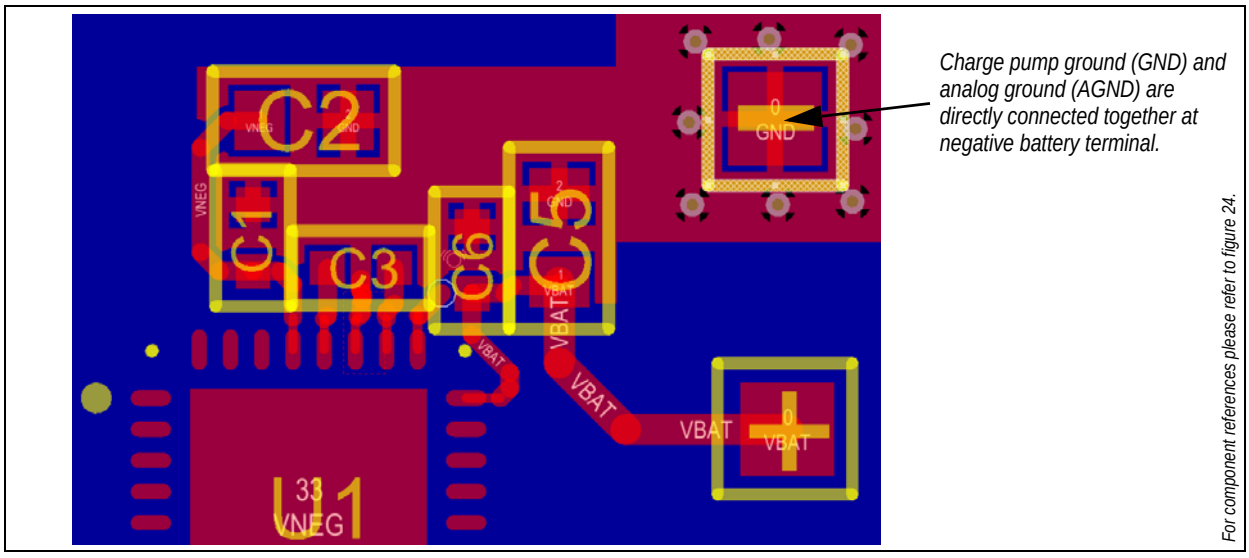
The layout recommendation shown in Figure 43 below shows an example placement of the components of the charge pump. The reference designators of the components used in the example refer to the schematic shown in Figure 37. It can be seen clearly that the ground pins of all capacitors as well as the ground pin of AS3422 are placed closely. This compact placement of the components help to minimize high frequency cross over currents all over the PCB and therefore helps to improve the audio quality. A dedicated ground plane on the top (red) layer minimizes the resistance between the ground pads of the components. The ground plane (GND) is then connected to the analog ground (AGND) at a single point which is indicated with three vias in the example.

Figure 43. AS3422 CP Layout Recommendation



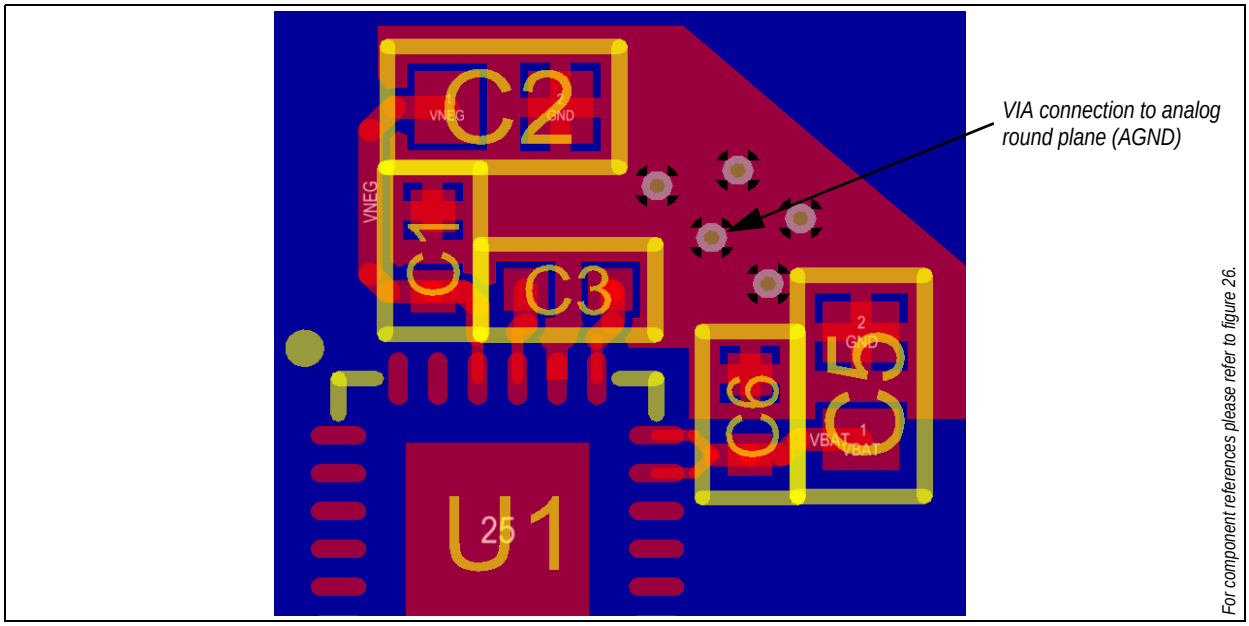
If the physical alignment of the components allows it, it is also recommended to connect the charge pump ground plane on top layer directly to the battery ground terminal of your device. The analogue- (AGND) and charge pump ground plane (GND) are then connected together directly at the battery terminal. This concept is also know as star shaped ground concept shown in Figure 44 below.

Figure 44. AS3422 Star Shaped Ground Concept



The layout examples showed in the examples before are based on AS3422. The AS3421 has of course a smaller package than AS3422, therefore the alignment of the charge pump components is different. A layout recommendation for AS3421 is shown in Figure 45 below.

Figure 45. AS3421 CP Layout Recommendation



11.4 Bill of Materials

The following section shows the Bill of Materials which is necessary to operate the device. The necessary R-C filter networks which are necessary for gain- and phase compensation are excluded. These components very much depend on the acoustic design of each headset. Both devices basically need 17 external component for standard operation without the necessary filter components. The reference designator of the components shown in Table 39 refer to the schematics shown in Figure 37 and Figure 41.

Table 39. AS3421/22 Bill of Materials

POS	Reference	Value/Name	Description	Count
1	U1	AS3421	Stereo Bluetooth ANC headphone driver circuit	1
2	U2	AS1363-AD	Low Drop Voltage Regulator	1
3	C3, C15	1µF	Charge Pump flying capacitor; +/- 10% tolerance and LDO support	2
4	C1, C6	100nF	PMU Blocking capacitors; +/- 10% tolerance	2
5	C7, C8, C9, C10	220nF	Audio DC coupling capacitors; +/- 10% tolerance	4
6	C13	10µF	Microphone supply filter capacitor; +/- 10% tolerance	1
7	C12, C14	4.7uF	Microphone DC coupling capacitors; +/-5% tolerance	2
8	R5, R6	2k2	Microphone bias resistors; +/- 5%tolerance	2
9	C2, C5	10µF	PMU Blocking capacitors; +/- 10% tolerance	2
10	R7	15k	Voltage Regulator feedback resistor	1
11	R8	47k	Voltage Regulator feedback resistor	1
12	R3, R4	10k	Two wire interface pull up resistors; +/- 10% tolerance	2
Sum				21

11.5 PCB Footprint Recommendation

Figure 46. AS3421 PCB Footprint Recommendation

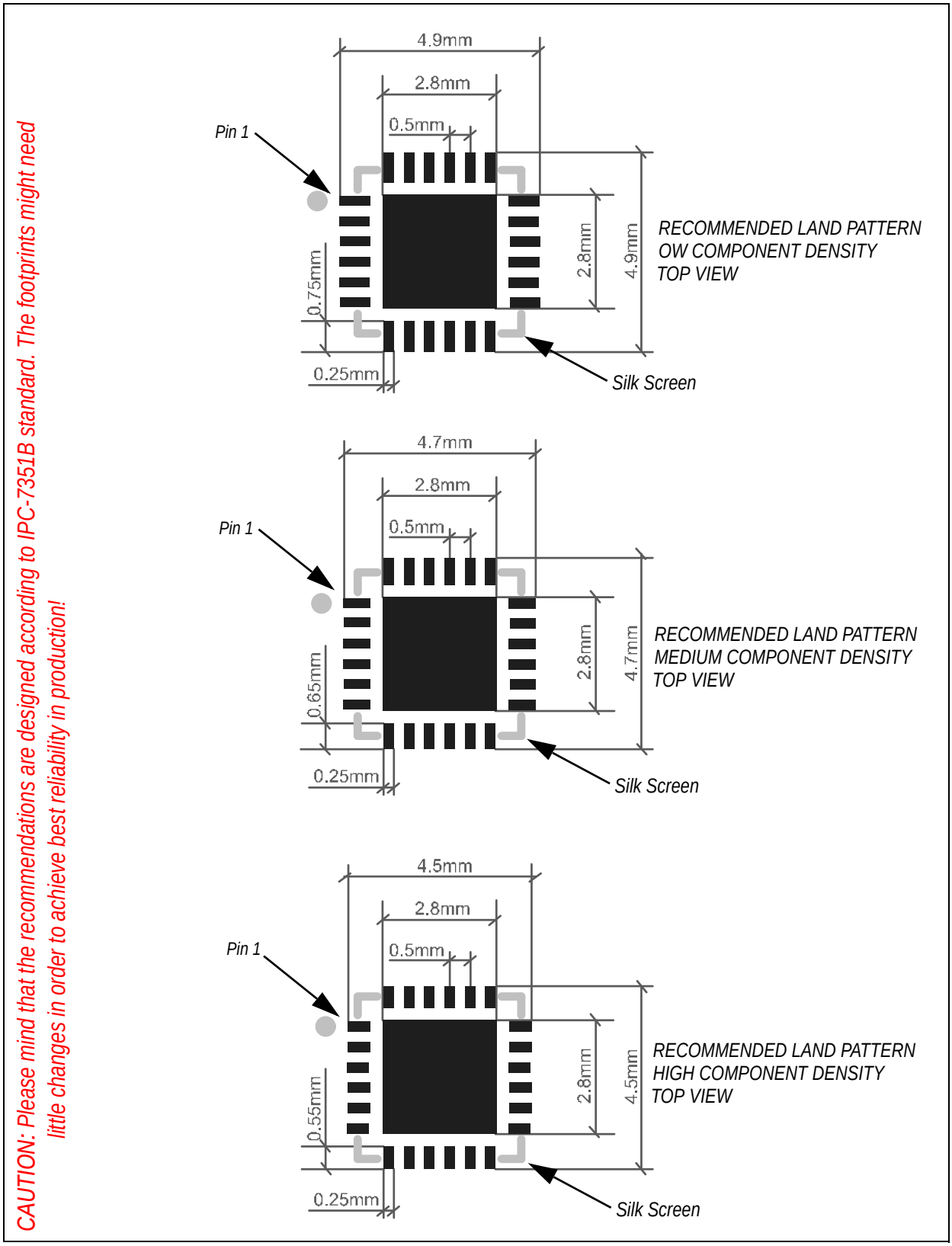
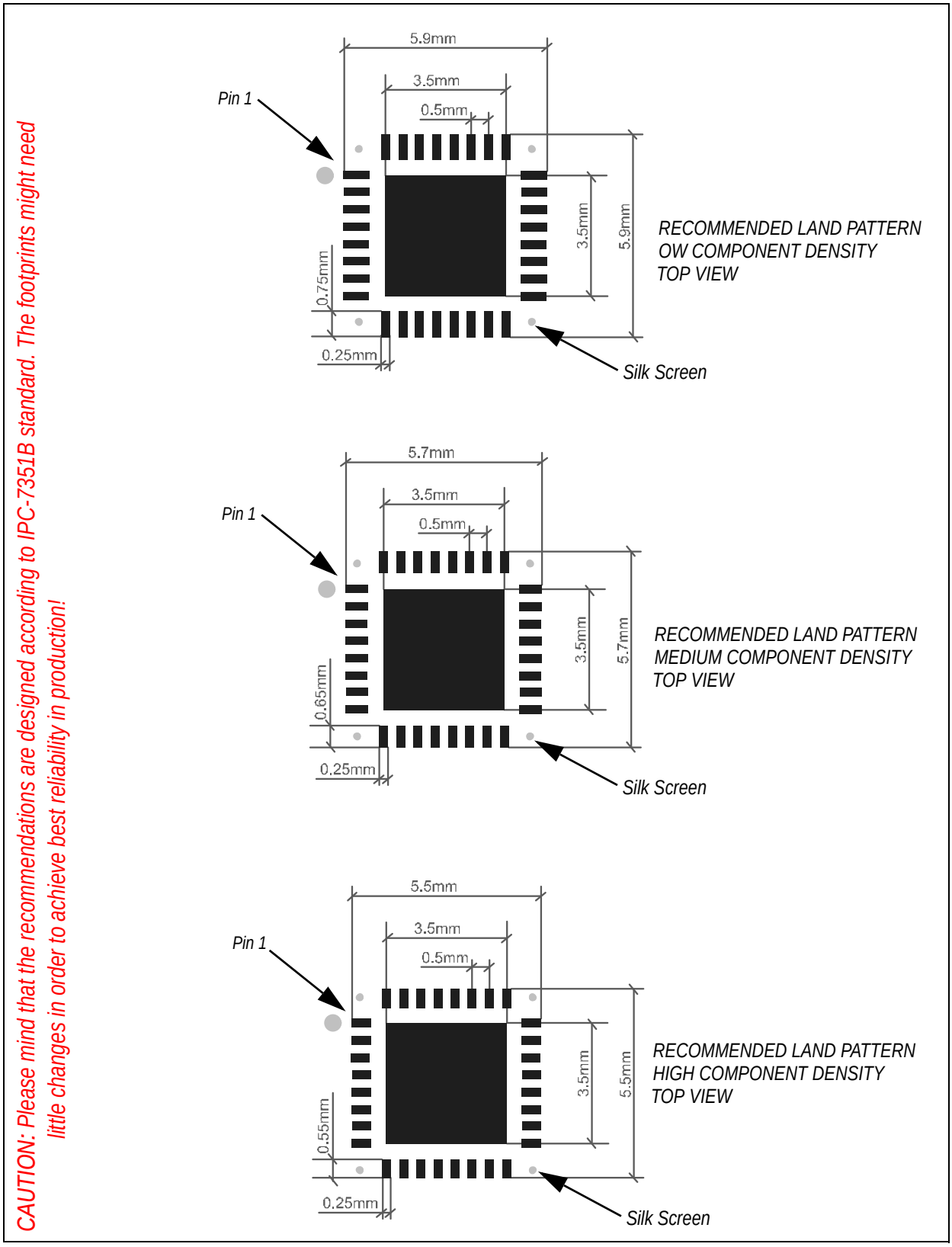


Figure 47. AS3422 PCB Footprint Recommendation



12 Package Drawings and Marking

Figure 48. QFN Marking

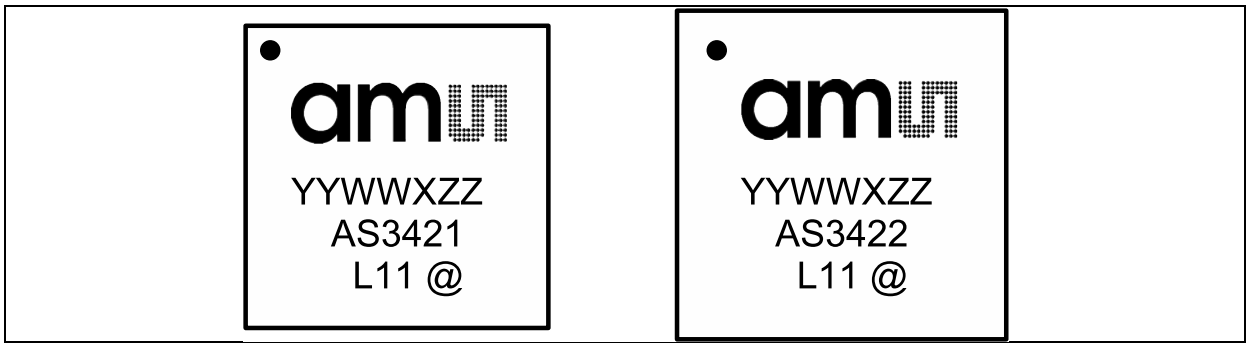
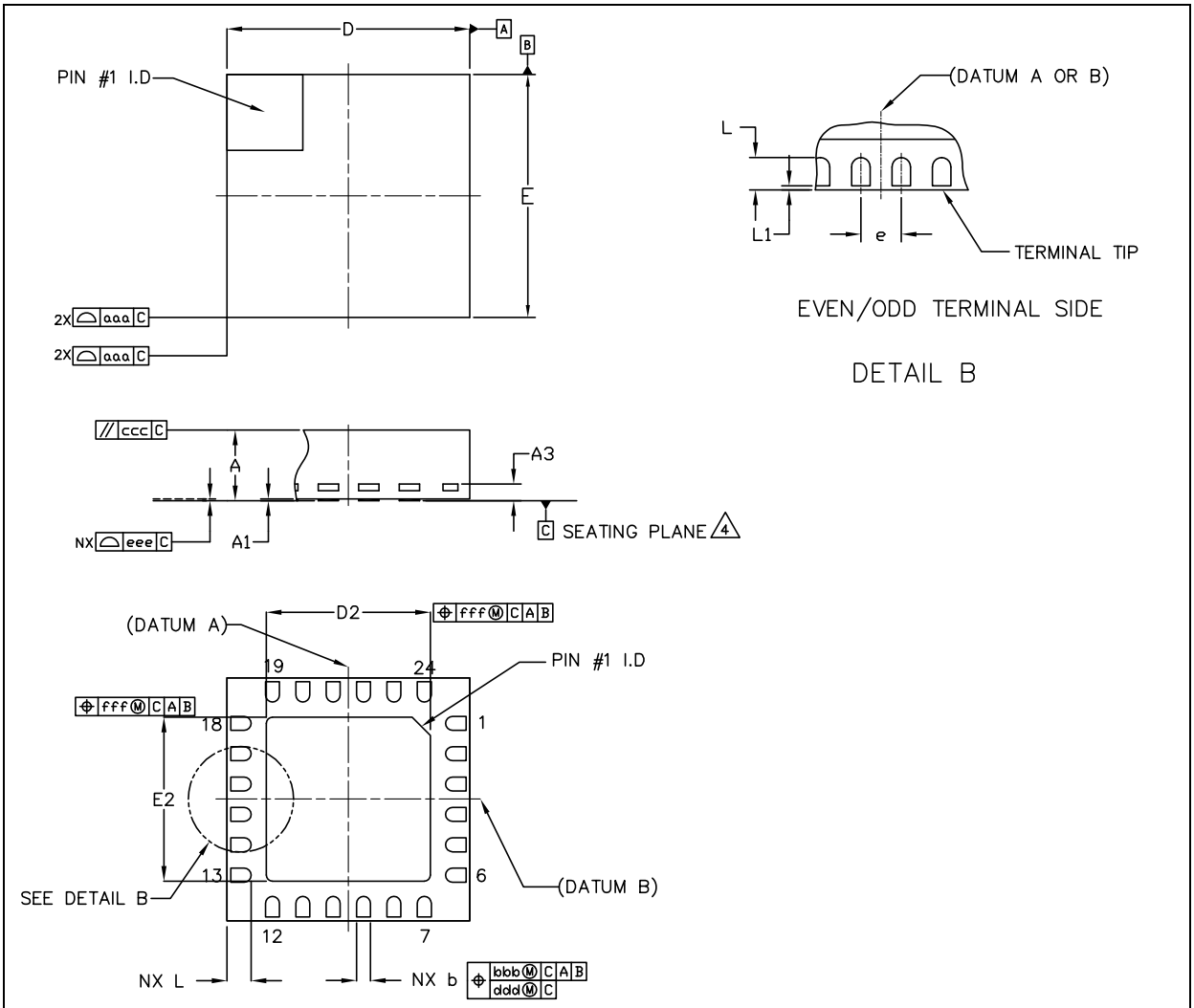


Table 40. Package Code YYWWIZZ

YY	WW	X	ZZ
last two digits of the year	manufacturing week	plant identifier	free choice / traceability code

Figure 49. AS3421, 24-pin QFN 0.5mm Pitch

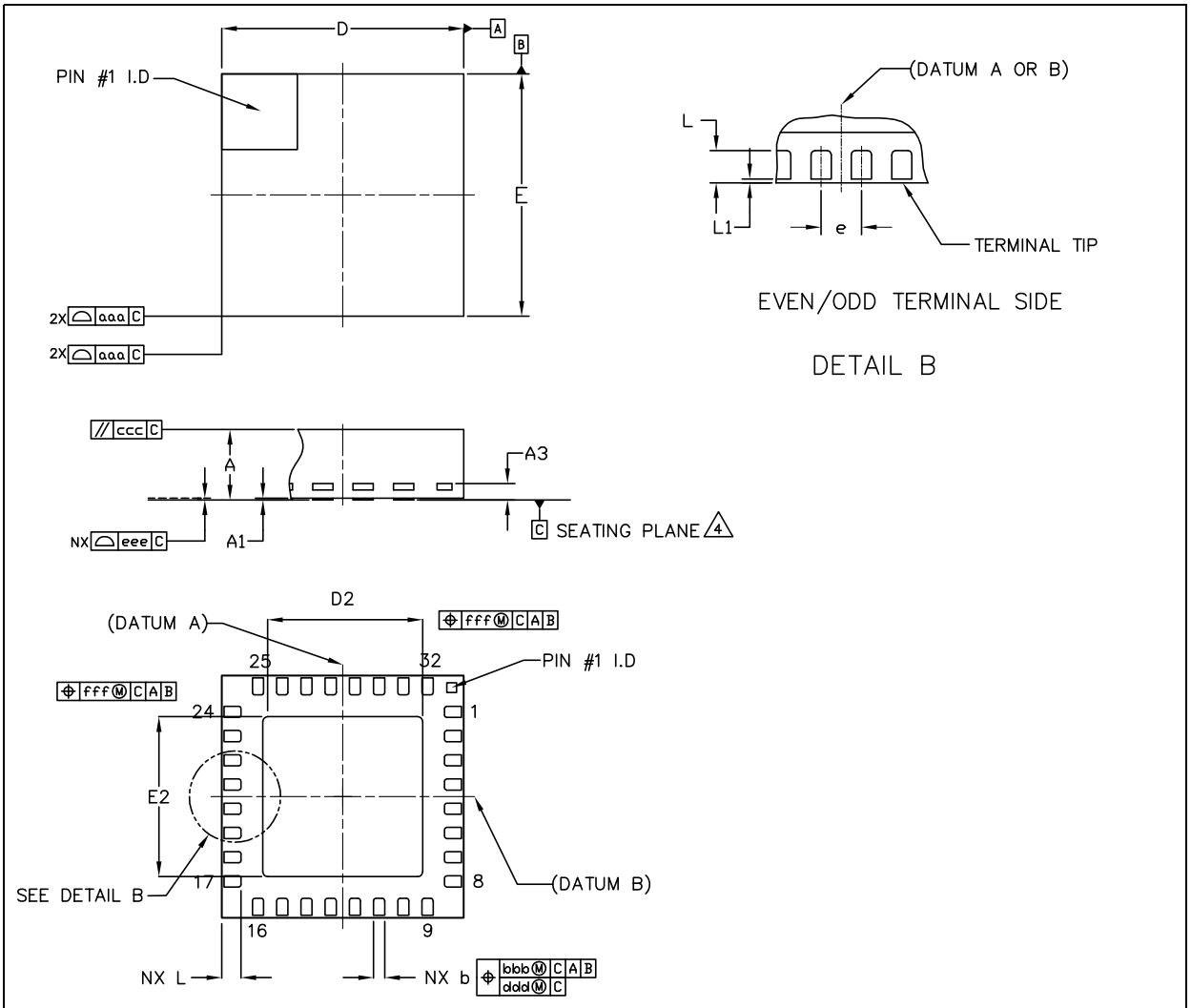


REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.35	0.40	0.45
L1	0	–	0.15
b	0.18	0.23	0.28
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

Figure 50. AS2322 32-pin QFN 0.5mm Pitch



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.35	0.40	0.45
L1	0	–	0.15
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.20	3.30	3.40
E2	3.20	3.30	3.40
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		32	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

Revision History

Revision	Date	Owner	Description
1.00	25.6.2012	hgt	initial release
1.10	08.04.2013	hgt	Updated package marking to new logo, changed Exposed Pad comments

Note: Typos may not be explicitly mentioned under revision history.

13 Ordering Information

The devices are available as the standard products shown in Table 41.

Table 41. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS3421-EQFP	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 24 [4.0x4.0x0.85mm] 0.5mm pitch
AS3421-EQFP-500	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 24 [4.0x4.0x0.85mm] 0.5mm pitch
AS3422-EQFP	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 32 [5.0x5.0x0.85mm] 0.5mm pitch
AS3422-EQFP-500	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 32 [5.0x5.0x0.85mm] 0.5mm pitch

Note: All products are RoHS compliant and ams green.
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For further information and requests, please contact us mailto:sales@ams.com
or find your local distributor at http://www.ams.com/distributor

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