
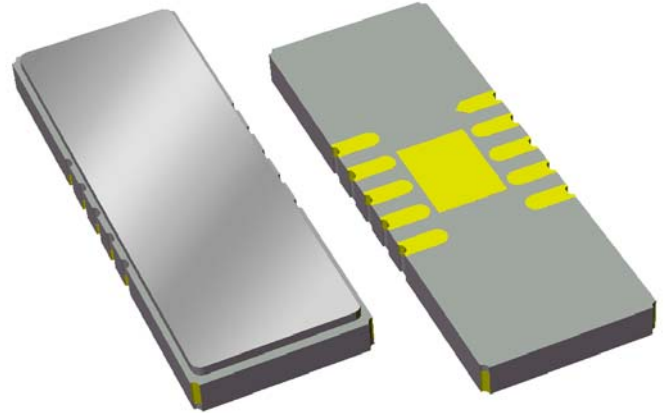


# Data Sheet

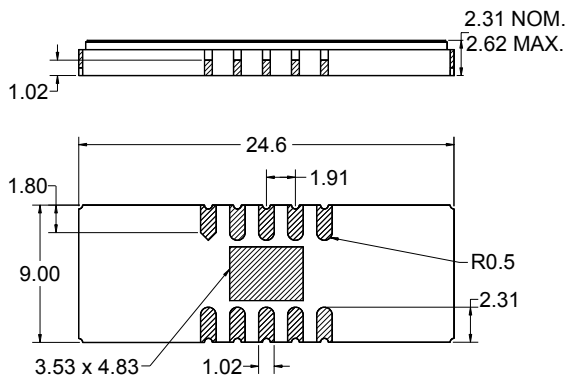
## Features

- For broadband applications
- Typical 3 dB bandwidth of 0.31 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851541 (BW 3dB=0.25 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



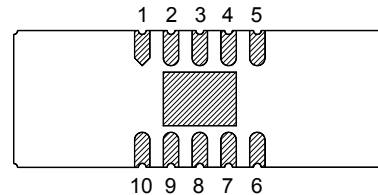
## Package

Surface Mount 24.60 x 9.00 x 2.31 mm



## Pin Configuration

Bottom View



Pin No.	Description
1	Input return
5	Output
6	Output return
10	Input
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15$ mm except overall  
length and width  $+0.13$ mm/ $-0.20$ mm

Body:  $Al_2O_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
over a 2 - 6 $\mu$ m Ni plating

**Data Sheet**
**Electrical Specifications <sup>(1)</sup>**
**Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C**

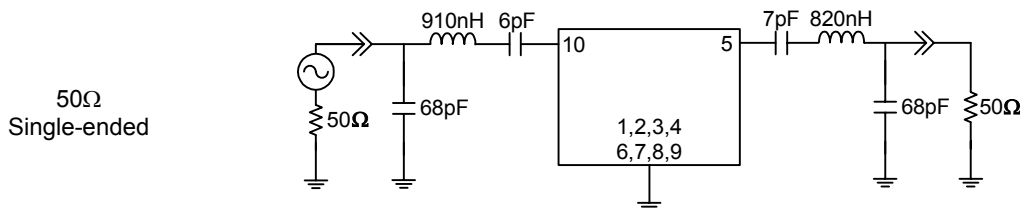
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
<b>Center Frequency</b>	-	70	-	MHz
<b>Minimum Insertion Loss</b>	-	16.36	20	dB
<b>Lower 1 dB Bandedge <sup>(4)</sup></b>	-	69.90	69.935	MHz
<b>Upper 1 dB Bandedge</b>	70.065	70.09	-	MHz
<b>Lower 3 dB Bandedge <sup>(4)</sup></b>	-	69.84	69.87	MHz
<b>Upper 3 dB Bandedge</b>	70.13	70.16	-	MHz
<b>Lower 40 dB Bandedge <sup>(4)</sup></b>	69.5	69.56	-	MHz
<b>Upper 40 dB Bandedge</b>	-	70.46	70.5	MHz
<b>Amplitude Variation</b> 69.935 - 70.065 MHz	-	0.42	1	dB
<b>Phase Linearity</b> 69.935 - 70.065 MHz	-	0.84	3	deg
<b>Group Delay Variation</b> 69.935 - 70.065 MHz	-	249.70	470	nsec
<b>Absolute Delay</b>	-	3.19	-	μsec
<b>Relative Attenuation <sup>(4)</sup></b>				
10 - 68 MHz	50	69	-	dB
72 - 80 MHz	40	52	-	dB
80 - 135 MHz	50	64.5	-	dB
135 - 145 MHz	40	49.5	-	dB
145 - 200 MHz	50	63	-	dB
<b>Source Impedance: <sup>(5)</sup></b>	-	50	-	Ω
<b>Load Impedance: <sup>(5)</sup></b>	-	50	-	Ω

**Notes:**

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

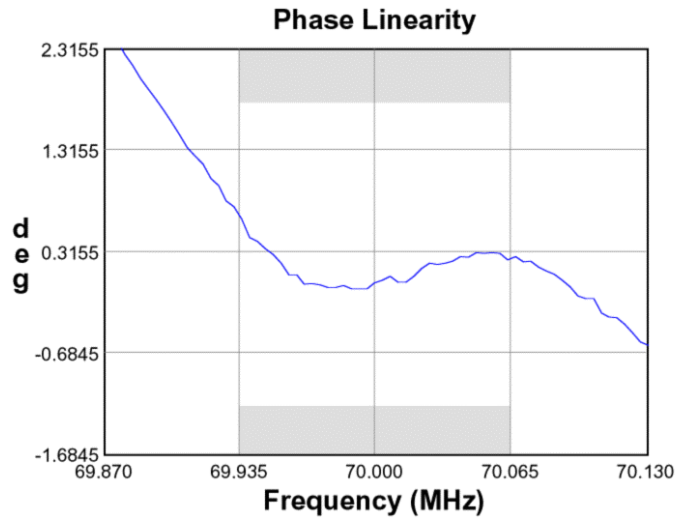
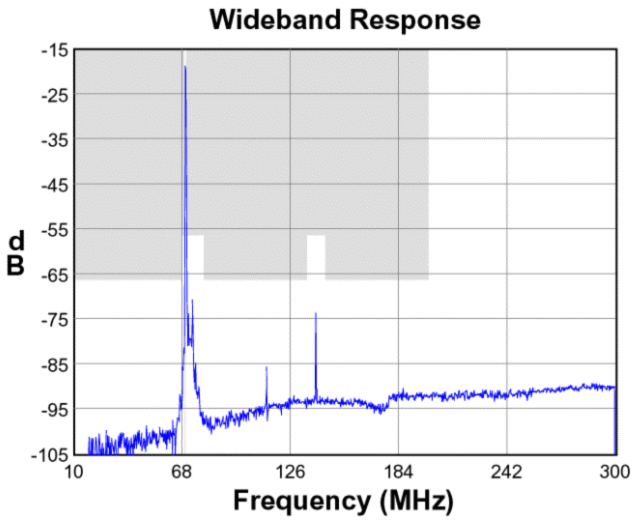
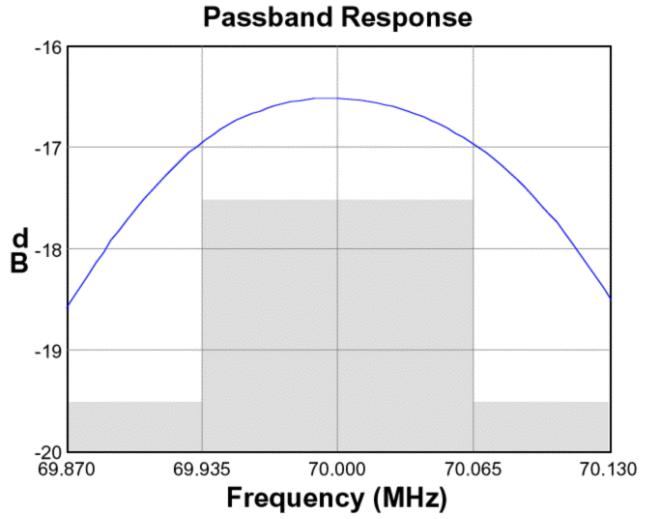
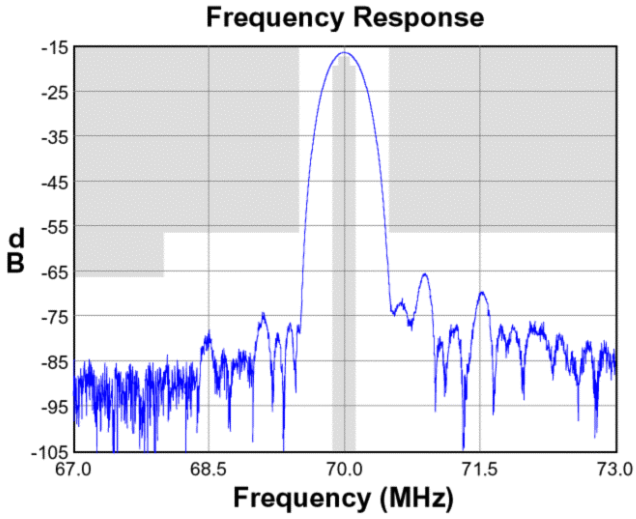
**Test Circuit:**

Actual matching values may vary due to PCB layout and parasitics

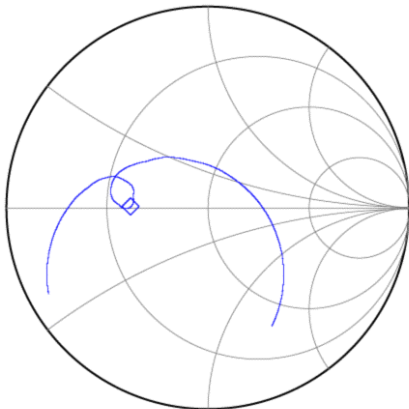


**Data Sheet**

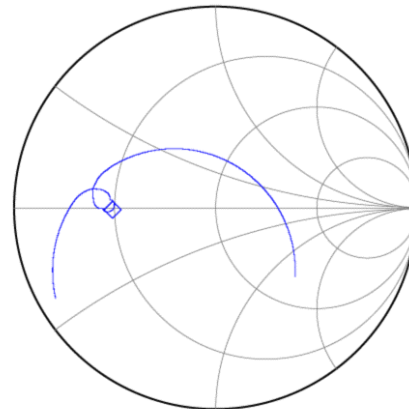
**Typical Performance (at +25°C)**



**Input Smith Chart**



**Output Smith Chart**






# Data Sheet

## Maximum Ratings


Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	-	+85	°C

## Important Notes

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

### Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

## Links to Additional Technical Information

[PCB Layout Tips](#)
[Qualification Flowchart](#)
[Soldering Profile](#)
[S-Parameters](#)
[RoHS Information](#)
[Other Technical Information](#)

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