Voltage Detector IC Series

Low Voltage Free Delay Time Setting CMOS Voltage Detector IC Series

BU42xx series　BU43xx series

●General Description

ROHM's BU42xx and BU43xx series are CMOS Voltage Detector ICs with adjustable output delay. It is a high-accuracy, low current consumption Voltage Detector IC series with a built-in delay circuit. The lineup was established with two output types (Nch open drain and CMOS output) and detection voltages range from 0.9V to 4.8V in increments of 0.1V, so that the series may be selected according to application.

●Features

- Delay Time Controlled by external Capacitor
- Two output types (Nch open drain and CMOS output)
- Ultra-low current consumption
- Wide operating temperature range
- Very small and low height package
- Package SSOP5 and SOP4 is similar to SOT-23-5 and SC-82 respectively (JEDEC)

●Key Specifications

- Detection voltage: 0.9V to 4.8V (Typ.) 0.1V steps
- High accuracy detection voltage: ±1.0%
- Ultra-low current consumption: 0.55μA (Typ.)
- Operating temperature range: -40°C to +125°C

●Package

SSOP5:  2.90mm x 2.80mm x 1.25mm

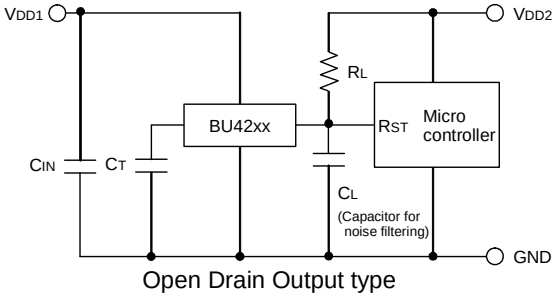
SOP4:  2.00mm x 2.10mm x 0.95mm

VSOF5:  1.60mm x 1.60mm x 0.60mm

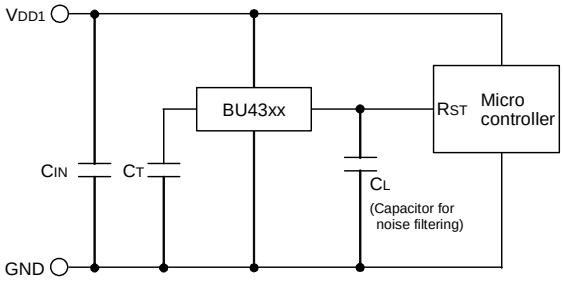
●Applications

Circuits using microcontrollers or logic circuits that require a reset.

●Typical Application Circuit



Open Drain Output type
BU42xx series

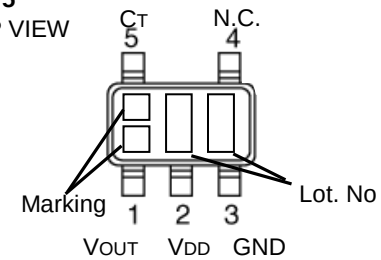


CMOS Output type
BU43xx series

●Connection Diagram & Pin Descriptions

SSOP5

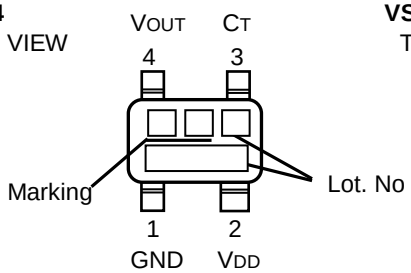
TOP VIEW



PIN No.	Symbol	Function
1	VOUT	Reset output
2	VDD	Power supply voltage
3	GND	GND
4	N.C.	Unconnected terminal
5	CT	Capacitor connection terminal for output delay time

SOP4

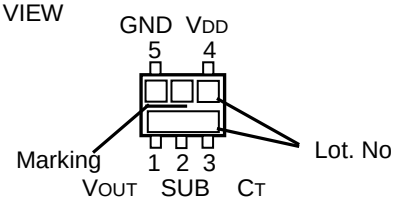
TOP VIEW



PIN No.	Symbol	Function
1	GND	GND
2	VDD	Power supply voltage
3	CT	Capacitor connection terminal for output delay time
4	VOUT	Reset output

VSOF5

TOP VIEW



PIN No.	Symbol	Function
1	VOUT	Reset output
2	SUB	Substrate*
3	CT	Capacitor connection terminal for output delay time
4	VDD	Power supply voltage
5	GND	GND

*Connect the substrate to VDD

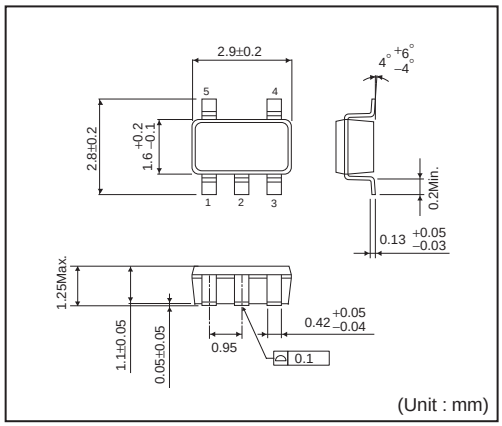
○Product structure：Silicon monolithic integrated circuit　○This product is not designed for protection against radioactive rays

●**Ordering Information**

B	U	x	x	x	x	x	-	T	R

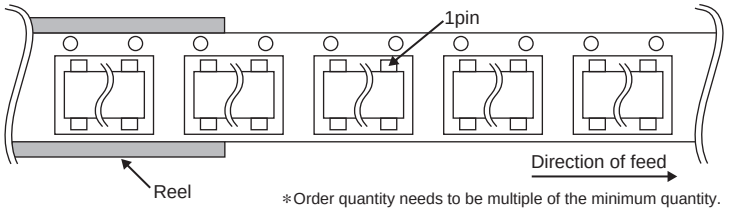
Part Number	Output Type	Reset Voltage Value	Package	Packaging and forming specification
	42 : Open Drain 43 : CMOS	09 : 0.9V ⇩ 0.1V step 48 : 4.8V	G : SSOP5 F : SOP4 FVE : VSOF5	TR : Embossed tape and reel

SSOP5



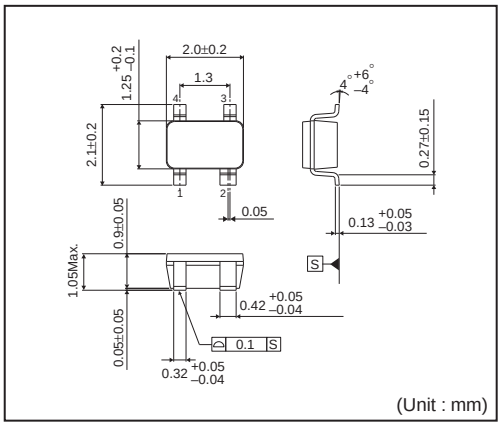
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

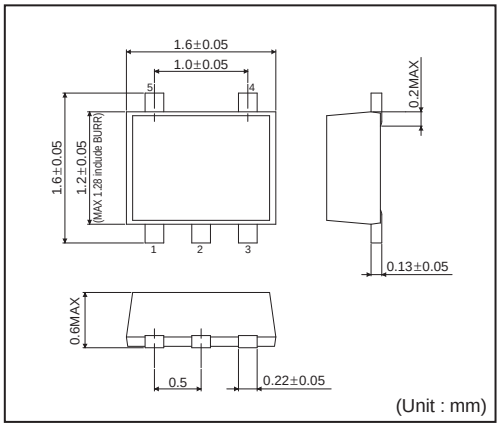


∗Order quantity needs to be multiple of the minimum quantity.

SOP4



VSOF5



●**Lineup**

Output Type	Open Drain		CMOS	
Detection Voltage	Marking	Part Number	Marking	Part Number
4.8V	ZR	BU4248	1H	BU4348
4.7V	ZQ	BU4247	1G	BU4347
4.6V	ZP	BU4246	1F	BU4346
4.5V	ZN	BU4245	1E	BU4345
4.4V	ZM	BU4244	1D	BU4344
4.3V	ZL	BU4243	1C	BU4343
4.2V	ZK	BU4242	1B	BU4342
4.1V	ZJ	BU4241	1A	BU4341
4.0V	ZH	BU4240	0Z	BU4340
3.9V	ZG	BU4239	0Y	BU4339
3.8V	ZF	BU4238	0X	BU4338
3.7V	ZE	BU4237	0W	BU4337
3.6V	ZD	BU4236	0V	BU4336
3.5V	ZC	BU4235	0U	BU4335
3.4V	ZB	BU4234	0T	BU4334
3.3V	ZA	BU4233	0S	BU4333
3.2V	YZ	BU4232	0R	BU4332
3.1V	YY	BU4231	0Q	BU4331
3.0V	YX	BU4230	0P	BU4330
2.9V	YW	BU4229	0N	BU4329
2.8V	YV	BU4228	0M	BU4328
2.7V	YU	BU4227	0L	BU4327
2.6V	YT	BU4226	0K	BU4326
2.5V	YS	BU4225	0J	BU4325
2.4V	YR	BU4224	0H	BU4324
2.3V	YQ	BU4223	0G	BU4323
2.2V	YP	BU4222	0F	BU4322
2.1V	YN	BU4221	0E	BU4321
2.0V	YM	BU4220	0D	BU4320
1.9V	YL	BU4219	0C	BU4319
1.8V	YK	BU4218	0B	BU4318
1.7V	YJ	BU4217	0A	BU4317
1.6V	YH	BU4216	ZZ	BU4316
1.5V	YG	BU4215	ZY	BU4315
1.4V	YF	BU4214	ZX	BU4314
1.3V	YE	BU4213	ZW	BU4313
1.2V	YD	BU4212	ZV	BU4312
1.1V	YC	BU4211	ZU	BU4311
1.0V	YB	BU4210	ZT	BU4310
0.9V	YA	BU4209	ZS	BU4309

●**Absolute Maximum Ratings**

Parameter		Symbol	Limit	Unit
Power Supply Voltage		V_{DD}	-0.3 to +7	V
Output Voltage	Nch Open Drain Output	V_{OUT}	GND-0.3 to +7	V
	CMOS Output		GND-0.3 to V_{DD}+0.3	
Output Current		Io	70	mA
Power Dissipation	SSOP5(SOT-23-5) *1*4	Pd	540	mW
	SOP4(SC-82) *2*4		400	
	VSOF5 *3*4		210	
Operation Temperature Range		Topt	-40 to +125	°C
Ambient Storage Temperature		Tstg	-55 to +125	°C

*1 Reduced by 5.4mW/°C when used over 25°C.
*2 Reduced by 4.0mW/°C when used over 25°C.
*3 Reduced by 2.1mW/°C when used over 25°C.
*4 When mounted on ROHM standard circuit board (70mm×70mm×1.6mm, glass epoxy board).

●**Electrical Characteristics (Unless Otherwise Specified Ta=-25 to 125°C)**

Parameter	Symbol	Condition		Limit Min.	Limit Typ.	Limit Max.	Unit
Detection Voltage	V_{DET}	V_{DD}=H→L, Ta=25°C, R_L=470kΩ		V_{DET}(T) ×0.99	V_{DET}(T)	V_{DET}(T) ×1.01	V
		VDET=1.8V	Ta=+25°C	1.782	1.8	1.818	
			Ta=-40°C to 85°C	1.741	-	1.860	
			Ta=85°C to 125°C	1.718	-	1.883	
		VDET=2.5V	Ta=+25°C	2.475	2.5	2.525	
			Ta=-40°C to 85°C	2.418	-	2.584	
			Ta=85°C to 125°C	2.386	-	2.615	
		VDET=3.0V	Ta=+25°C	2.970	3.0	3.030	
			Ta=-40°C to 85°C	2.901	-	3.100	
			Ta=85°C to 125°C	2.864	-	3.139	
		VDET=3.3V	Ta=+25°C	3.267	3.3	3.333	
			Ta=-40°C to 85°C	3.191	-	3.410	
			Ta=85°C to 125°C	3.150	-	3.452	
		VDET=4.2V	Ta=+25°C	4.158	4.2	4.242	
			Ta=-40°C to 85°C	4.061	-	4.341	
			Ta=85°C to 125°C	4.009	-	4.394	
Circuit Current when ON	I_{DD}1	V_{DD}=V_{DET}-0.2V	V_{DET} =0.9 to 1.3V	-	0.15	0.88	µA
			V_{DET} =1.4 TO 2.1V	-	0.20	1.05	
			V_{DET} =2.2 TO 2.7V	-	0.25	1.23	
			V_{DET} =2.8 to 3.3V	-	0.30	1.40	
			V_{DET} =3.4 to 4.2V	-	0.35	1.58	
			V_{DET} =4.3 to 4.8V	-	0.40	1.75	
Circuit Current when OFF	I_{DD}2	V_{DD}=V_{DET}+2.0V	V_{DET} =0.9 TO 1.3V	-	0.30	1.40	µA
			V_{DET} =1.4 TO 2.1V	-	0.35	1.58	
			V_{DET} =2.2 to 2.7V	-	0.40	1.75	
			V_{DET} =2.8 to 3.3V	-	0.45	1.93	
			V_{DET} =3.4 to 4.2V	-	0.50	2.10	
			V_{DET} =4.3 to 4.8V	-	0.55	2.28	
Operating Voltage Range	V_{OPL}	V_{OL}≤0.4V, Ta=25 to 125°C, R_L=470kΩ		0.70	-	-	V
		V_{OL}≤0.4V, Ta=-40 to 25°C, R_L=470kΩ		0.90	-	-	
'High' Output Voltage (Pch)	V_{OH}	V_{DD}=4.8V, I_{SOURCE}=1.7 mA, V_{DET}=0.9V to 3.9V		VDD-0.5	-	-	V
		V_{DD}=6.0V, I_{SOURCE}=2.0 mA, V_{DET}=4.0V to 4.8V		VDD-0.5	-	-	V
'Low' Output Voltage (Nch)	V_{OL}	V_{DD}=0.85V, I_{SINK} = 20 µA		-	-	0.05	V
		V_{DD}=1.5V, I_{SINK} = 1 mA, V_{DET}=1.7 to 4.8V		-	-	0.5	V
		V_{DD}=2.4V, I_{SINK} = 3.6 mA, V_{DET}=2.7 to 4.8V		-	-	0.5	

*1: Design Guarantee. (Outgoing inspection is not done on all products.)
V_{DET}(T) : Standard Detection Voltage (0.9V to 4.8V, 0.1V step)
R_L: Pull-up resistor to be connected between V_{OUT} and power supply.

●**Electrical Characteristics (Unless Otherwise Specified Ta=-25 to 125°C) - continued**

Parameter	Symbol	Condition		Limit			Unit
				Min.	Typ.	Max.	
Leak Current when OFF	I_{leak}	V_{DD}=V_{DS}=7V Ta=-40 to 85°C		-	0	0.1	μA
		V_{DD}=V_{DS}=7V Ta=85 to 125°C		-	0	1	
CT pin Threshold Voltage	V_{CTH}	V_{DD}=V_{DET}×1.1, V_{DET}=0.9 to 2.5V Ta=25°C R_L=470kΩ		V_{DD} ×0.35	V_{DD} ×0.45	V_{DD} ×0.55	V
		V_{DD}=V_{DET}×1.1, V_{DET}=2.6 to 4.8V Ta=25°C R_L=470kΩ		V_{DD} ×0.40	V_{DD} ×0.50	V_{DD} ×0.60	
Output Delay Resistance	R_{CT}	V_{DD}=V_{DET}×1.1 V_{CT}=0.5V Ta=25°C *1		9	10	11	MΩ
CT pin Output Current	I_{CT}	V_{CT}=0.1V V_{DD}=0.85V		5	40	-	μA
		V_{CT}=0.5V V_{DD}=1.5V V_{DET}=1.7 to 4.8V		200	400	-	
Detection Voltage Temperature coefficient	V_{DET}/ΔT	Ta=-40°C to 125°C		-	±30	-	ppm/°C
Hysteresis Voltage	ΔVDET	V_{DD}=L→H→L Ta=-40 to 125°C R_L=470kΩ	V_{DET}≤1.0V	V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.08	V
			V_{DET}≥1.1V	V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.07	

*1: Design Guarantee. (Outgoing inspection is not done on all products.)
V_{DET}(T) : Standard Detection Voltage (0.9V to 4.8V, 0.1V step)
R_L: Pull-up resistor to be connected between V_{OUT} and power supply.

●**Block Diagrams**

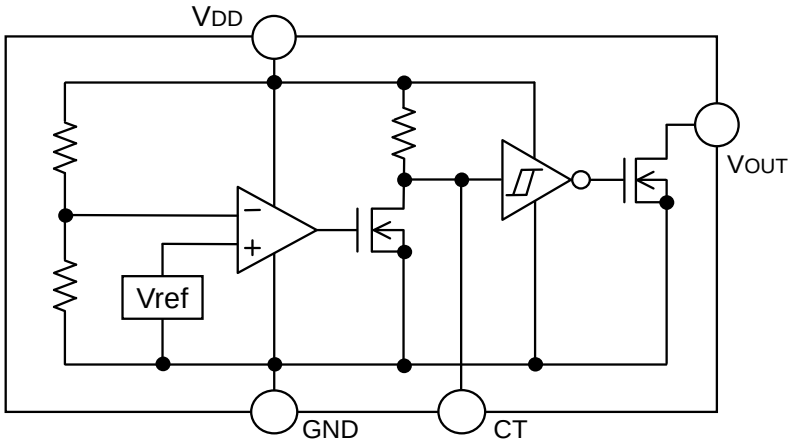


Fig.1 BU42xx Series

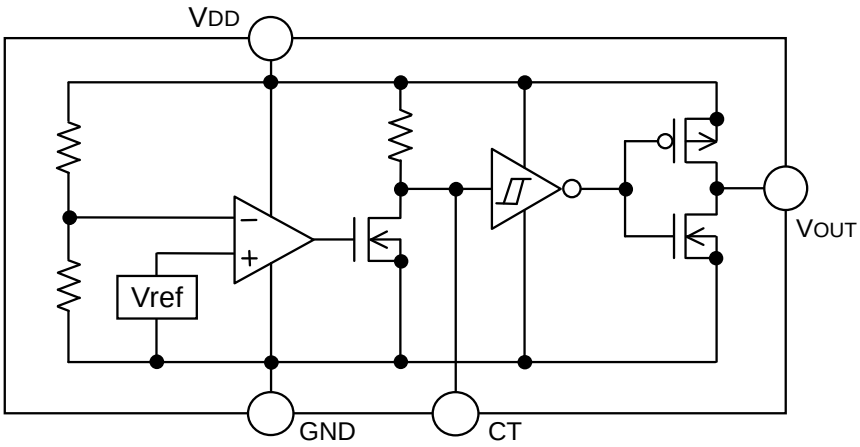


Fig.2 BU43xx Series

●**Typical Performance Curves**

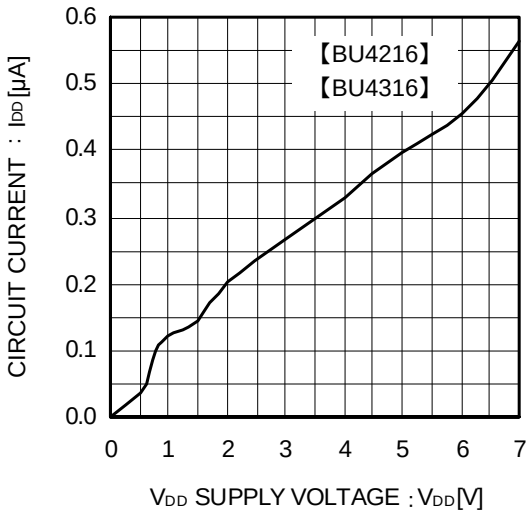


Fig.3 Circuit Current

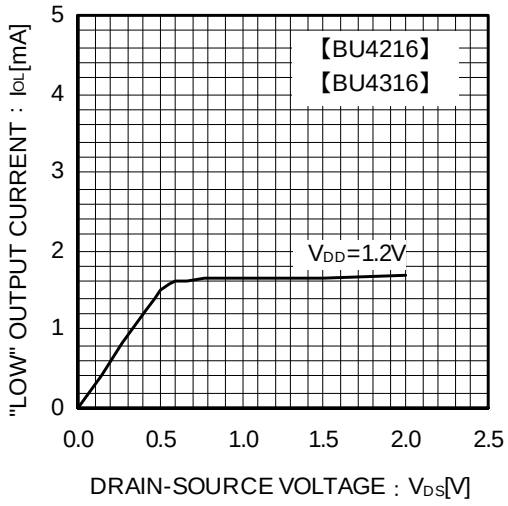


Fig.4 “LOW” Output Current

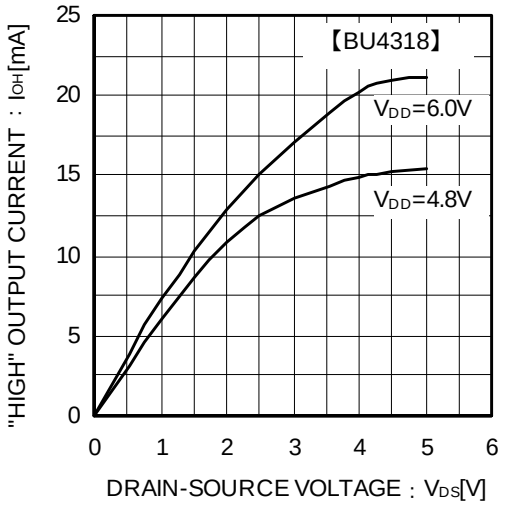


Fig.5 “High” Output Current

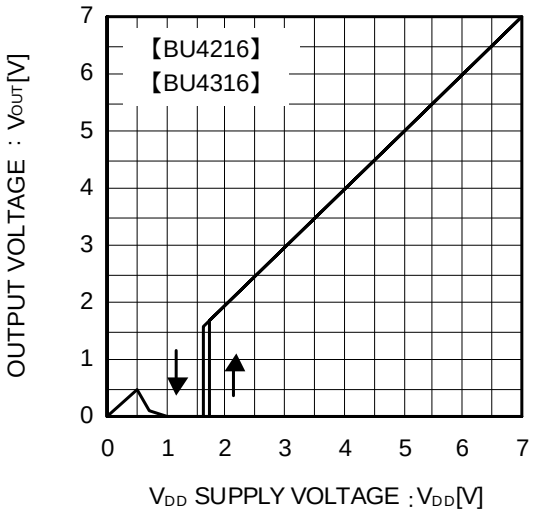


Fig.6 I/O Characteristics

●**Typical Performance Curves – continued**

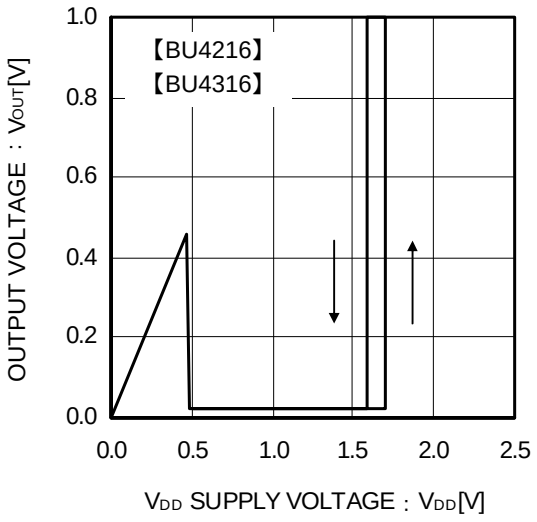


Fig.7 Operating Limit Voltage

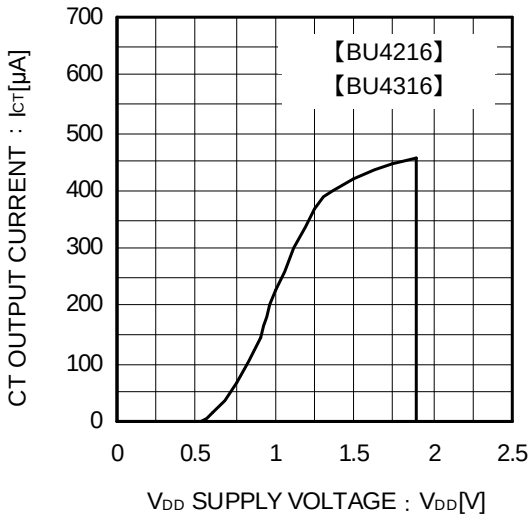


Fig.8 CT Terminal Current

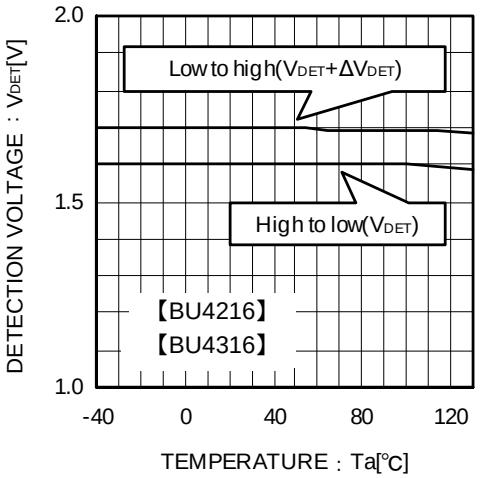


Fig.9 Detecting Voltage
Release Voltage

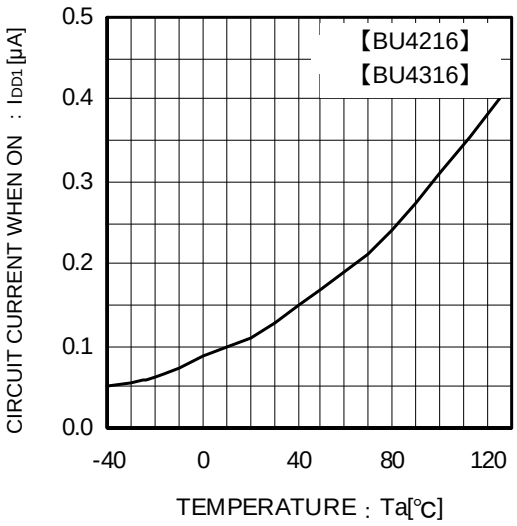


Fig.10 Circuit Current when ON

●**Typical Performance Curves – continued**

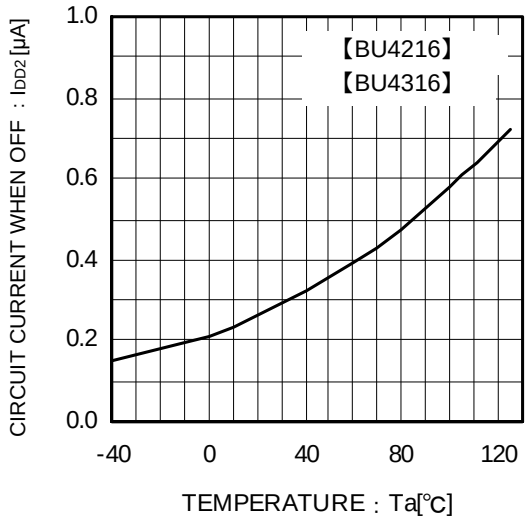


Fig.11 Circuit Current when OFF

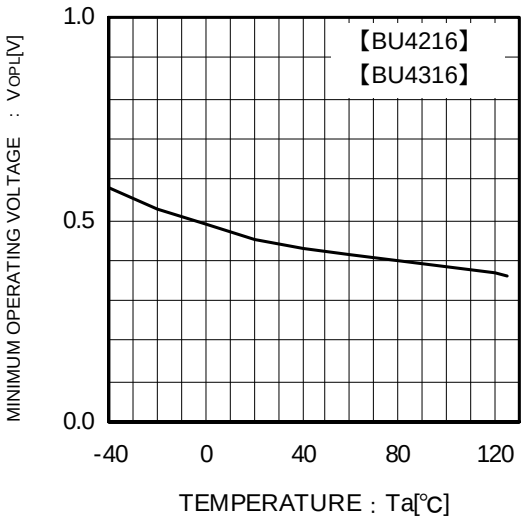


Fig.12 Operating Limit Voltage

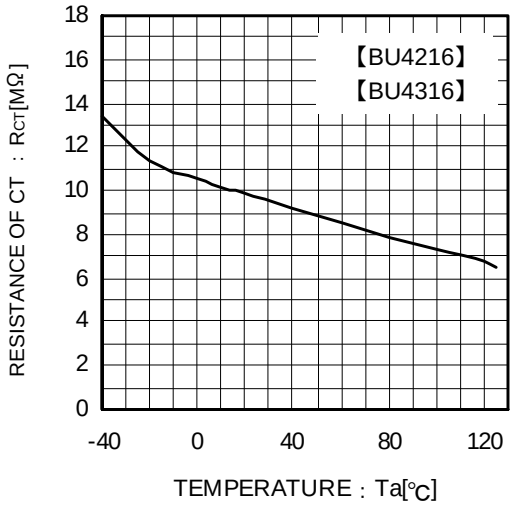


Fig.13 C_T Terminal Circuit Resistance

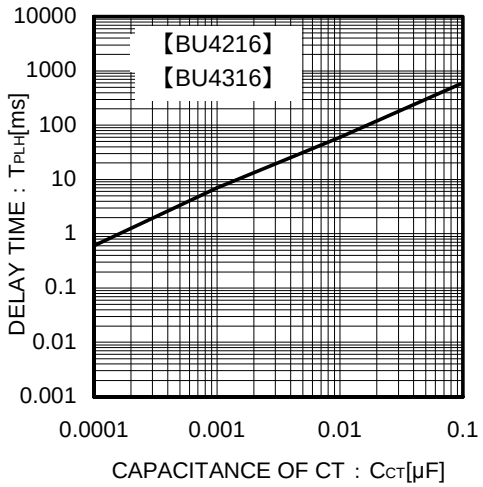


Fig.14 Delay Time (t_{PLH}) and C_T Terminal External Capacitance

●Application Information

Explanation of Operation

For both the open drain type (Fig.15) and the CMOS output type (Fig.16), the detection and release voltages are used as threshold voltages. When the voltage applied to the V_{DD} pins reaches the applicable threshold voltage, the V_{OUT} terminal voltage switches from either “High” to “Low” or from “Low” to “High”. BU42xx and BU43xx series have delay time function which set t_{PLH} (Output “Low”→”High”) using an external capacitor (C_{CT}). Because the BU42xx series uses an open drain output type, it is necessary to connect a pull-up resistor to V_{DD} or another power supply if needed [The output “High” voltage (V_{OUT}) in this case becomes V_{DD} or the voltage of the other power supply].

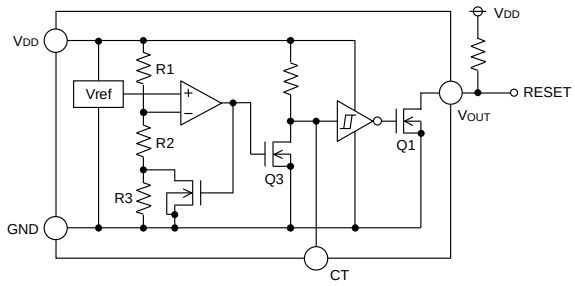


Fig.15 (BU42xx series Internal Block Diagram)

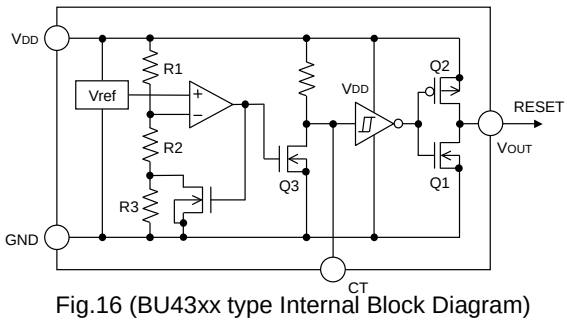


Fig.16 (BU43xx type Internal Block Diagram)

Setting of Detector Delay Time

The delay time of this detector IC can be set at the rise of V_{DD} by the capacitor connected to C_T terminal.

Delay time at the rise of V_{DD} t_{PLH}:Time until when V_{OUT} rises to 1/2 of V_{DD} after V_{DD} rises up and beyond the release voltage($V_{DET}+\Delta V_{DET}$)

$$T_{PLH}=-1\times C_{CT}\times R_{CT}\times \ln\left(\frac{V_{DD}-V_{CTH}}{V_{DD}}\right)$$

C_{CT}: C_T pin Externally Attached Capacitance
R_{CT}: C_T pin Internal Impedance(P.3 R_{CT} refer.)
V_{CTH}: C_T pin Threshold Voltage(P.3 V_{CTH} refer.)
In: Natural Logarithm

Reference Data of Falling Time (t_{PHL}) Output

Examples of Falling Time (t_{PHL}) Output

Part Number	t_{PHL} [µs]
BU4245	275.7
BU4345	359.3

* This data is for reference only.
The figures will vary with the application, so please confirm the actual operating conditions before use.

Timing Waveforms

Example: The following shows the relationship between the input voltage V_{DD}, the C_T Terminal Voltage V_{CT} and the output voltage V_{OUT} when the input power supply voltage V_{DD} is made to sweep up and sweep down (The circuits are shown in Fig.15 and 16).

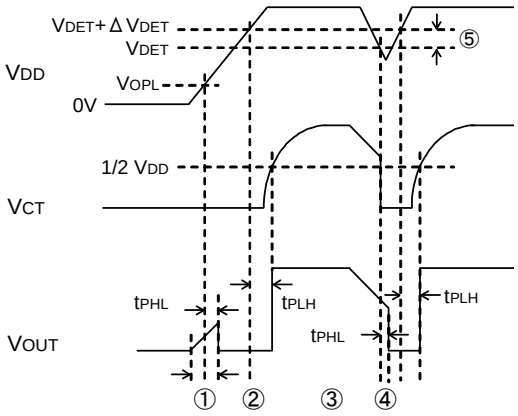


Fig.17 Timing Waveforms

① When the power supply is turned on, the output is unstable from after over the operating limit voltage (V_{OPL}) until t_{PHL}. Therefore, it is possible that the reset signal is not outputted when the rise time of V_{DD} is faster than t_{PHL}.

② When V_{DD} is greater than V_{OPL} but less than the reset release voltage ($V_{DET}+\Delta V_{DET}$), the C_T terminal (V_{CT}) and output (V_{OUT}) voltages will switch to L.

③ If V_{DD} exceeds the reset release voltage ($V_{DET}+V_{DET}$), then V_{OUT} switches from L to H (with a delay to the C_T terminal).

④ If V_{DD} drops below the detection voltage (V_{DET}) when the power supply is powered down or when there is a power supply fluctuation, V_{OUT} switches to L (with a delay of t_{PHL}).

⑤ The potential difference between the detection voltage and the release voltage is known as the hysteresis width (V_{DET}). The system is designed such that the output does not toggle with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

●**Circuit Applications**

1) Examples of common power supply detection reset circuits

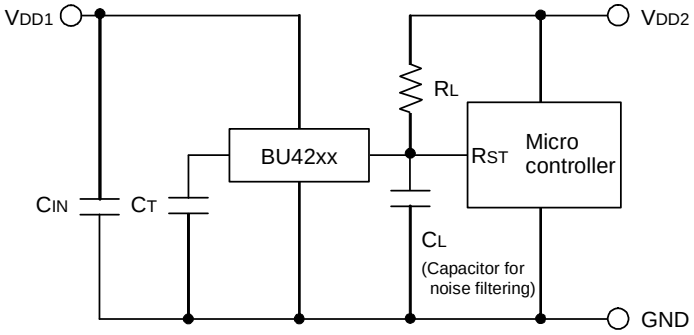


Fig.18 Open Drain Output type

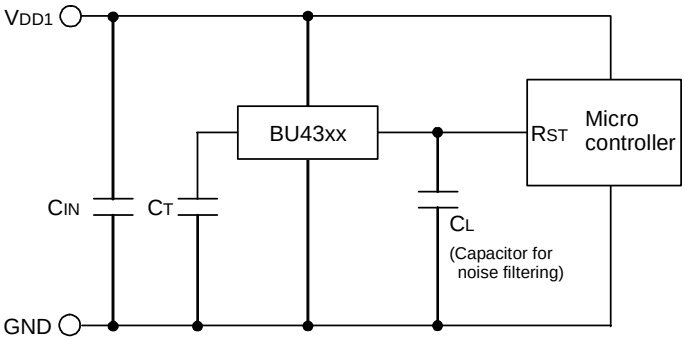


Fig.19 CMOS Output type

Application examples of BU42xx series (Open Drain output type) and BU43xx series (CMOS output type) are shown below.

CASE1: Power supply of microcontroller ($V_{DD}2$) differs from the power supply of the reset detection ($V_{DD}1$). Use an open drain output Type (BU42xx series) device with a load resistance R_L as shown Fig.18.

CASE2: Power supply of microcontroller ($V_{DD}1$) is the same as the power supply of the reset detection ($V_{DD}1$). Use a CMOS output type (BU43xx series) device or an open drain output type (BU42xx series) device with a pull up resistor between the output and $V_{DD}1$.

When a capacitance C_L for noise filtering is connected to V_{OUT} pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall time of the output voltage (V_{OUT}).

2) The following is an example of a circuit application in which an OR connection between two types of detection voltage resets the microcontroller.

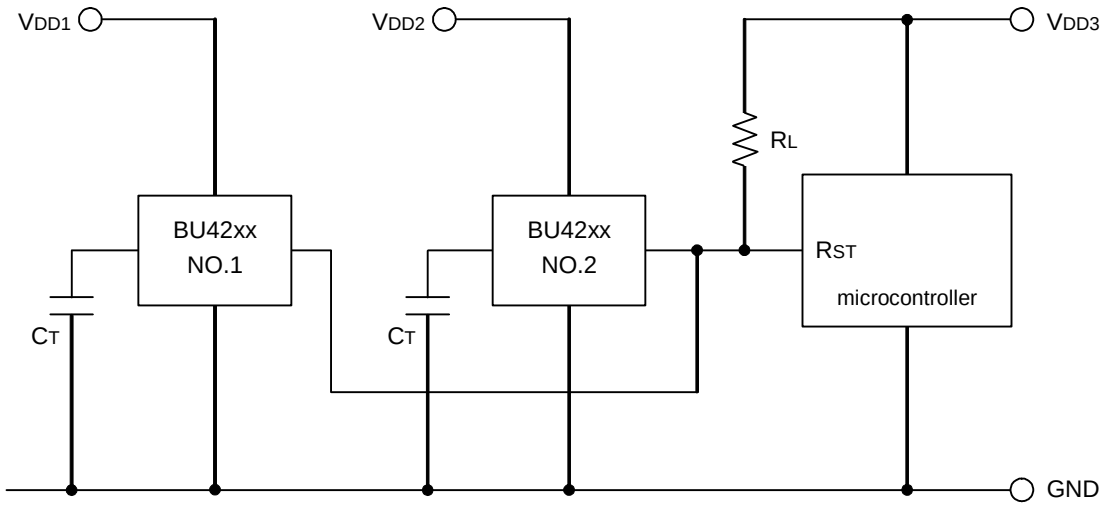


Fig.20

To reset the microcontroller when many independent power supplies are used in the system, OR connect an open drain output type (BU42xx series) to the microcontroller's input with pull-up resistor to the supply voltage of the microcontroller (V_{DD3}) as shown in Fig. 20. By pulling-up to V_{DD3}, output "High" voltage of micro-controller power supply is possible.

3) Examples of the power supply with resistor dividers

In applications wherein the power supply input terminal (VDD) of an IC has resistor dividers, it is possible that an in-rush current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillations).

(In-rush current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from “High” to “Low” or vice versa.)

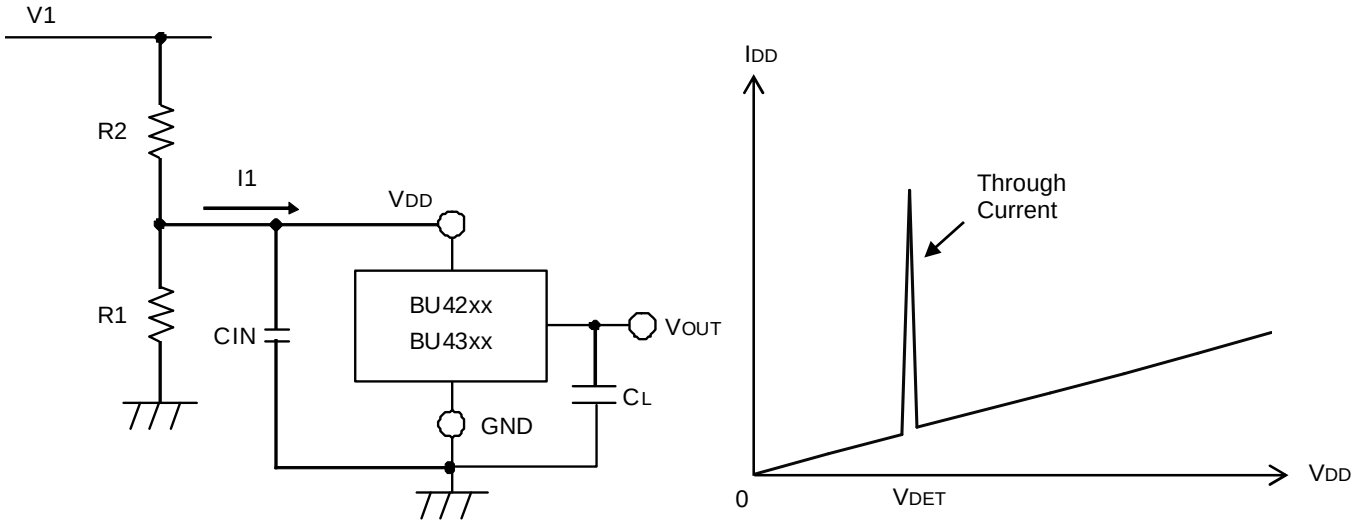


Fig.21

A voltage drop [in-rush current (I1)] × [input resistor (R2)] is caused by the in-rush current, and causes the input voltage to drop when the output switches from “Low” to “High”. When the input voltage decreases and falls below the detection voltage, the output voltage switches from “High” to “Low”. At this time, the in-rush current stops flowing through output “Low”, and the voltage drop is reduced. As a result, the output switches from “Low” to “High”, which again causes the in-rush current to flow and the voltage to drop. This operation repeats and will result to oscillation.

Consider the use of BD52xx when the power supply input has resistor dividers.

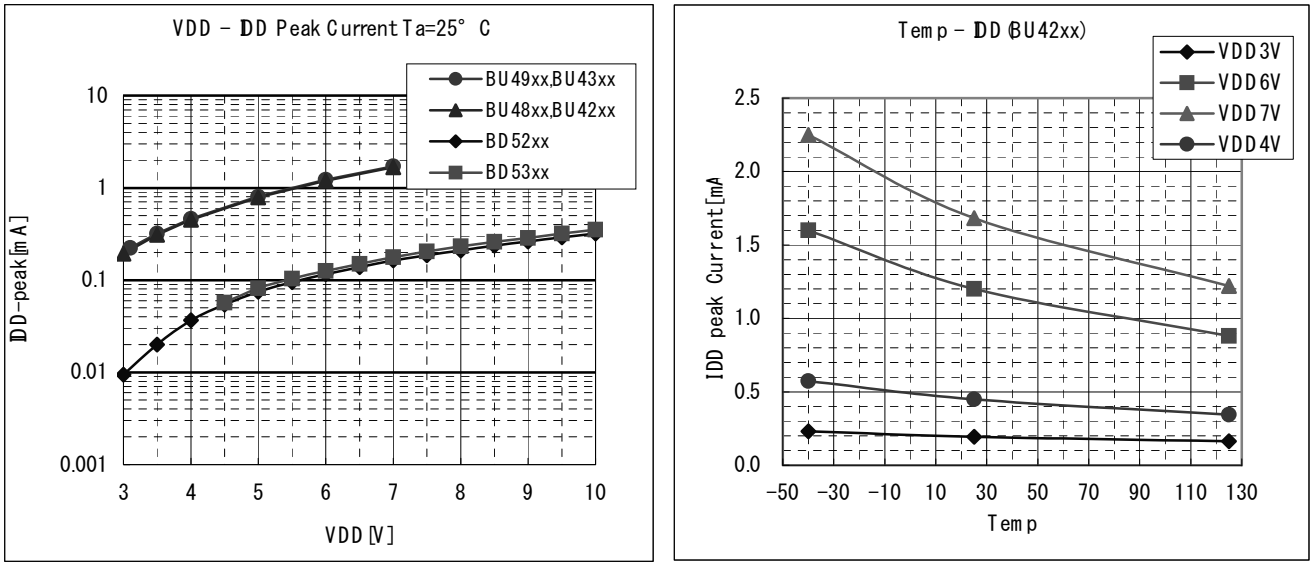


Fig.22 Current Consumption vs. Power Supply Voltage

* This data is for reference only.

The figures will vary with the application, so please confirm the actual operating conditions before use.

●Operational Notes

1) Absolute maximum ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

2) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

3) Recommended operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

4) Bypass Capacitor for Noise Rejection
To help reject noise, put a 1µF capacitor between V_{DD} pin and GND and 1000pF capacitor between V_{OUT} pin and GND. Be careful when using extremely big capacitor as transient response will be affected.

5) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

6) Operation under strong electromagnetic field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

7) The V_{DD} line impedance might cause oscillation because of the detection current.

8) A V_{DD} to GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

9) Lower than the mininum input voltage puts the V_{OUT} in high impedance state, and it must be V_{DD} in pull up (V_{DD}) condition.

10) External parameters
The case of needless “Delay Time”, recommended to insert more 470kΩ resister between V_{DD} and C_T. The recommended value of R_L Resistor is over 50kΩ to 1MΩ for V_{DET}=1.5V to 4.8V, and over 100kΩ to 1MΩ for V_{DET}=0.9V to 1.4V. The recommended value of C_T Capacitor is over 100pF to 0.1µF. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

11) Power on reset operation
Please note that the power on reset output varies with the V_{DD} rise time. Please verify the behavior in the actual operation.

12) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC’s power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

13) Rush current
When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

14) C_T pin discharge
Due to the capabilities of the C_T pin discharge transistor, the C_T pin may not completely discharge when a short input pulse is applied, and in this case the delay time may not be controlled. Please verify the actual operation.

15) This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the C_T terminal and the GND terminal, 1MΩ connection between the CT terminal and the V_{DD} terminal would be recommended. Also, if the leakage is assumed between the Vout terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance. The value of Rct depends on the external resistor that is connected to C_T terminal, so please consider the delay time that is decided by $t \times R_{CT} \times C_{CT}$ changes.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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