SmartMesh IP Network Manager
2.4GHz 802.15.4e Wireless Manager

NETWORK FEATURES

- Complete Radio Transceiver, Embedded Processor, and Networking Software for Forming a Self-Healing Mesh Network
- SmartMesh® Networks Incorporate:
  - Time Synchronized Network-Wide Scheduling
  - Per-Transmission Frequency-Hopping
  - Redundant Spatially Diverse Topologies
  - Network-Wide Reliability and Power Optimization
  - NIST Certified Security
- SmartMesh Networks Deliver:
  - >99.999% Network Reliability Achieved in the Most Challenging RF Environments
  - Sub 50µA Routing Nodes
- Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

LTC5800-IPR FEATURES

- Provides Network Management Functions and Security Capabilities
- Manages Networks of Up to 100 nodes
- Sub 1mA Average Current Consumption Enables Battery-Powered Network Management
- PCB Module Versions Available (LTP™5901/2-IPR) with RF Modular Certifications
- 72-Lead 10mm × 10mm QFN Package

DESCRIPTION

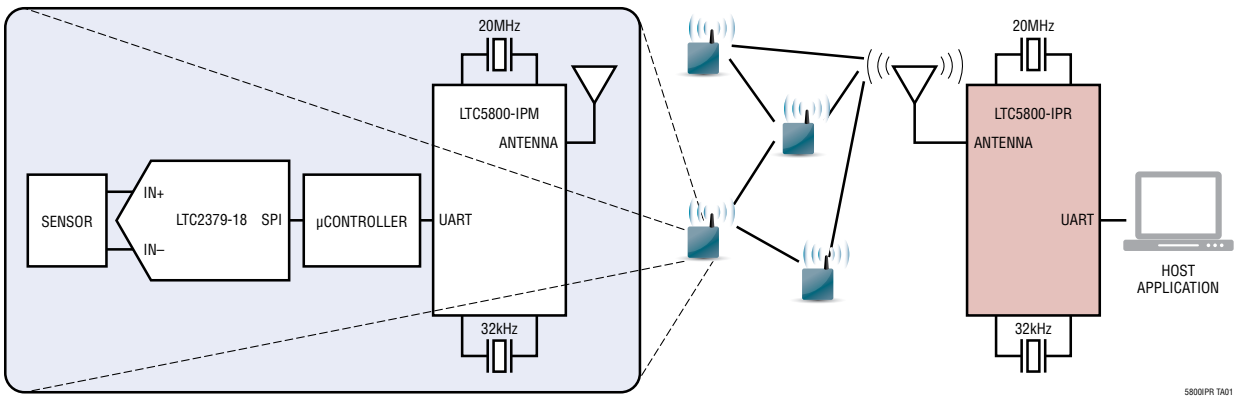
SmartMesh IP™ wireless sensor networks are self managing, low power internet protocol (IP) networks built from wireless nodes called motes. The LTC®5800-IPR is the IP Manager-on-Chip™ in the Eterna®* family of IEEE 802.15.4e system-on-chip (SoC) solutions, featuring a highly integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software.

Based on the IETF 6LoWPAN and IEEE-802.15.4e standards, the LTC5800-IPR SoC runs SmartMesh IP network management software to monitor and manage network performance and provide a data ingress/egress point via a UART interface. The SmartMesh IP software provided with the LTC5800-IPR is fully tested and validated, and is readily configured via a software Application Programming Interface. With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery-powered operation.

SmartMesh IP motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION



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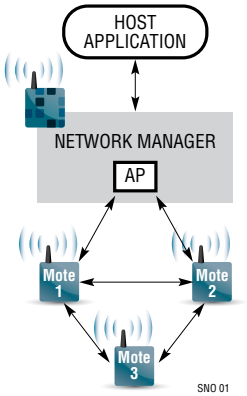
SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop, mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into time slots, which enable collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g., mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

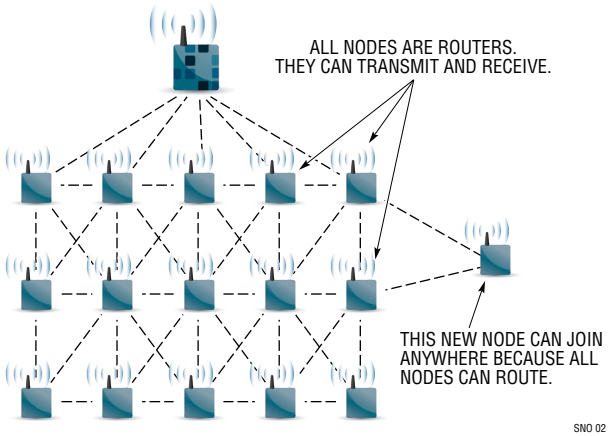
A network begins to form when the network manager instructs its on-board access point (AP) radio to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.



An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g., quality of used paths, and lists of potential paths) and periodically sends that information to the network manager in packets called health reports.

The network manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments.

The use of TSCH allows SmartMesh devices to sleep in-between scheduled communications and draw very little power in this state. Motes are only active in time slots where they are scheduled to transmit or receive, typically resulting in a duty cycle of <1%. The optimization software in the Network Manager coordinates this schedule automatically. When combined with the Eterna low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.



At the heart of SmartMesh motes and network managers is the Eterna IEEE 802.15.4e system-on-chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of application programming interfaces (APIs) which allows a host application to interact with the network, e.g., to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed.

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ABSOLUTE MAXIMUM RATINGS

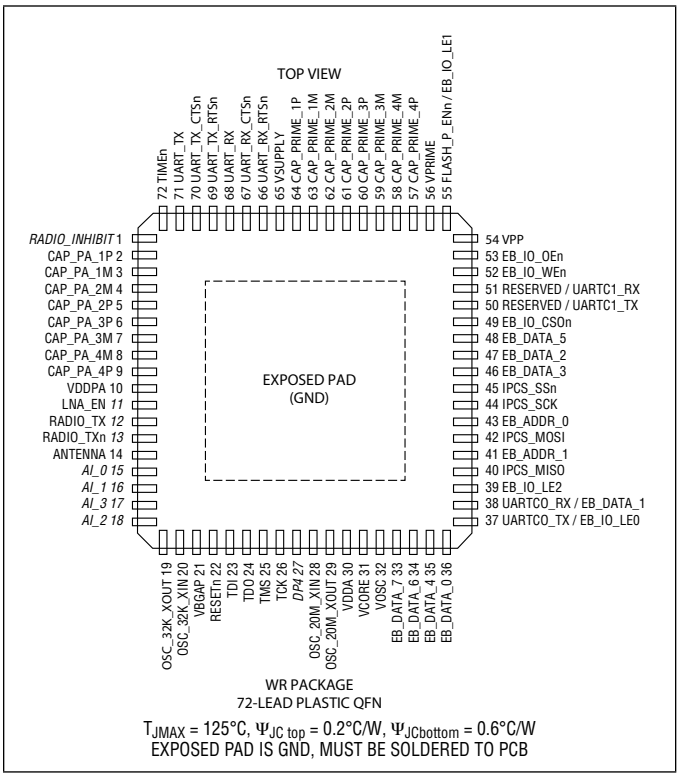
(Note 1)

Supply Voltage on VSUPPLY 4.20V
Input Voltage on AI_0/1/2/3 Inputs 1.80V
Voltage on Any Digital I/O pin ..–0.3V to VSUPPLY + 0.3V
Input RF Level 10dBm
Storage Temperature Range (Note 3) ..... –55°C to 125°C
Junction Temperature (Note 3) ..... 125°C
Operating Temperature Range
LTC5800I ..... –40°C to 85°C
LTC5800H ..... –55°C to 105°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTC5800-IPR.

PIN CONFIGURATION

Pin functions shown in italics are currently not supported in software.



WR PACKAGE
72-LEAD PLASTIC QFN

T_{JMAX} = 125°C, $\Psi_{JC\ top}$ = 0.2°C/W, $\Psi_{JCbottom}$ = 0.6°C/W
EXPOSED PAD IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC5800IWR-IPMA#PBF	LTC5800WR-IPMA	72-Lead (10mm × 10mm × 0.85mm) Plastic QFN	–40°C to 85°C
LTC5800HWR-IPMA#PBF	LTC5800WR-IPMA	72-Lead (10mm × 10mm × 0.85mm) Plastic QFN	–55°C to 105°C

For legacy part numbers and ordering information go to: http://www.linear.com/product/LTC5800-IPR#orderinfo.
*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VSUPPLY	Supply Voltage	Including Noise and Load Regulation	●	2.1		3.76	V
	Supply Noise	Requires Recommended RLC Filter, 50Hz to 2MHz	●			250	mV
	Operating Relative Humidity	Non-Condensing	●	10		90	% RH
	Temperature Ramp Rate While Operating in Network	–40°C ≤ Temperature ≤ 85°C Temperature > 85°C or Temperature < –40°C		–8 –2		8 2	°C/Min °C/Min

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

OPERATION/STATE	CONDITIONS		MIN	TYP	MAX	UNITS
Power-On Reset	During Power-On Reset, Maximum 750µs + VSUPPLY Rise Time from 1V to 1.9V			12		mA
Doze	RAM On, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Active			1.2		µA
Deep Sleep	RAM On, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Inactive			0.8		µA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK at 8MHz			20		mA
Peak Operating Current 8dBm 0dBm	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum Duration 4.33ms			 30 26		 mA mA
Active	ARM Cortex M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 7.3728MHz, V_{CORE} = 1.2V			1.3		mA
Flash Write	Single Bank Flash Write			3.7		mA
Flash Erase	Single Bank Page or Mass Erase			2.5		mA
Radio Tx +0dBm (LTC5800I) +0dBm (LTC5800H) +8dBm (LTC5800I) +8dBm (LTC5800H)	Current With Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 5.4 5.6 9.7 9.9		 mA mA mA mA
Radio Rx LTC5800I LTC5800H	Current With Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 4.5 4.7		 mA mA

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where k = 11 to 25, as Defined by IEEE.802.15.4	●		2405 + 5 •(k – 11)		MHz
Modulation	IEEE 802.15.4 Direct Sequence Spread Spectrum (DSSS)					
Raw Data Rate		●		250		kbps
Antenna Pin ESD Protection	HBM Per JEDEC JESD22-A114F			±1000		V
Range (Note 4) Indoor Outdoor Free Space	25°C, 50% RH, 2dBi Omni-Directional Antenna, Antenna 2m Above Ground			 100 300 1200		 m m m

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)		–93		dBm
Receiver Sensitivity	PER = 50%		–95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets		0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)		22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)		19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)		40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)		36		dBc
Second Alternate Channel Rejection	Desired Signal at –82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)		42		dBc
Co-Channel Rejection	Desired Signal at –82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%		–6		dBc
LO Feed Through			–55		dBm
Frequency Error Tolerance (Note 6)			±50		ppm
Symbol Error Tolerance			±50		ppm
Received Signal Strength Indicator (RSSI) Input Range			–90 to –10		dBm
RSSI Accuracy			±6		dB
RSSI Resolution			1		dB

RADIO TRANSMITTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power	Delivered to a 50Ω load				
High Calibrated Setting			8		dBm
Low Calibrated Setting			0		dBm
Spurious Emissions	Conducted Measurement with a 50Ω Single-Ended Load, 8dBm Output Power. All Measurements Made with Max Hold. RF Implementation Per Eterna Reference Design				
30MHz to 1000 MHz	RBW = 120kHz, VBW = 100Hz		<–70		dBm
1GHz to 12.75GHz	RBW = 1MHz, VBW = 3MHz		–45		dBm
2.4GHz ISM Upper Band Edge (Peak)	RBW = 1MHz, VBW = 3MHz		–37		dBm
2.4GHz ISM Upper Band Edge (Average)	RBW = 1MHz, VBW = 10Hz		–49		dBm
2.4GHz ISM Lower Band Edge	RBW = 100kHz, VBW = 100kHz		–45		dBc
Harmonic Emissions	Conducted Measurement Delivered to a 50Ω Load, Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz. RF Implementation Per Eterna Reference Design				
2nd Harmonic			–50		dBm
3rd Harmonic			–45		dBm

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		●	–0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{OL(MAX)}$ = 1.2mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{OH(MAX)}$ = –0.8mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 2, Low Drive, $I_{OL(MAX)}$ = 2.2mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 2, Low Drive, $I_{OH(MAX)}$ = –1.6mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 2, High Drive, $I_{OL(MAX)}$ = 4.5mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 2, High Drive, $I_{OH(MAX)}$ = –3.2mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	Input Leakage Current	Input Driven to VSUPPLY or GND			50		nA
	Pull-Up/Pull-Down Resistance				50		kΩ

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C			±0.25		°C
Slope Error				±0.033		°C/°C

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Doze to Active State Transition				5		µs
	Doze to Radio Tx or Rx				1.2		ms
Q_{CCA}	Charge to Sample RF Channel RSSI	Charge Consumed Starting from Doze State and Completing an RSSI Measurement			4		µC
Q_{MAX}	Largest Atomic Charge Operation	Flash Erase, 21ms Max Duration	●			200	µC
	RESETn Pulse Width		●	125			µs

UART AC CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Permitted Rx Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	–2		2	%
	Generated Tx Baud Rate Error	Both API and CLI UARTs	●	–1		1	%
$t_{RX\_RTS\ to\ RX\_CTS}$	Assertion of UART_RX_RTSn to Assertion of UART_RX_CTSn, or Negation of UART_RX_RTSn to Negation of UART_RX_CTSn		●	0		2	ms
$t_{RX\_CTS\ to\ RX}$	Assertion of UART_RX_CTSn to Start of Byte		●	0		20	ms
$t_{EOP\ to\ RX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_RX_RTSn		●	0		22	ms
$t_{BEG\_TX\_RTS\ to\ TX\_CTS}$	Assertion of UART_TX_RTSn to Assertion of UART_TX_CTSn		●	0		22	ms
$t_{END\_TX\_RTS\ to\ TX\_CTS}$	Negation of UART_TX_RTSn to Negation of UART_TX_CTSn	Mode 2 Only				22	ms
$t_{END\_TX\_CTS\ to\ TX\_RTS}$	Negation of UART_TX_CTSn to Negation of UART_TX_RTSn	Mode 4 Only		2			Bit Period
$t_{TX\_CTS\ to\ TX}$	Assertion of UART_TX_CTSn to Start of Byte		●	0		2	Bit Period
$t_{EOP\ to\ TX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_TX_RTSn		●	0		1	Bit Period
$t_{RX\_INTERBYTE}$	Receive Inter-Byte Delay		●			100	ms
$t_{RX\_INTERPACKET}$	Receive Inter-Packet Delay		●	20			ms
$t_{TX\_INTERPACKET}$	Transmit Inter-Packet Delay		●	1			Bit Period
$t_{TX\ to\ TX\_CTS}$	Start of Byte to Negation of UART_TX_CTSn		●	0			ns

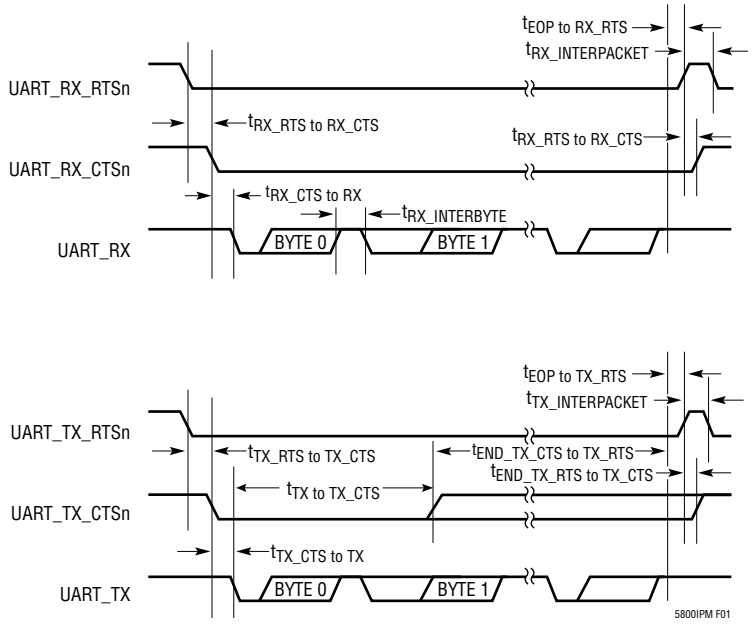


Figure 1. API UART Timing

TIMEn AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{STROBE}	TIMEn Signal Strobe Width		●	125			µs
$t_{RESPONSE}$	Delay from Rising Edge of TIMEn to the Start of Time Packet on API UART		●	0		100	ms
t_{TIME_HOLD}	Delay from End of Time Packet on API UART to Falling Edge of Subsequent TIMEn		●	0			ns
	Timestamp Resolution (Note 9)		●		1		µs
	Network-Wide Time Accuracy (Note 10)		●		±5		µs

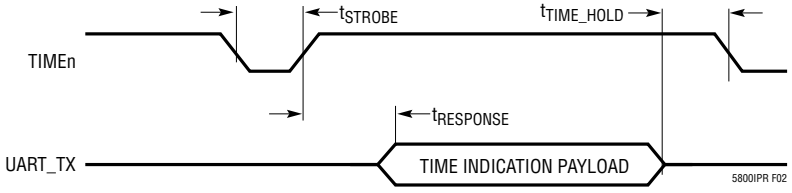


Figure 2. Timestamp Timing

RADIO_INHIBIT AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RADIO_OFF}	Delay from Rising Edge of RADIO_INHIBIT to Radio Disabled		●			20	ms
$t_{RADIO\_INHIBIT\_STROBE}$	Maximum RADIO_INHIBIT Strobe Width		●			2	s

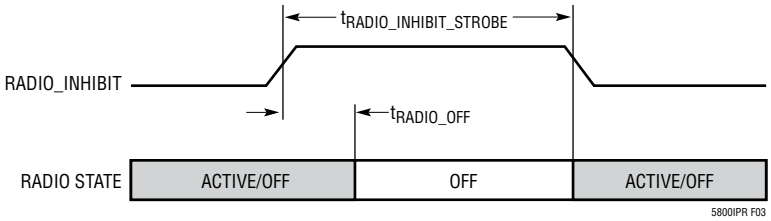


Figure 3. RADIO_INHIBIT Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 11)		●			21	µs
t_{PAGE_ERASE}	Time to Erase a 2kB Page (Note 11)		●			21	ms
t_{MASS_ERASE}	Time to Erase 256kB Flash Bank (Note 11)		●			21	ms
	Data Retention	25°C 85°C 105°C		100 20 8			Years Years Years

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{FP\_EN\_to\_RESET}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0			ns
t_{FP_ENTER}	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125			µs
t_{FP_EXIT}	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn (Note 12)		●	10			µs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15			ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15			ns
t_{CK}	IPCS_SCK Period		●	300			ns
t_{DIS}	IPCS_MOSI Data Setup		●	15			ns
t_{DIH}	IPCS_MOSI Data Hold		●	5			ns
t_{DOV}	IPCS_MISO Data Valid		●	3			ns
t_{OFF}	IPCS_MISO Data Tri-state		●	0		30	ns

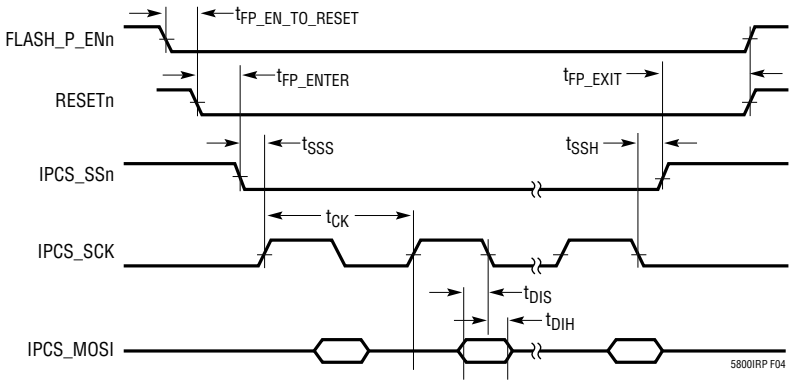


Figure 4. Flash Programming Interface Timing

EXTERNAL BUS AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{LEPW}	EB_IO_LE0, EB_IO_LE1, EB_IO_LE2 Pulse Width		●	100			ns
t_{AH}	EB_DATA_[7:0] Address Hold from the Rising Edge of EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2	EB_DATA_[7:0] During Address Phase	●	90			ns
$t_{AV\_to\_DL}$	EB_ADDR_[1:0] Address Valid Until EB_DATA_[7:0] Data Latched		●	90			ns
$t_{CSn\_to\_OEn}$	EB_CS0n Asserted Until EB_OEn Asserted		●	150			ns
t_{CSn}	EB_CS0n Asserted		●	100			ns
t_{CSn_OFF}	EB_CS0n Negated Between External Bus Transfers		●	100			ns
$t_{SU\_to\_CSn}$	EB_ADDR_[1:0], EB_IO_WEn Setup to EB_CSn Asserted		●	50			ns
$t_{H\_from\_CSn}$	EB_ADDR_[1:0], EB_IO_WEn Hold from EB_CSn Negated		●	50			ns

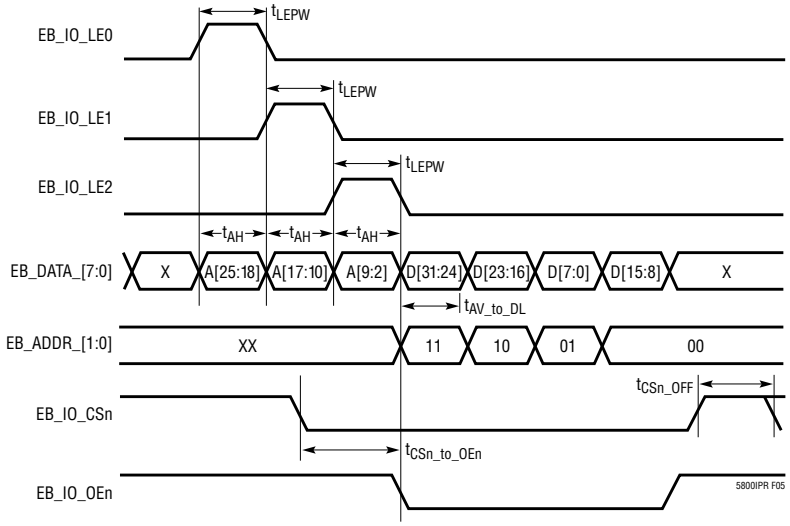


Figure 5. External Bus Read Timing

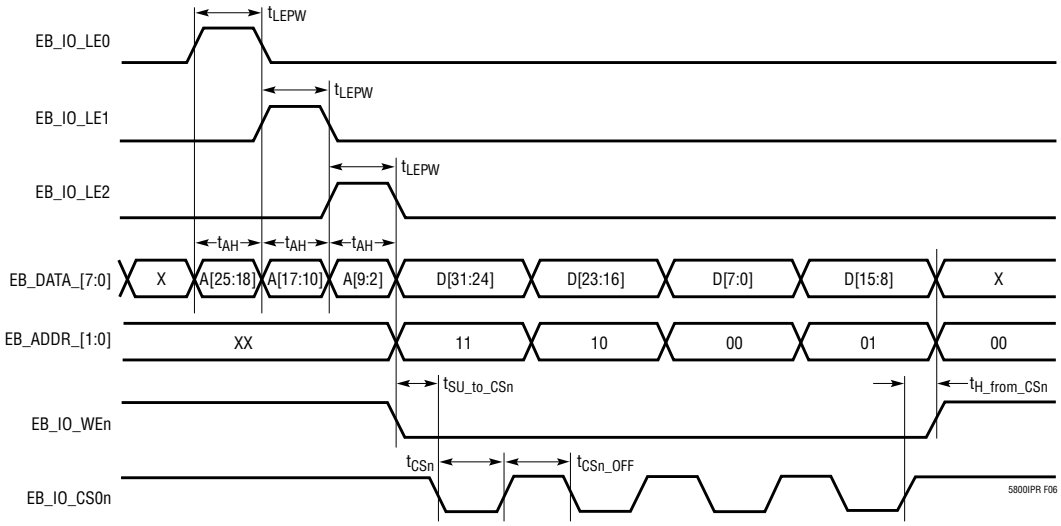


Figure 6. External Bus Write Timing

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to Eterna. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data. See the FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As Specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://www.standards.ieee.org/findstds/standard/802.15.4-2011.html

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than ±40 ppm.

Note 7: Per pin I/O types are provided in the Pin Functions section.

Note 8: VIH maximum voltage input must respect the VSUPPLY maximum voltage specification.

Note 9: See the SmartMesh IP Manager API Guide for the time Indication notification definition.

Note 10: Network time accuracy is a statistical measure and varies over the temperature range, reporting rate and the location of the device relative to the manager in the network. See the Typical Performance Characteristics section for a more detailed description.

Note 11: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 12: Following erase or write transfers, the IPCS SPI slave status register, 0xD7 must be polled to determine the completion time of the erase or write operation prior to negating either FLASH_P_ENn or RESETn.

Note 13: Guaranteed by design, not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

In mesh networks data can propagate from the manager to the nodes, downstream, or from the motes to the manager, upstream, via a sequence of transmissions from one device to the next. As shown in Figure 8, data originating from mote P1 may propagate to the manager directly or through P2. As mote P1 may directly communicate with the manager, mote P1 is referred to as a 1-hop mote. Data originating from mote D1, must propagate through at least one other mote, P2 or P1, and as a result is referred to as a 2-hop mote. The fewest number of hops from a mote to the manager determines the hop depth.

As described in Application Time Synchronization, Eterna provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the manager and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was thus affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between –40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for 8 hours, followed by rapid cycling between –5°C and 45°C for 8 hours, and lastly, rapid cycling between –40°C and 15°C for 8 hours.

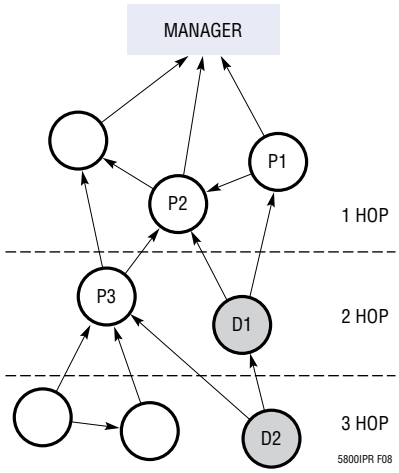
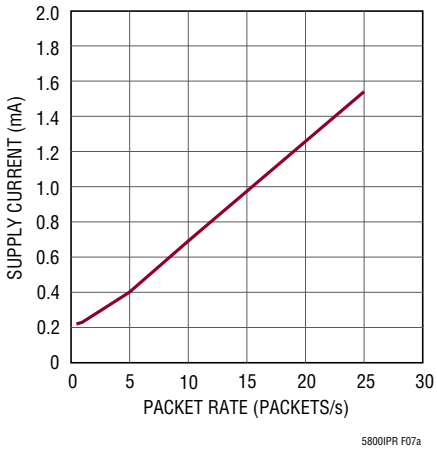


Figure 8. Example Network Graph



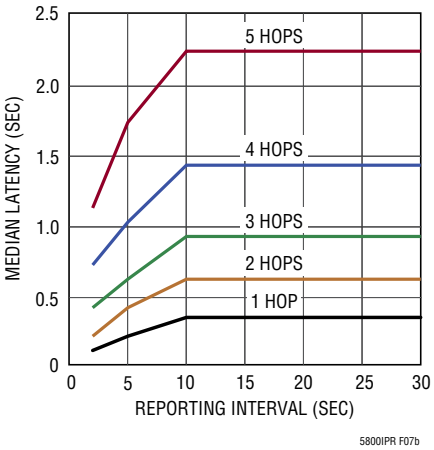
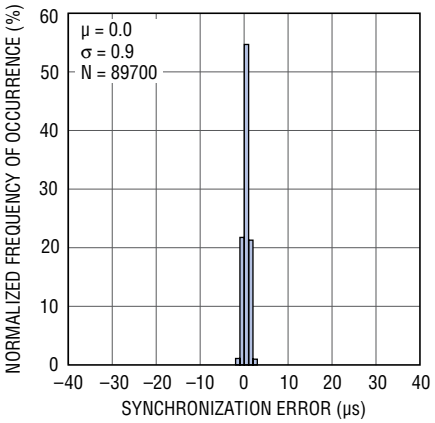


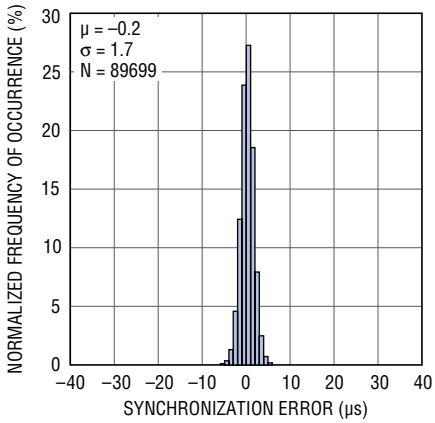
Figure 7

TYPICAL PERFORMANCE CHARACTERISTICS

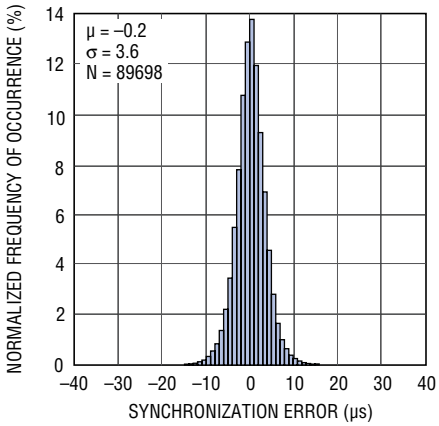
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 1 Hop, Room Temperature



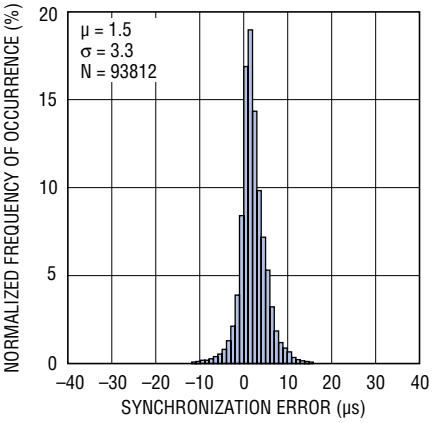
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 3 Hops, Room Temperature



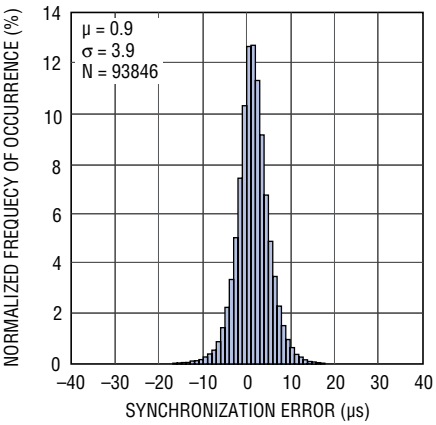
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 5 Hops, Room Temperature



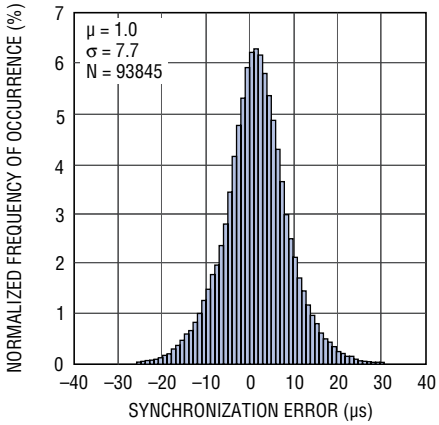
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 1 Hop, 2°C/Min



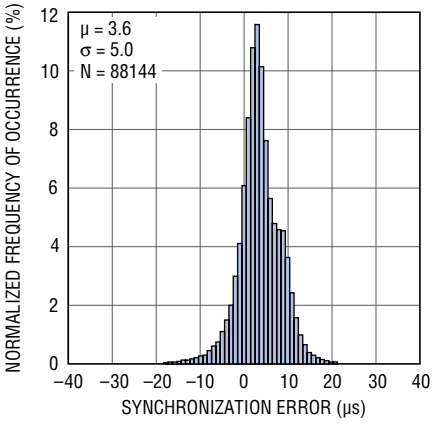
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 3 Hops, 2°C/Min



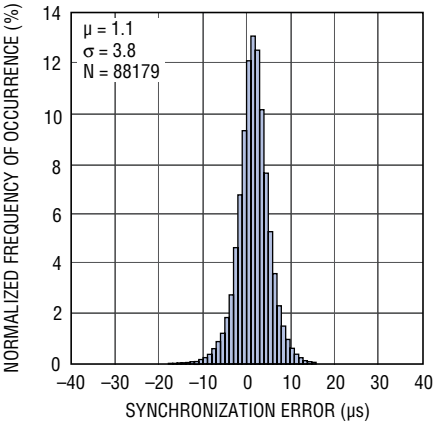
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 5 Hops, 2°C/Min



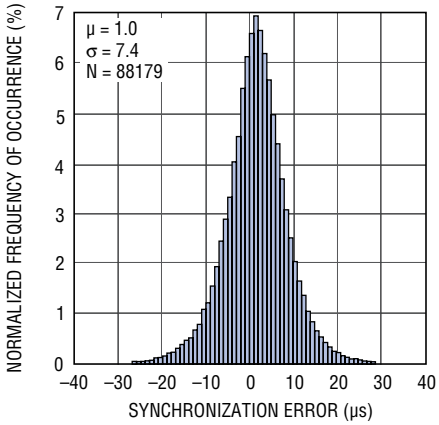
TIMEn Synchronization Error 0 Packets/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 0 Packets/s Publishing Rate, 3 Hops, 8°C/Min

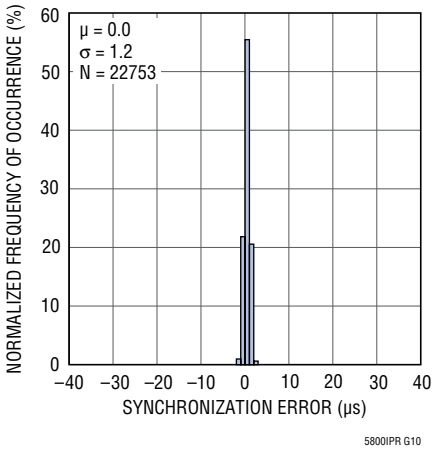


TIMEn Synchronization Error 0 Packets/s Publishing Rate, 5 Hops, 8°C/Min

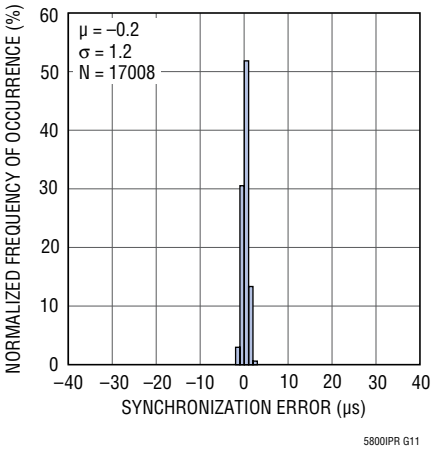


TYPICAL PERFORMANCE CHARACTERISTICS

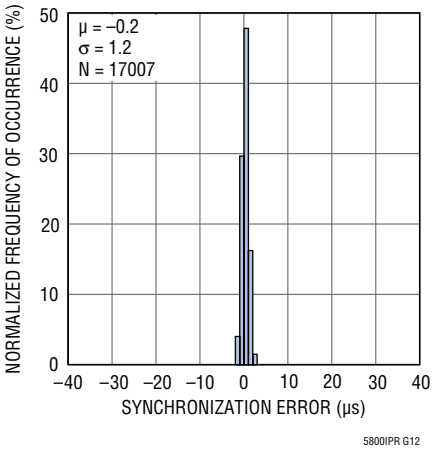
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, Room Temperature



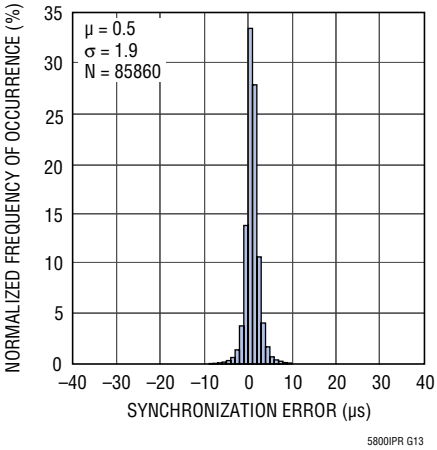
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, Room Temperature



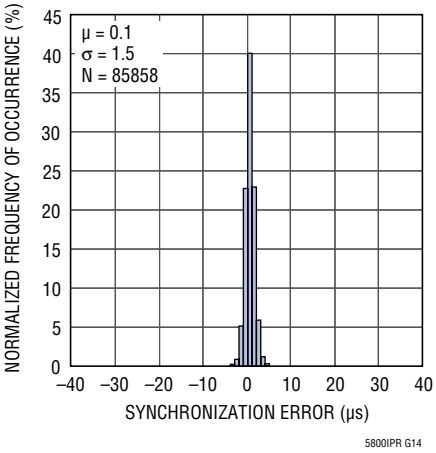
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, Room Temperature



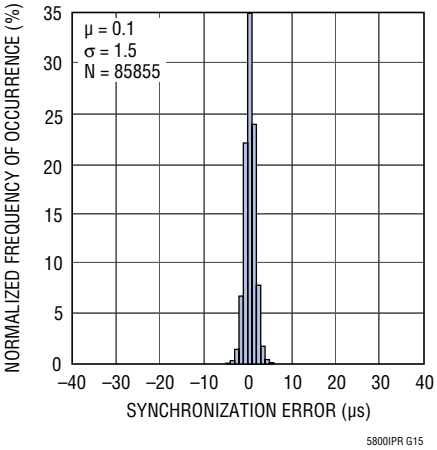
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 2°C/Min



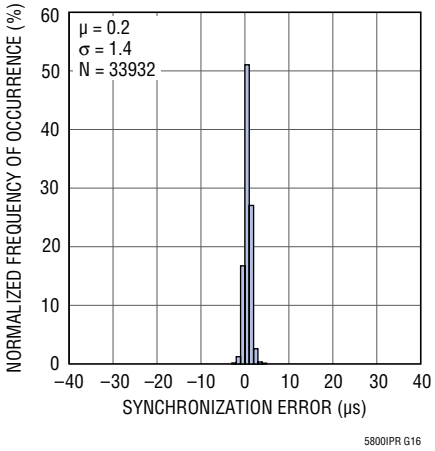
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 2°C/Min



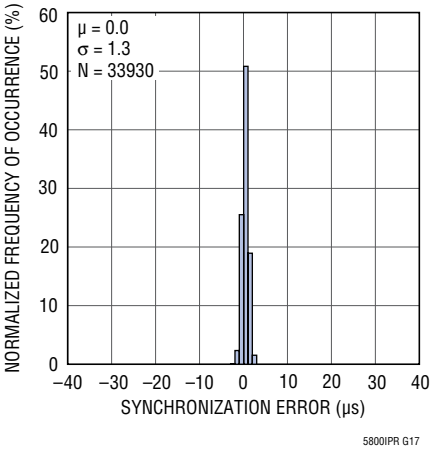
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 2°C/Min



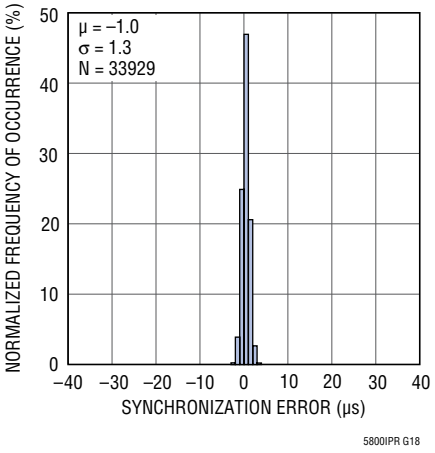
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 8°C/Min



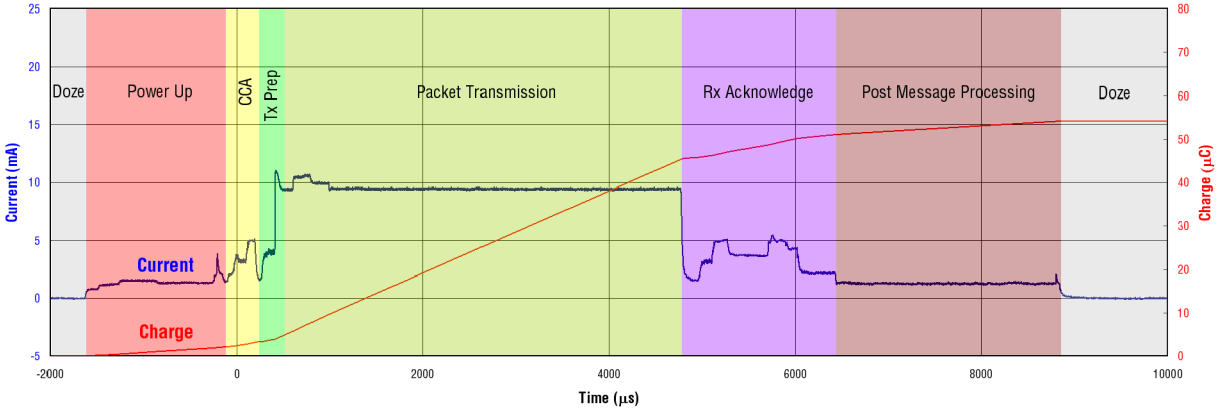
TYPICAL PERFORMANCE CHARACTERISTICS

As described in the SmartMesh Network Overview, devices in network spend the vast majority of their time inactive in their lowest power state (doze). On a synchronous schedule a mote will wake to communicate with another mote. Regularly occurring sequences which wake, perform a significant function and return to sleep are considered atomic. These operations are considered atomic as the sequence of events can not be separated into smaller events while performing a useful function. For example, transmission of a packet over the radio is an atomic operation. Atomic operations may be characterized in either charge or energy. In a time slot where a mote successfully sends a packet, an atomic transmit includes setup prior to sending the message, sending the message, receiving the acknowledgment and the post processing needed as a result of the message being sent. Similarly in a time slot when a mote successfully receives a packet, an atomic receive includes setup prior to listening, listening until the start of the packet transition, receiving the packet, sending the acknowledgement and post processing required due to the arrival of the packet.

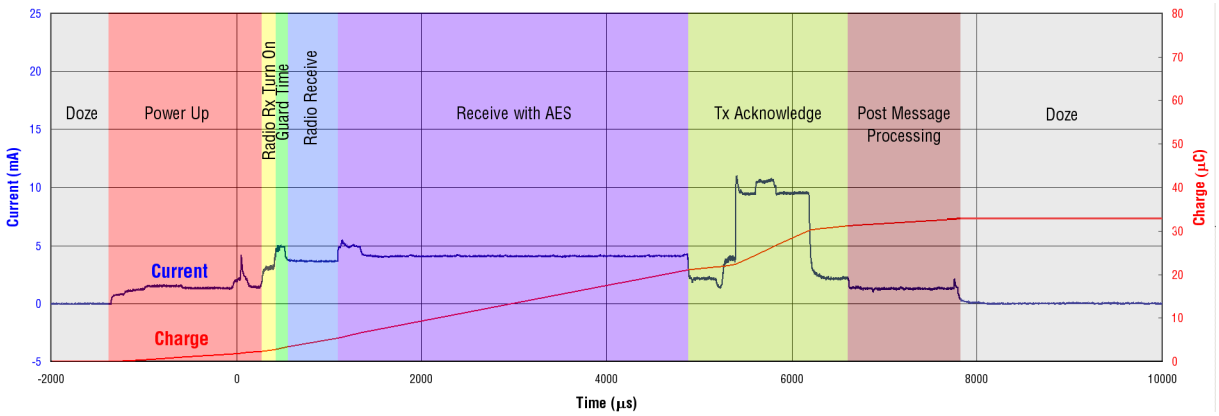
To ensure reliability each mote in the network is provided multiple time slots for each packet it nominally will send and forward. The time slots are assigned to communicate upstream, towards the manager, with at least two different motes. When combined with frequency hopping this provides temporal, spatial and spectral redundancy. Given this approach a mote will often listen for a message that it will never receive since the time slot is not being used by the transmitting mote. It has already successfully transmitted the packet. Since typically 3 time slots are scheduled for every 1 packet to be sent or forwarded, motes will perform more of these atomic “Idle Listens” than atomic transmit or atomic receive sequences. Examples of transmit, receive and idle listen atomic operations are shown in Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS

Atomic Operation—Maximum Length Transmit with Acknowledge, 7.25ms Time Slot (54.5µC Total Charge at 3.6V)



Atomic Operation—Maximum Length Receive with Acknowledge, 7.25ms Time Slot (32.6µC Total Charge at 3.6V)



Atomic Operation—Idle Listen, 7.25ms Time Slot (6.4µC Total Charge at 3.6V)

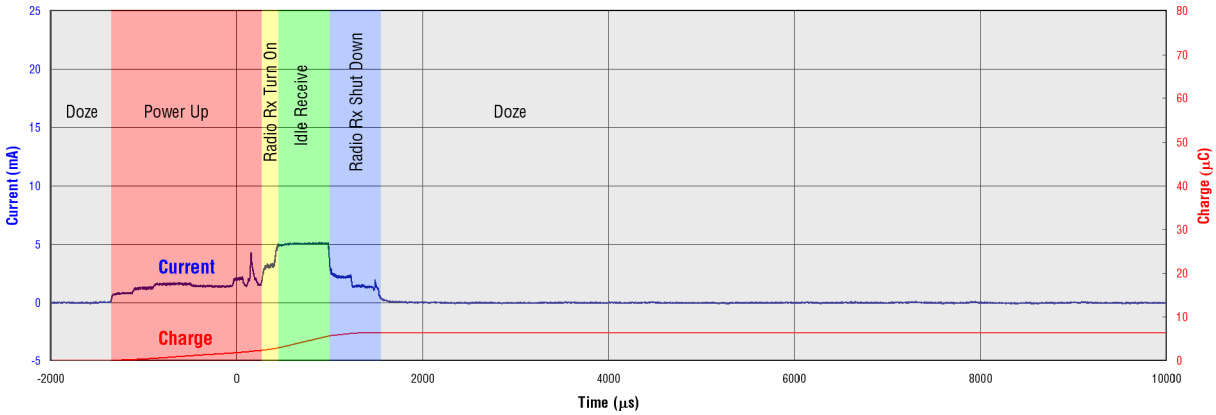


Figure 9

PIN FUNCTIONS

Pin functions in italics are currently not supported in software.

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **NO** column provides the pin number. The second column lists the function. The **TYPE** column lists the I/O type. The **I/O** column lists the direction of the signal relative to Eterna. The **PULL** column shows which signals have a fixed passive pull-up or pull-down. The **DESCRIPTION** column provides a brief signal description.

NO	POWER SUPPLY	TYPE	I/O	PULL	DESCRIPTION
P	GND	Power	–	–	Ground Connection, P = QFN Paddle
2	CAP_PA_1P	Power	–	–	PA DC/DC Converter Capacitor 1 Plus Terminal
3	CAP_PA_1M	Power	–	–	PA DC/DC Converter Capacitor 1 Minus Terminal
4	CAP_PA_2M	Power	–	–	PA DC/DC Converter Capacitor 2 Minus Terminal
5	CAP_PA_2P	Power	–	–	PA DC/DC Converter Capacitor 2 Plus Terminal
6	CAP_PA_3P	Power	–	–	PA DC/DC Converter Capacitor 3 Plus Terminal
7	CAP_PA_3M	Power	–	–	PA DC/DC Converter Capacitor 3 Minus Terminal
8	CAP_PA_4M	Power	–	–	PA DC/DC Converter Capacitor 4 Minus Terminal
9	CAP_PA_4P	Power	–	–	PA DC/DC Converter Capacitor 4 Plus Terminal
10	VDDPA	Power	–	–	Internal Power Amplifier Power Supply, Bypass
30	VDDA	Power	–	–	Regulated Analog Supply, Bypass
31	VCORE	Power	–	–	Regulated Core Supply, Bypass
32	VOSC	Power	–	–	Regulated Oscillator Supply, Bypass
54	VPP	Power	-	-	Internal Regulator Test Port
56	VPRIME	Power	–	–	Internal Primary Power Supply, Bypass
57	CAP_PRIME_4P	Power	–	–	Primary DC/DC Converter Capacitor 4 Plus Terminal
58	CAP_PRIME_4M	Power	–	–	Primary DC/DC Converter Capacitor 4 Minus Terminal
59	CAP_PRIME_3M	Power	–	–	Primary DC/DC Converter Capacitor 3 Minus Terminal
60	CAP_PRIME_3P	Power	–	–	Primary DC/DC Converter Capacitor 3 Plus Terminal
61	CAP_PRIME_2P	Power	–	–	Primary DC/DC Converter Capacitor 2 Plus Terminal
62	CAP_PRIME_2M	Power	–	–	Primary DC/DC Converter Capacitor 2 Minus Terminal
63	CAP_PRIME_1M	Power	–	–	Primary DC/DC Converter Capacitor 1 Minus Terminal
64	CAP_PRIME_1P	Power	–	–	Primary DC/DC Converter Capacitor 1 Plus Terminal
65	VSUPPLY	Power	–	–	Power Supply Input to Eterna

NO	RADIO	TYPE	I/O	PULL	DESCRIPTION
1	*RADIO_INHIBIT*	*1 (Note 14)*	*I*	–	*Radio Inhibit*
11	LNA_EN	1	O	–	External LNA Enable
12	RADIO_TX	1	O	–	Radio TX Active (External PA Enable/Switch Control)
13	RADIO_TXn	1	O	–	Radio TX Active (External PA Enable/Switch Control), Active Low
14	ANTENNA	–	–	–	Single-Ended Antenna Port, 50Ω

PIN FUNCTIONS

Pin functions in italics are currently not supported in software.

NO	CRYSTALS	TYPE	I/O	PULL	DESCRIPTION
19	OSC_32K_XOUT	Crystal	O	–	32kHz Crystal Xout
20	OSC_32K_XIN	Crystal	I	–	32kHz Crystal Xin
28	OSC_20M_XIN	Crystal	I	–	20MHz Crystal Xin
29	OSC_20M_XOUT	Crystal	O	–	20MHz Crystal Xout

NO	RESET	TYPE	I/O	PULL	DESCRIPTION
22	RESETn	1	O	UP	Reset Input, Active Low

NO	JTAG	TYPE	I/O	PULL	DESCRIPTION
23	TDI	1	I	UP	JTAG Test Data In
24	TDO	1	O	–	JTAG Test Data Out
25	TMS	1	I	UP	JTAG Test Mode Select
26	TCK	1	I	DOWN	JTAG Test Clock

NO	SPECIAL PURPOSE	TYPE	I/O	PULL	DESCRIPTION
72	TIMEn	1 (Note 14)	I	–	Time Capture Request, Active Low

NO	CLI and EXTERNAL MEMORY	TYPE	I/O	PULL	DESCRIPTION
33	EB_DATA_7	1	I/O	–	External Bus Data Bit 7
34	EB_DATA_6	1	I/O	–	External Bus Data Bit 6
35	EB_DATA_4	1	I/O	–	External Bus Data Bit 4
36	EB_DATA_0	1	I/O	–	External Bus Data Bit 0
37	UARTC0_TX EB_IO_LE0	2	O O	–	CLI UART 0 Transmit External Bus I/O Latch Enable 0 for External Address Bits A[25:18]
38	UARTC0_RX EB_DATA_1	1	I I/O	–	CLI UART 0 Receive External Bus Data Bit 1
39	EB_IO_LE2	1	O	–	External Bus I/O Latch Enable 2 for External Address Bits A[9:2]
41	EB_ADDR_1	2	O	–	External Bus Address Bit 1
43	EB_ADDR_0	2	O	–	External Bus Address Bit 0
46	EB_DATA_3	1	I/O	–	External Bus Data Bit 3
47	EB_DATA_2	1	I/O	–	External Bus Data Bit 2
48	EB_DATA_5	1	I/O	–	External Bus Data Bit 5
49	EB_IO_CS0n	2	O	–	External Bus Chip Select 0
50	UARTC1_TX	2	O	–	CLI UART 1 Transmit
51	UARTC1_RX	1	I	–	CLI UART 1 Receive
52	EB_IO_WEn	2	O	–	External Bus Write Enable Strobe
53	EB_IO_OEn	2	O	–	External Bus Output Enable Strobe

PIN FUNCTIONS

Pin functions in italics are currently not supported in software.

NO	IPCS SPI/FLASH PROGRAMMING (NOTE 15)	TYPE	I/O	PULL	DESCRIPTION
40	IPCS_MISO	2	O	–	SPI Flash Emulation (MISO) Master In Slave Out Port
42	IPCS_MOSI	1	I	–	SPI Flash Emulation (MOSI) Master Out Slave In Port
44	IPCS_SCK	1	I	–	SPI Flash Emulation (SCK) Serial Clock Port
45	IPCS_SSn	1	I	–	SPI Flash Emulation Slave Select, Active Low
55	FLASH_P_ENn EB_IO_LE1	1	I O	UP UP	Flash Program Enable, Active Low External Bus I/O Latch Enable 1 for External Address Bits A[17:10]

NO	API UART	TYPE	I/O	PULL	DESCRIPTION
66	UART_RX_RTSn	1 (Note 14)	I	–	UART Receive (RTS) Request to Send, Active Low
67	UART_RX_CTSn	1	O	–	UART Receive (CTS) Clear to Send, Active Low
68	UART_RX	1 (Note 14)	I	–	UART Receive
69	UART_TX_RTSn	1	O	–	UART Transmit (RTS) Request to Send, Active Low
70	UART_TX_CTSn	1 (Note 14)	I	–	UART Transmit (CTS) Clear to Send, Active Low
71	UART_TX	2	O	–	UART Transmit

Note 14: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage.

Note 15: Embedded programming over the IPCS SPI bus is only avaliable when RESETn is asserted.

VSUPPLY: System and I/O Power Supply. Provides power to the chip including the on-chip DC/DC converters. The digital-interface I/O voltages are also set by this voltage. Bypass with 2.2µF and 0.1µF to ensure the DC/DC converters operate properly.

VDDPA: PA-Converter Bypass Pin. A 0.47µF capacitor should be connected from VDDPA to ground with as short a trace as feasible. Do not connect anything else to this pin.

VDDA: Analog-Regulator Bypass Pin. A 0.1µF capacitor should be connected from VDDA to ground with as short a trace as feasible. Do not connect anything else to this pin.

VCORE: Core-Regulator Bypass Pin. A 56nF capacitor should be connected from VCORE to ground with as short a trace as feasible. Do not connect anything else to this pin.

VOSC: Oscillator-Regulator Bypass Pin. A 56nF capacitor should be connected from VOSC to ground with as short a trace as feasible. Do not connect anything else to this pin.

VPP: Manufacturing Test port for internal regulator. Do not connect anything to this pin.

VPRIME: Primary-Converter Bypass Pin. A 0.22µF capacitor should be connected from VPRIME to ground with as short a trace as feasible. Do not connect anything else to this pin.

VBGAP: Bandgap reference output. Used for testing and calibration. Do not connect anything to this pin.

CAP_PA_1P, CAP_PA_1M Through CAP_PA_4P, CAP_PA_4M: Dedicated Power Amplifier DC/DC Converter Capacitor Pins. These pins are used when the radio is transmitting to efficiently convert VSUPPLY to the proper voltage for the power amplifier. A 56nF capacitor should be connected between each P and M pair. Trace length should be as short as feasible.

CAP_PRIME_1P, CAP_PRIME_1M Through CAP_PRIME_4P, CAP_PRIME_4M: Primary DC/DC Converter Capacitor Pins. These pins are used when the device is awake to efficiently convert VSUPPLY to the proper voltage for the three on-chip low dropout regulators. A 56nF capacitor should be connected between each P and M pair. Trace length should be as short as feasible.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the antenna pin should be 50Ω, single-ended with respect to paddle ground. To ensure regulatory compliance of the final product please see the Eterna Integration Guide for filtering requirements. The antenna pin should not have a DC path to ground; AC blocking must be included if a DC-grounded antenna is used.

PIN FUNCTIONS

OSC_32K_XOUT: Output Pin for the 32kHz Oscillator. Connect to 32kHz quartz crystal. The OSC_32K_XOUT and OSC_32K_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 10.

OSC_32K_XIN: Input for the 32kHz Oscillator. Connect to 32kHz quartz crystal. The OSC_32K_XOUT and OSC_32K_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 10.

OSC_20M_XOUT: Output for the 20MHz Oscillator. Connect only to a supported 20MHz quartz crystal. The OSC_20M_XOUT and OSC_20M_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 10. See the Eterna Integration Guide for supported crystals.

OSC_20M_XIN: Input for the 20MHz Oscillator. Connect only to a supported 20MHz quartz crystal. The OSC_20M_XOUT and OSC_20M_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 10.

RESETn: The asynchronous reset signal is internally pulled up. Resetting Eterna will result in the ARM Cortex M3 rebooting and loss of network connectivity. Use of this signal for resetting Eterna is not recommended, except during power-on and in-circuit programming.

RADIO_INHIBIT: The radio inhibit function is currently not supported by software. RADIO_INHIBIT provides a mechanism for an external device to temporarily disable radio operation. Failure to observe the timing requirements defined in the RADIO_INHIBIT AC Characteristics table may result in unreliable network operation. In designs where the RADIO_INHIBIT function is not needed the input must either be tied, pulled or actively driven low to avoid excess leakage.

LNA_ENABLE, RADIO_TX, RADIO_TXn: Control signals generated by the autonomous MAC supporting the integration of an external LNA/PA. See the Eterna Extended Range Reference Design for implementation details.

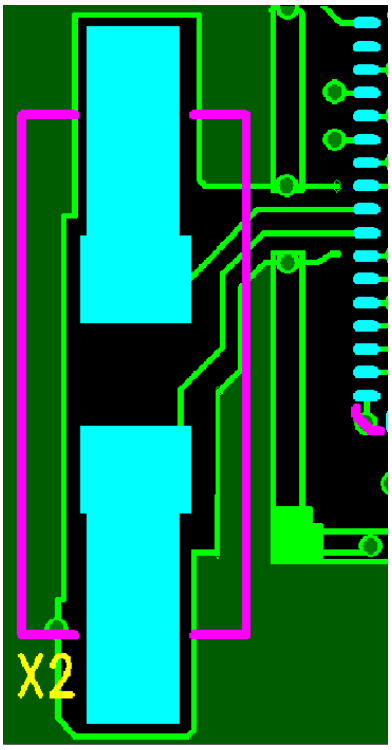


Figure 10. PCB Top Metal Layer Shielding of Crystal Signals

TMS, TCK, TDI, TDO: JTAG Port Supporting Software Debug and Boundary Scan. An IEEE Std 1149.1b-1994 compliant boundary scan definition language (BDSL) file for the WR QFN72 package can be found here.

SLEEPn: The SLEEPn function is not currently supported in software. The SLEEPn input must either be tied, pulled or actively driven high to avoid excess leakage.

UART_RX, UART_RX_RTSn, UART_RX_CTSn, UART_TX, UART_TX_RTSn, UART_TX_CTSn: The API UART interface includes bidirectional wake-up and flow control. Unused input signals must be driven or pulled to their inactive state.

TIMEn: Strobing the TIMEn input is the most accurate method to acquire the network time maintained by Eterna. Eterna latches the network timestamp with sub-microsecond resolution on the rising edge of the TIMEn signal and produces a packet on the API serial port containing the timing information.

PIN FUNCTIONS

UARTC0_RX, UARTC0_TX, UARTC1_RX, UARTC1_TX: The CLI UART provides a mechanism for monitoring, configuration and control of Eterna during operation. On the LTC5800-IPR CLI UART 0 is used when Eterna is not configured to support external RAM and CLI UART 1 is used when Eterna is configured to support external RAM. For a complete description of the supported commands see the SmartMesh IP Manager CLI Guide.

EB_DATA_0 through EB_DATA_7, EB_ADDR_0, EB_ADDR_1, EB_IO_LE1 through EB_IO_LE2, EB_IO_CS0n, EB_IO_WEn, EB_IO_ENn: The external bus provides a multiplexed address data bus enabling the Cortex-M3 direct access of external byte wide RAM. The additional RAM is used by network management software enabling the support of a larger network of motes with higher packet throughput. To support the addressing needed, each latch signal, EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2 will strobe to latch 8-bits of address from the EB_DATA[7:0] bus. EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2 correspond to address bits [25:18], [17:10] and [9:2] respectively. EB_ADDR_0 and EB_ADDR_1 correspond to the lower two bits of address. For systems with 256kB or less EB_IO_LE2 can be ignored. EB_IO_CS0n, EB_IO_WEn and EB_IO_OEn provide chip select, write enable and output enable control of the external RAM.

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The in-circuit programming control system (IPCS) bus enables in-circuit programming of Eterna's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

OPERATION

The LTC5800 is the world's most energy-efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex-M3, best-in-class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 11, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low-power states. Items in the gray shaded region labeled Analog Core correspond to the analog/RF components.

POWER SUPPLY

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low power state. The integrated power supply conditioning architecture, including the two integrated DC/DC converters and three integrated low dropout regulators, provides excellent rejection of supply noise. Eterna's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride (Li-$SOCl_2$) sources and wide enough to support battery operation over a broad temperature range.

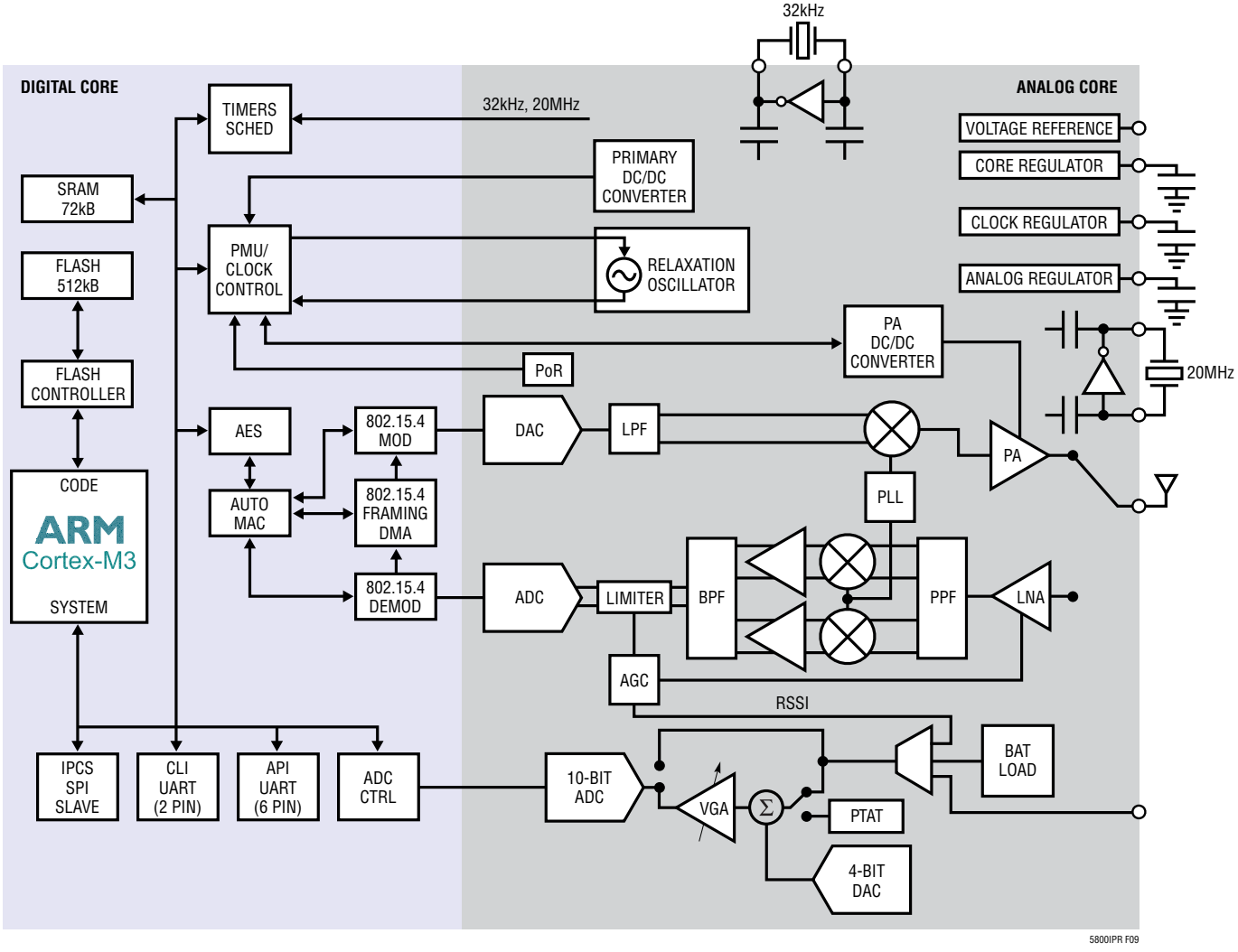


Figure 11. Eterna Block Diagram

OPERATION

SUPPLY MONITORING AND RESET

Eterna integrates a power-on-reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. For a graceful shutdown, the software and the networking layers should be cleanly halted via API commands prior to assertion of the RESETn pin. See the SmartMesh IP Manager API Guide for details on the disconnect and reset commands. Eterna includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. The integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust nonvolatile storage solution.

PRECISION TIMING

Eterna's unique low power dedicated timing hardware and timing algorithms provide a significant improvement over competing 802.15.4 product offerings. This functionality provides timing precision two to three orders of magnitude better than any other low power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

APPLICATION TIME SYNCHRONIZATION

In addition to coordinating time slots across the network, which is transparent to the user, Eterna's timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. Eterna will send a time packet through its serial interface when one of the following occurs:

- Eterna receives an API request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the time stamp is captured in hardware relative to the rising edge of TIMEn. If an API request is used, due to packet processing, the value of the time stamp may be captured several milliseconds after receipt of the packet. See the TIMEn AC Characteristics table for the TIMEn function's definition and specifications.

TIME REFERENCES

Eterna includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

OPERATION

Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 7.3728MHz. The internal relaxation oscillator typically starts up in a few µs, providing an expedient, low energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in the State Diagram section, allows Eterna to wake up and receive data over the UART and SPI interfaces by simply detecting activity on the appropriate signals.

32.768kHz Crystal Oscillator

Once Eterna is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational while in the Active state, and is used as the timing basis when in Doze state. See the State Diagram section, for a description of Eterna's operational states.

20MHz Crystal Oscillator

The 20 MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed. Eterna requires specific characterized 20MHz crystal references. See the Eterna Integration Guide for a complete list of the currently supported 20MHz crystals.

RADIO

Eterna includes the lowest power commercially available 2.4GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to Radio Specifications section for power consumption numbers.) Eterna's integrated power amplifier is calibrated and temperature compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, Eterna uniquely includes a hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and advanced encryption standard (AES) peripherals. The hardware-based autonomous media access controller (MAC) minimizes CPU activity, thereby further decreasing power consumption.

UARTS

The principal network interface is through the application programming interface (API) UART. A command-line interface (CLI) UART is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred over the port and then automatically returning to their lowest power state after the conclusion of a transfer. The definition for packet encoding on the API UART interface can be found in the SmartMesh IP Manager API Guide and the CLI command definitions can be found in the SmartMesh IP Manager CLI Guide.

OPERATION

API UART Protocols

The API UART supports multiple modes with the goal of supporting a wide range of companion multipoint control units (MCUs) while reducing power consumption of the system. As a general rule, higher serial data rates translate into lower energy consumption for both endpoints. The API UART receive protocol includes two additional signals in addition to UART_RX: UART_RX_RTSn and UART_RX_CTSn. The transmit half of the API UART protocol includes two additional signals in addition to UART_TX: UART_TX_RTSn and UART_TX_CTSn. The two supported protocols are referred to as UART Mode 2 and UART Mode 4. Mode setting is controlled via the Fuse Table.

In the Figures accompanying the protocol descriptions, signals driven by the companion processor are drawn in black and signals driven by Eterna are drawn in blue.

UART Mode 2

UART Mode 2 provides the most energy-efficient method for operating Eterna's API UART. UART Mode 2 requires the use of all six UART signals, but does not require adherence to the minimum inter-packet delay as defined in section UART AC Characteristics. UART Mode 2 incorporates edge-sensitive flow control, at either 9600 or 115200 baud. Packets are HDLC encoded with one stop bit and no parity bit. The flow control signals for Eterna's API receive path are shown in Figure 12, UART Mode 2 Receive Flow Control. Transfers are initiated by the companion processor asserting UART_RX_RTSn. Eterna then responds by enabling the UART and asserting UART_RX_CTSn. After detecting the assertion of UART_RX_CTSn the companion processor sends the entire packet. Following the transmission of the final byte in the packet, the companion processor negates UART_RX_RTSn and waits until the negation of UART_RX_CTSn before asserting UART_RX_RTSn again.

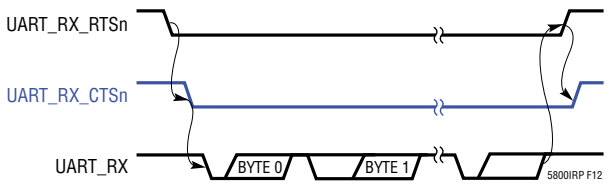


Figure 12. UART Mode 2 Receive Flow Control

The flow control signals for Eterna's API transmit path are shown in Figure 13, UART Mode 2 Transmit Flow Control. Transfers are initiated by Eterna asserting UART_TX_RTSn. The companion processor responds by asserting UART_TX_CTSn when ready to receive data. After detecting the falling edge of UART_TX_CTSn Eterna sends the entire packet. Following the transmission of the final byte in the packet Eterna negates UART_TX_RTSn and waits until the negation of UART_TX_CTSn before asserting UART_TX_RTSn again. The companion processor may negate UART_TX_CTSn any time after the first byte is transferred provided the timeout from UART_TX_RTSn to UART_TX_CTSn, $t_{END\_TX\_RTS\ to\ TX\_CTS}$, is met.

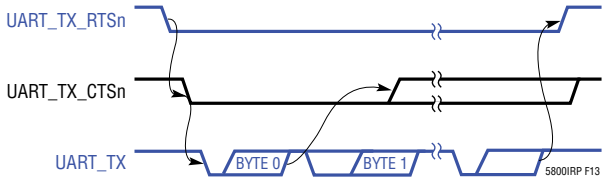


Figure 13. UART Mode 2 Transmit Flow Control

UART Mode 4

UART Mode 4 incorporates level-sensitive flow control on the TX channel and requires no flow control on the RX channel, supporting 115200 baud. The use of level-sensitive flow control signals enables the option of using a reduced set of the flow control signals; however, Mode 4 has specific limitations. First, The use of the RX flow control signals (UART_RX_RTSn and UART_RX_CTSn) for Mode 4 are optional provided the use is limited to the industrial temperature range (–40°C to 85°C); otherwise, the flow control is mandatory. If RX flow control signals are not used, UART_RX_RTSn should be tied to VSUPPLY (inactive) and UART_RX_CTSn should be left unconnected.

OPERATION

Second, unless the companion processor is always ready to receive a packet, the companion processor must negate UART_TX_CTSn prior to the end of the current packet. Failure to negate UART_TX_CTSn prior to the end of a packet may result in back to back packets. Third, the companion processor must wait at least $t_{RX\_INTERPACKET}$ between transmitting packets on UART_RX. See the UART AC Characteristics section for complete timing specifications. Packets are HDLC encoded with one stop bit and no parity bit. The flow control signals for the TX channel are shown in Figure 17. Transfers are initiated by Eterna asserting UART_TX_RTSn. The UART_TX_CTSn signal may be actively driven by the companion processor when ready to receive a packet or UART_TX_CTSn may be tied low if the companion processor is always ready to receive a packet. After detecting a logic '0' on UART_TX_CTSn, Eterna sends the entire packet. Following the transmission of the final byte in the packet, Eterna negates UART_TX_RTSn and waits for $t_{TX\_INTERPACKET}$, defined in the UART AC Characteristics section before asserting UART_TX_RTSn again.

For details on the timing of the UART protocol, see section UART AC Characteristics.

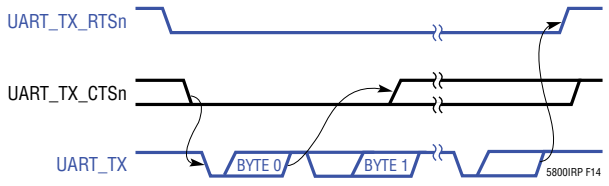


Figure 14. UART Mode 4 Transmit Flow Control

CLI UART

The command line interface (CLI) UART port is a 2-wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one stop bit and no parity. The CLI UART interface is intended to support command line instructions and response activity. The pins used for the CLI UART change when the Eterna is configured to use external SRAM. The CLI UART is assigned to UARTC0 when external SRAM is not used and assigned to UARTC1 when external SRAM is used.

AUTONOMOUS MAC

Eterna was designed as a system solution to provide a reliable, ultralow power, and secure network. A reliable network capable of dynamically optimizing operation over changing environments requires solutions that are far too complex to completely support through hardware acceleration alone. As described in the Precision Timing section, proper time management is essential for optimizing a solution that is both low power and reliable. To address these requirements Eterna includes the autonomous MAC, which incorporates a coprocessor for controlling all of the time-critical radio operations. The autonomous MAC provides two benefits: first, preventing variable software latency from affecting network timing and second, greatly reducing system power consumption by allowing the CPU to remain inactive during the majority of the radio activity. The autonomous MAC provides software-independent timing control of the radio and radio-related functions, resulting in superior reliability and exceptionally low power.

SECURITY

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. Eterna system solutions provide a FIPS-140 compliant encryption scheme that includes authentication and encryption at the MAC and network layers with separate keys for each mote. This not only yields end-to-end security, but if a mote is somehow compromised, communication from other motes is still secure. A mechanism for secure key exchange allows keys to be kept fresh. To prevent physical attacks, Eterna includes hardware support for electronically locking devices, thereby preventing access to Eterna's flash and RAM memory and thus the keys and code stored therein. This lock-out feature also provides a means to securely unlock a device should support of a product require access. For details see the Board Specific Configuration Guide.

OPERATION

TEMPERATURE SENSOR

Eterna includes a calibrated temperature sensor on chip. The temperature readings are available locally through Eterna's serial API, in addition to being available via the network manager. The performance characteristics of the temperature sensor can be found in the Temperature Sensor Characteristics table.

RADIO INHIBIT

The RADIO_INHIBIT input enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When RADIO_INHIBIT is asserted the software radio drivers will disallow radio operations including clear channel assessment, packet transmits, or packet receipts. If the current time slot is active when RADIO_INHIBIT is asserted the radio will be disabled after the present operation completes. For details on the timing associated with RADIO_INHIBIT, see the RADIO_INHIBIT AC Characteristics table.

FLASH PROGRAMMING

This product is provided without software programmed into the device. OEMs will need to program software images during development and manufacturing. Eterna's software images are loaded via the in-circuit programming control system (IPCS) SPI interface. Sequencing of RESETn and FLASH_P_ENn, as described in the Flash SPI Slave A/C Characteristics table, places Eterna in a state emulating a serial flash to support in-circuit programming. Hardware and software for supporting development and production programming of devices is described in the Eterna Serial Programmer Guide. The serial protocol, SPI, and timing parameters are described in the Flash SPI Slave A/C Characteristics table.

FLASH DATA RETENTION

Eterna contains internal flash (non-volatile memory) to store calibration results, unique ID, configuration settings and software images. Flash retention is specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive storage above the operating temperature range of –55°C to 105°C is possible; however, this may result in a degradation of retention characteristics.

The degradation in flash retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 0.6eV

$k = 8.625 \bullet 10^{-5}$eV/°K

T_{USE} = is the specified temperature retention in °C

T_{STRESS} = actual storage temperature in °C

Example: Calculate the effect on retention when storing at a temperature of 125°C.

T_{STRESS} = 125°C

T_{USE} = 85°C

AF = 7.1

So the overall retention of the flash would be degraded by a factor of 7.1, reducing data retention from 20 years at 85°C to 2.8 years at 125°C.

OPERATION

NETWORKING

The LTC5800-IPR network manager provides the ingress/egress point at the wired to wireless mesh network boundary via the API UART interface. The complexity of the mesh network management is handled entirely within the embedded software, which also provides dynamic network optimization, deterministic power management, intelligent routing, and configurable bandwidth allocation while achieving carrier class data reliability and low power operation.

Dynamic Network Optimization

Dynamic network optimization allows Eterna to address the changing RF requirements in harsh environments resulting in a network that is continuously self-monitoring and self-adjusting. The manager performs dynamic network optimization based upon periodic reports on network health and link quality that it receives from the network motes. The manager uses this information to provide performance statistics to the application layer and proactively solve connectivity problems in the network. Dynamic network optimization not only maintains network health, but also allows Eterna to deliver deterministic power management. One of the key advantages of SmartMesh networking solutions is the network manager is aware of and tracking the success or failure of every packet transaction, so not only can the network be optimized, but the solution can be rigorously tested to produce a system solution with better than 99.999% reliability.

Deterministic Power Management

Deterministic power management balances traffic in the network by diverting traffic around heavily loaded motes (for example, motes with high reporting rates). In doing so, it reduces power consumption for these motes and balances power consumption across the network. Deterministic power management provides predictable maintenance schedules to prevent down time and lower the cost of network ownership. When combined with field devices using Eterna's industry-leading low power radio technology, deterministic power management enables over a decade of battery life for network motes.

Intelligent Routing

Intelligent routing provides each packet with an optimal path through the network. The shortest distance between two points is a straight line, but in RF the quickest path is not always the one with the fewest hops. Intelligent routing finds optimal paths by considering the link quality (one path may lose more packets than another) and the retry schedule, in addition to the number of hops. The result is reduced network power consumption, elimination of in-network collisions, and unmatched network scalability and reliability.

Configurable Bandwidth Allocation

SmartMesh networks provide configurations that enable users to make bandwidth and latency versus power tradeoffs both network wide and on a per device basis. This flexibility enables solutions that tailored to the application requirements, such as request/response, fast file transfer, and alerting. Relevant configuration parameters are described in the SmartMesh IP User's Guide. The Design trade-offs between network performance and current consumption are supported via the SmartMesh Power and Performance Estimator.

IP Manager Options

The IP Manager can operate with or without external SRAM, as described in the Eterna Integration Guide. When used without external SRAM, the IP manager is limited to managing networks of 32 motes or fewer and is limited to a maximum packet throughput of 24 packets per second. With external SRAM, the IP Manager supports managing networks of up to 100 motes and the packet throughput of the IP Manager increases from 24 packets per second without SRAM to 36 packets per second with SRAM.

OPERATION

STATE DIAGRAM

In order to provide capabilities and flexibility in addition to ultra low power, Eterna operates in various states, as shown in Figure 15, and described in this section. State transitions shown in red are not recommended.

Fuse Table

Eterna's Fuse Table is a 2kB page in flash that contains two data structures. One structure supports hardware configuration immediately following power-on reset or the assertion of RESETn. The second structure supports configuration of software board support parameters. Fuse Tables are generated via the Fuse Table application described in the Board Specific Configuration Guide. Hardware configuration of I/O immediately following power-on reset provides a method to minimize leakage due to floating nets prior to software configuration. I/O leakage can contribute hundreds of microamperes of leakage per input, potentially stressing current limited supplies. Examples of software board support parameters include setting of UART modes, clock sources and trim values. Fuse Tables are loaded into flash using the same software and in-circuit programmer used to load software images as described in the Eterna Serial Programmer Guide.

Start-Up

Start-up occurs as a result of either crossing the power-on reset threshold or asserting RESETn. After the completion of power-on reset or the falling edge of an internally synchronized RESETn, Eterna loads its Fuse Table which, as described in the previous section, includes configuring I/O direction. In this state, Eterna checks the state of the FLASH_P_ENn and RESETn pins and enters the serial flash emulation mode if both signals are asserted. If the FLASH_P_ENn pin is not asserted but RESETn is asserted, Eterna automatically reduces its energy consumption to a minimum until RESETn is released. Once RESETn is de-asserted, Eterna goes through a boot sequence, and then enters the Active state.

Serial Flash Emulation

When both RESETn and FLASH_P_ENn are asserted, Eterna disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed.

Operation

Once Eterna has completed start-up Eterna transitions to the Operational group of states (active/CPU active, active/CPU inactive, and Doze). There, Eterna cycles between the various states, automatically selecting the lowest possible power state while fulfilling the demands of network operation.

Active State

In the Active State, Eterna's relaxation oscillator is running and peripherals are enabled as needed. The ARM Cortex-M3 cycles between CPU-active and CPU-inactive (referred to in the ARM Cortex-M3 literature as "Sleep Now" mode). Eterna's extensive use of DMA and intelligent peripherals that independently move Eterna between Active state and Doze state minimizes the time the CPU is active, significantly reducing Eterna's energy consumption.

Doze State

The Doze state consumes orders of magnitude less current than the Active state and is entered when all of the peripherals and the CPU are inactive. In the Doze state Eterna's full state is retained, timing is maintained, and Eterna is configured to detect, wake, and rapidly respond to activity on I/Os (such as UART signals and the TIMEn pin). In the Doze state the 32.768kHz oscillator and associated timers are active.

OPERATION

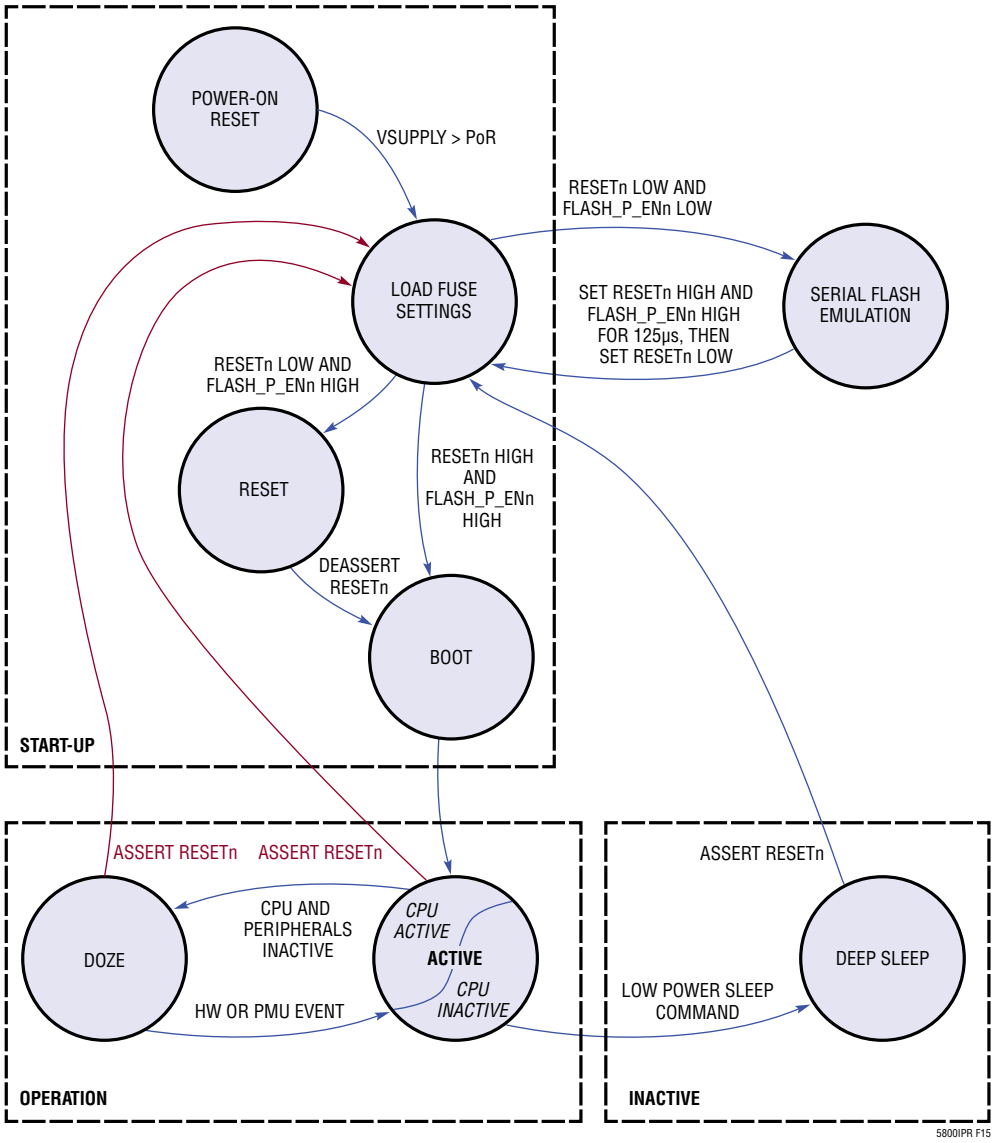


Figure 15. Eterna State Diagram

APPLICATIONS INFORMATION

REGULATORY AND STANDARDS COMPLIANCE

Radio Certification

Eterna is suitable for systems targeting compliance with worldwide radio frequency regulations: ETSI EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan). Application Programming Interfaces (APIs) supporting regulatory testing are provided on both the API and CLI UART interfaces. The Eterna Certification User Guide provides:

- Reference information required for certification
- Test plans for common regulatory test cases
- Example CLI API calls
- Sample manual language and example label

Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr^{+6}), mercury (Hg), Polybrominated Biphenyl (PBB), and Polybrominated Diphenyl Ethers (PBDE). Linear Technology is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2002/95/EC.

The RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Lead-free QFN package
- Halogen-free mold compound
- RoHS-compliant and 245 °C re-flow compatible

Note: Customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2002/95/EC. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

SOLDERING INFORMATION

Eterna is suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260 °C. A more detailed description of layout recommendations, assembly procedures and design considerations is included in the Eterna Integration Guide.

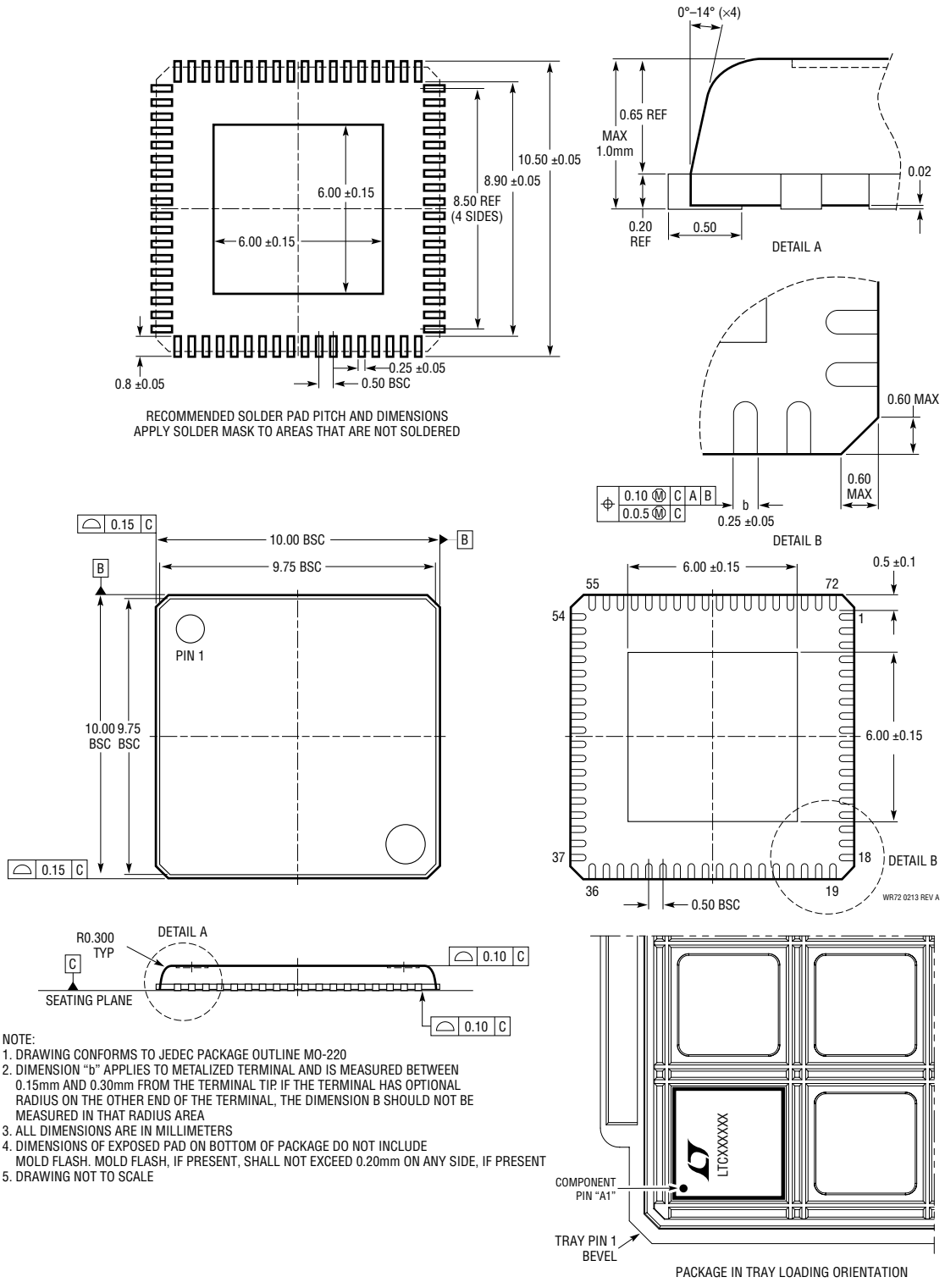
RELATED DOCUMENTATION

TITLE	LOCATION	DESCRIPTION
SmartMesh IP User's Guide	http://www.linear.com/docs/41880	Theory of operation for SmartMesh IP networks and motes
SmartMesh IP Manager API Guide	http://www.linear.com/docs/41883	Definitions of the applications interface commands available over the API UART
SmartMesh IP Manager CLI Guide	http://www.linear.com/docs/41882	Definitions of the command line interface commands available over the CLI UART
Eterna Integration Guide	http://www.linear.com/docs/41874	Recommended practices for designing with the LTC5800
Eterna Serial Programmer Guide	http://www.linear.com/docs/41876	User's guide for the Eterna serial programmer used for in circuit programming of the LTC5800
Board Specific Configuration Guide	http://www.linear.com/docs/41875	User's guide for the Eterna Board Specific Configuration application, used to configure the board specific parameters
Eterna Certification User Guide	http://www.linear.com/docs/42918	The essential documentation necessary to complete radio certifications, including examples for common test cases
SmartMesh IP Tools Guide	http://www.linear.com/docs/42453	The user's guide for all IP related tools, and specifically the definition for the on-chip application protocol (OAP)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC5800#packaging for the most recent package drawings.

WR Package
72-Lead QFN (10mm × 10mm)
(Reference LTC DWG # 05-08-1930 Rev A)



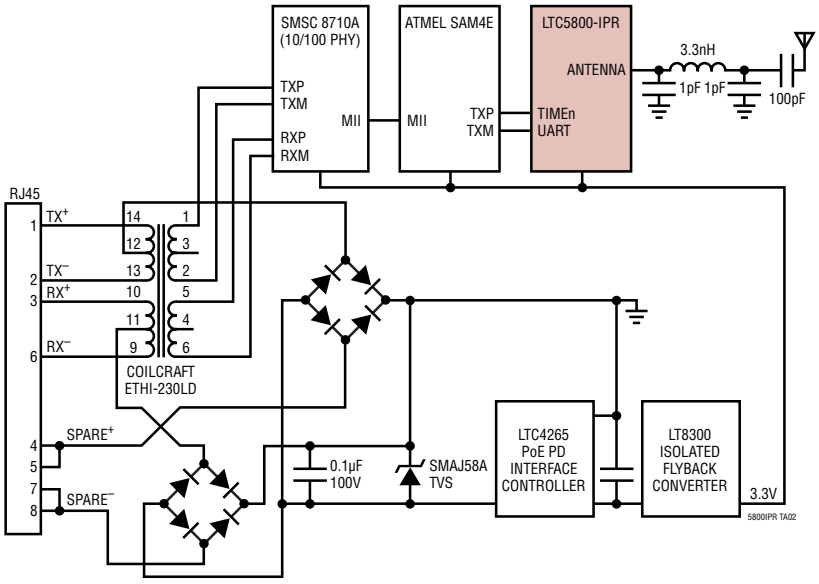
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220
2. DIMENSION "b" APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. DRAWING NOT TO SCALE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Updated Order Part Number and Manager Options	4, 29
		Added H-Grade Ordering Information and Product Specifications	4, 5, 26

TYPICAL APPLICATION

Power over Ethernet Network Manager



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTP5901-IPRA	IP Wireless Mesh Manager PCB Module with Chip Antenna	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Japan, Australia and New Zealand
LTP5902-IPRA	IP Wireless Mesh Manager PCB Module with MMCX Antenna Connector	Includes Modular Radio Certification in the United States, Canada, Europe, South Korea, Japan, Taiwan, India, Australia and New Zealand
LTP5901-IPRB	IP Wireless Mesh 100 Mote Manager PCB Module with Chip Antenna	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Australia and New Zealand
LTP5902-IPRB	IP Wireless Mesh 100 Mote Manager PCB Module with MMCX Antenna Connector	Includes Modular Radio Certification in the United States, Canada, Europe, South Korea, Japan, Taiwan, India, Australia and New Zealand
LTP5901-IPRC	IP Wireless Mesh 32 Mote Manager PCB Module with Chip Antenna, External RAM Support for Up to 36 Packets Per Second	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Australia and New Zealand
LTP5902-IPRC	IP Wireless Mesh 32 Mote Manager PCB Module with MMCX Antenna Connector, External RAM Support for Up to 36 Packets Per Second	Includes Modular Radio Certification in the United States, Canada, Europe, South Korea, Japan, Taiwan, India, Australia and New Zealand
LTC5800-IPMA	IP Wireless Mote	Ultralow Power Mote, 72-Lead 10mm × 10mm QFN
LTP5901-IPMA	IP Wireless Mesh Mote PCB Module with Chip Antenna	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Australia and New Zealand
LTP5902-IPMA	IP Wireless Mesh Mote PCB Module with MMCX Antenna Connector	Includes Modular Radio Certification in the United States, Canada, Europe,South Korea, Japan, Taiwan, India, Australia and New Zealand
LTC2379-18	18-Bit,1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC
LTC3388-1/ LTC3388-3	20V High Efficiency Nanopower Step-Down Regulator	860nA I_Q in Sleep, 2.7V to 20V Input, V_{OUT}: 1.2V to 5.0V, Enable and Standby Pins

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