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SN74LVC540A-Q1
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
SCAS712B−SEPTEMBER 2003−REVISED FEBRUARY 2008

FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Operates From 2 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.3 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DW OR PW PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	20	V_{CC}
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8
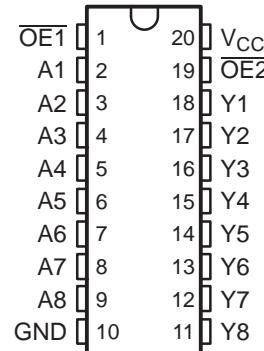
DESCRIPTION/ORDERING INFORMATION

The SN74LVC540A octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

This device is ideal for driving bus lines or buffer-memory address registers. This device features inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC – DW	Reel of 2000	SN74LVC540AQDWRQ1	L540AQ1
	TSSOP – PW	Reel of 2000	SN74LVC540AQPWRQ1	L540AQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

![warning symbol] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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FUNCTION TABLE

INPUTS			OUTPUT
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels
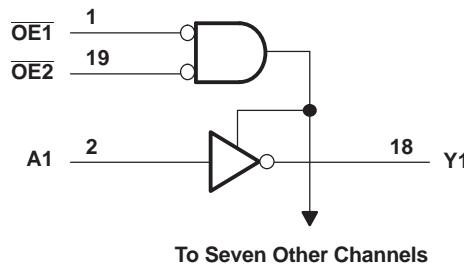
Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DW package		58	°C/W
		PW package		83	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Link(s): *SN74LVC540A-Q1*

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SCAS712B−SEPTEMBER 2003−REVISED FEBRUARY 2008

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
T_A	Operating free-air temperature		−40	125	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		2.7 V to 3.6 V	V_{CC} − 0.2			V
	I_{OH} = −12 mA		2.7 V		2.2		
			3 V		2.4		
	I_{OH} = −24 mA		3 V		2.2		
V_{OL}	I_{OL} = 100 µA		2.7 V to 3.6 V			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5	µA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±15	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			10	µA
	3.6 V ≤ V_I ≤ 5.5 V[2]					10	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	µA
C_i	V_I = V_{CC} or GND		3.3 V		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2)   This applies in the disabled state only.

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y		7.1	1	5.3	ns
t_{en}	$\overline{OE}$	Y		8	1	6.6	ns
t_{dis}	$\overline{OE}$	Y		8.2	1	7.4	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	56	31	pF
	Outputs disabled		3	3	

Product Folder Link(s): *SN74LVC540A-Q1*

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
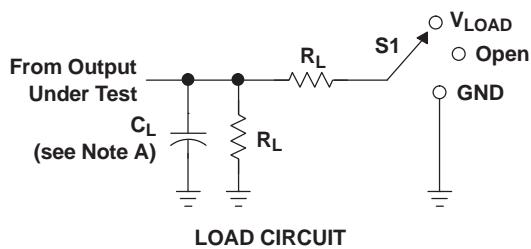
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING
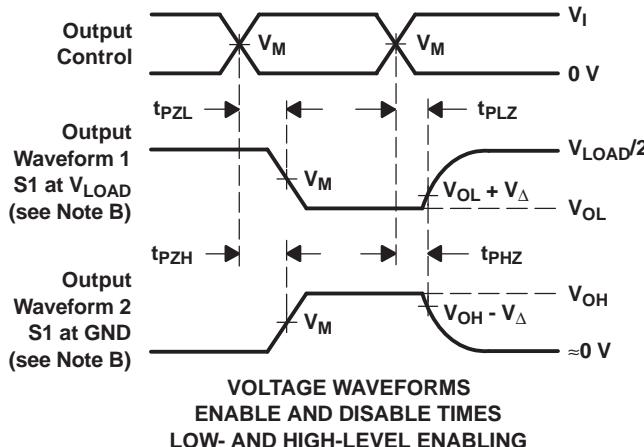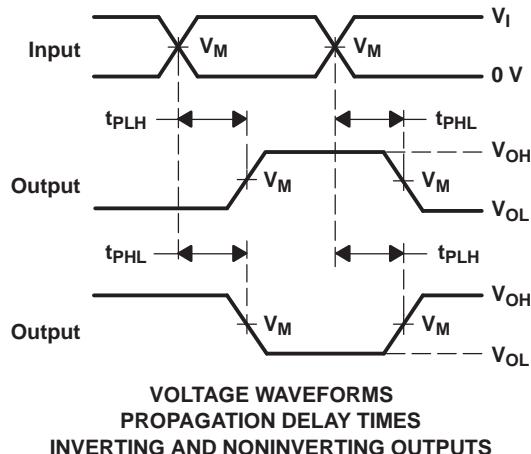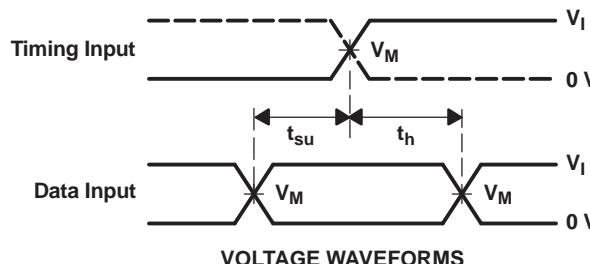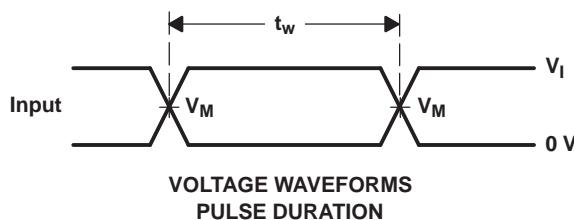
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC540AQDWRG4Q1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L540AQ1	Samples
CLVC540AQPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L540AQ1	Samples
SN74LVC540AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L540AQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC540A-Q1 :

- Catalog: SN74LVC540A

- Enhanced Product: SN74LVC540A-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
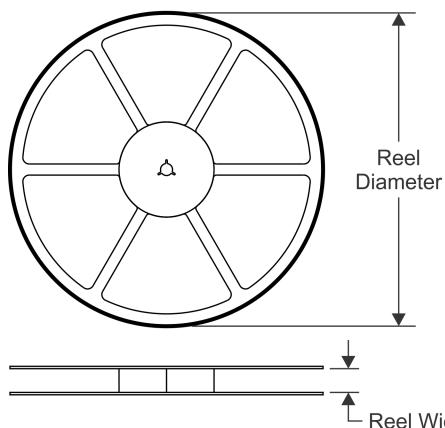
TAPE DIMENSIONS
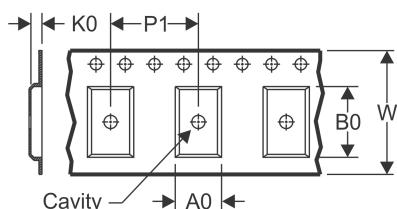
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
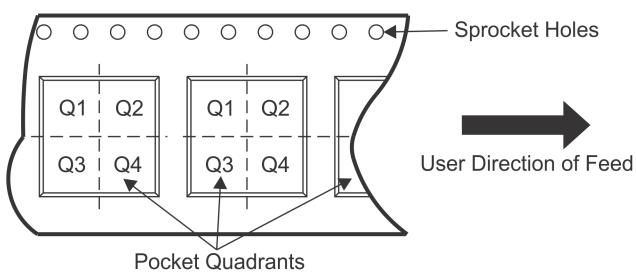
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC540AQDWRG4Q1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CLVC540AQPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC540AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC540AQDWRG4Q1	SOIC	DW	20	2000	367.0	367.0	45.0
CLVC540AQPWRG4Q1	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC540AQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30 / 0,19

⊕ 0,10 Ⓜ

20   11

4,50 / 4,30 ⟋D⟍

6,60 / 6,20

1   10

6,60 / 6,40

⟋C⟍

0,15 NOM

Gage Plane

0,25

0°−8°

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10
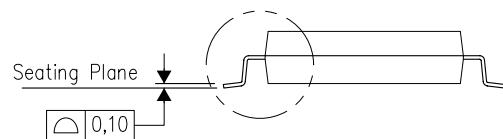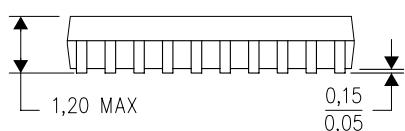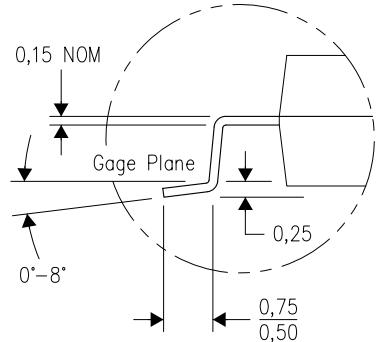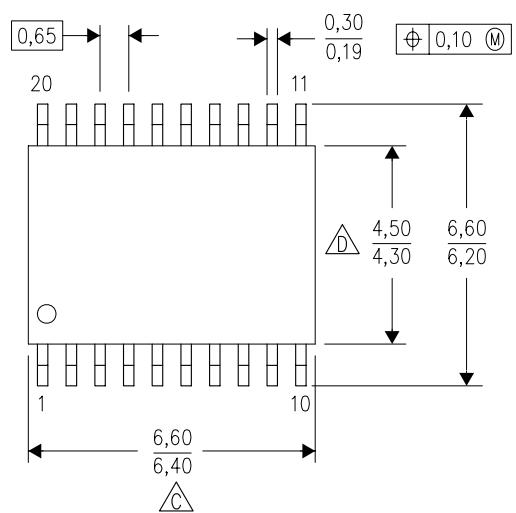
4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
      ⟋C⟍   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
      ⟋D⟍   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

5,6

20x0,25

5,6

1,55

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around
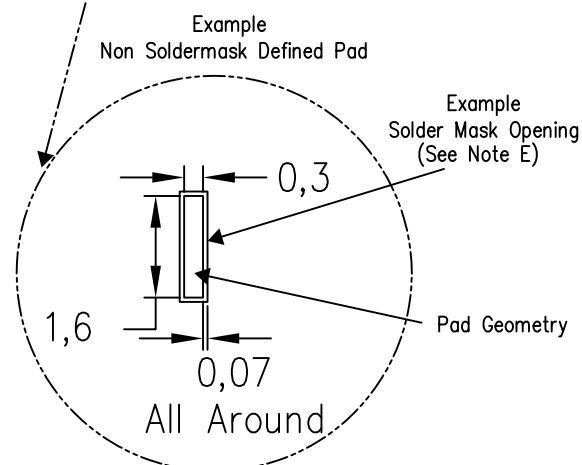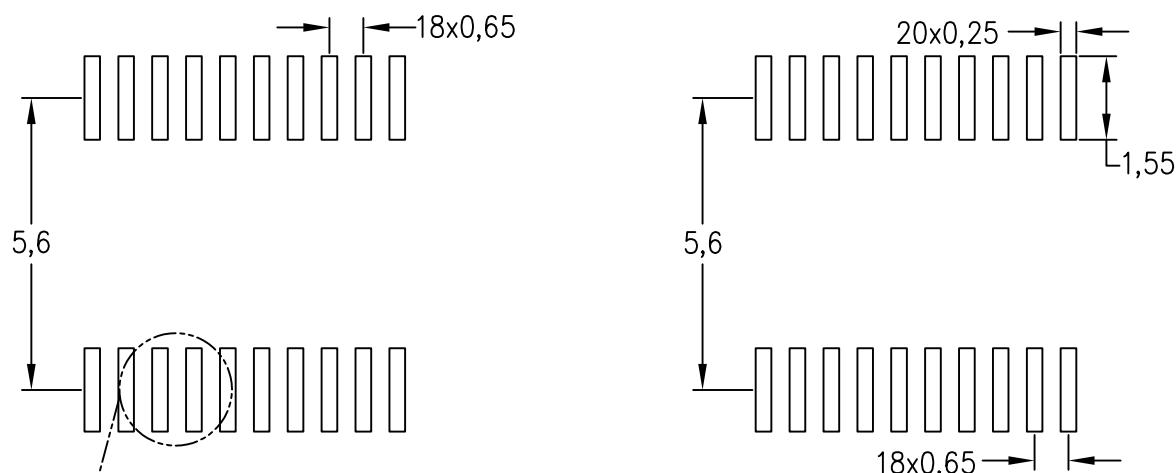
4211284−5/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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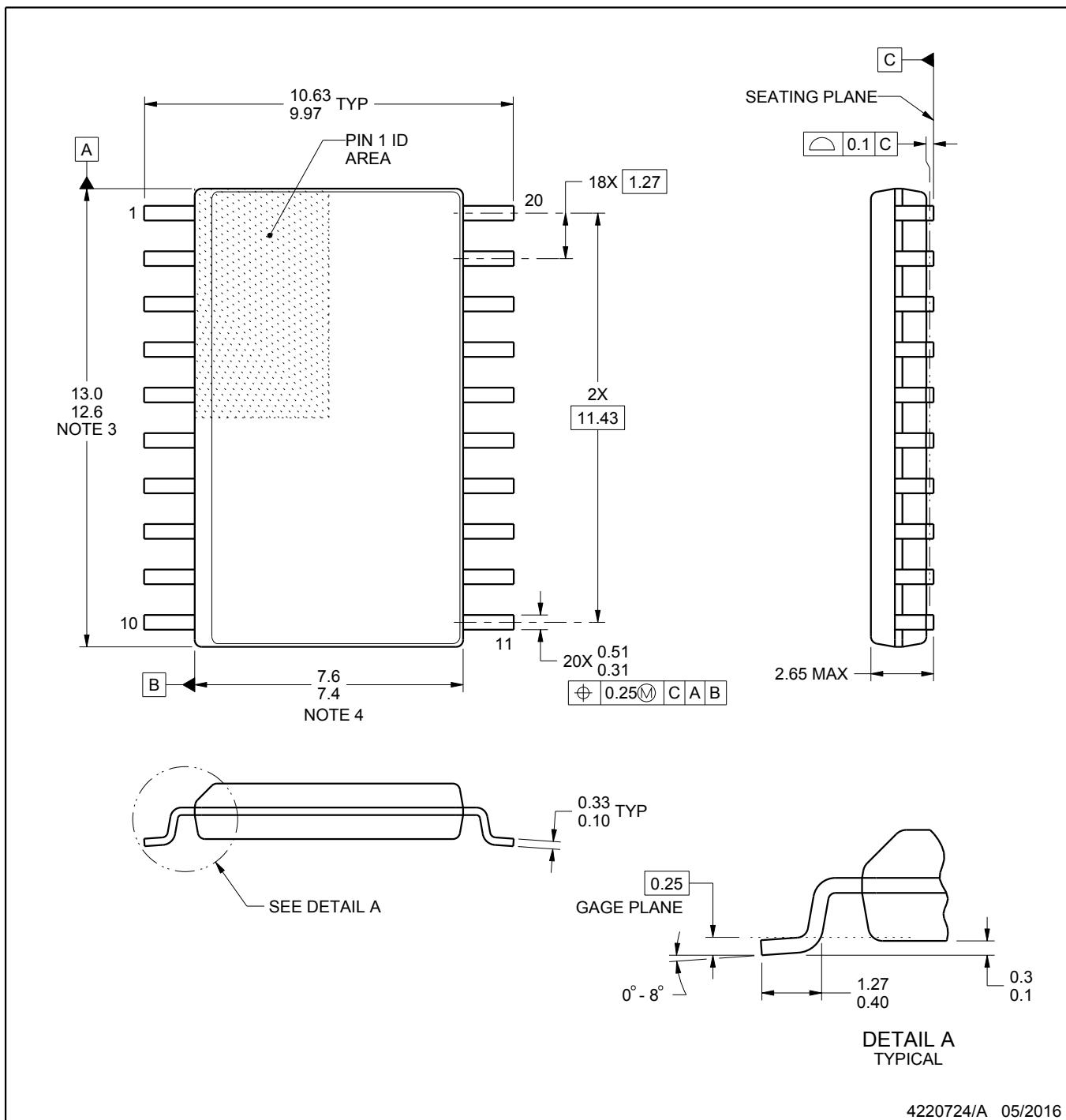
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20X (0.6)

18X (1.27)

20

SYMM

(R0.05)
TYP

10

11

(9.3)
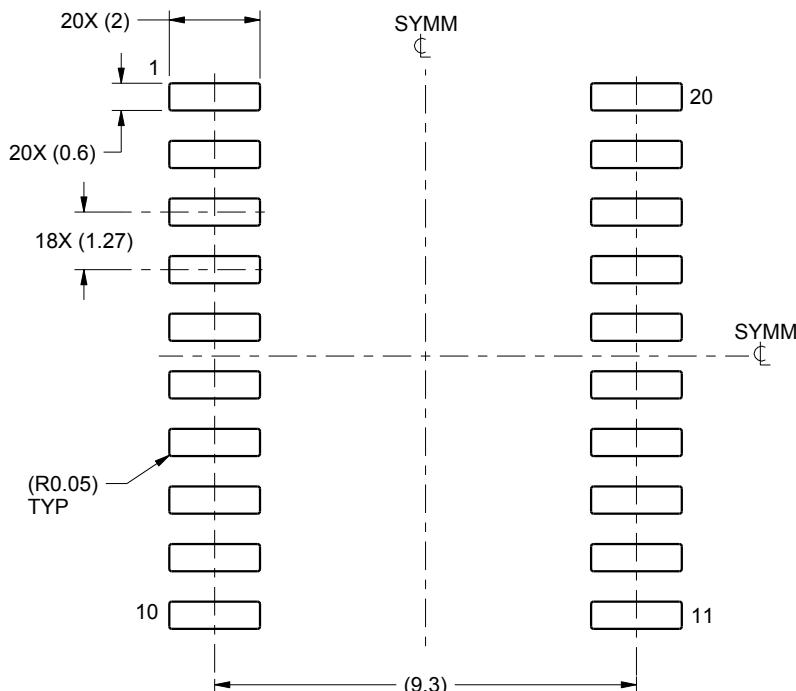
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
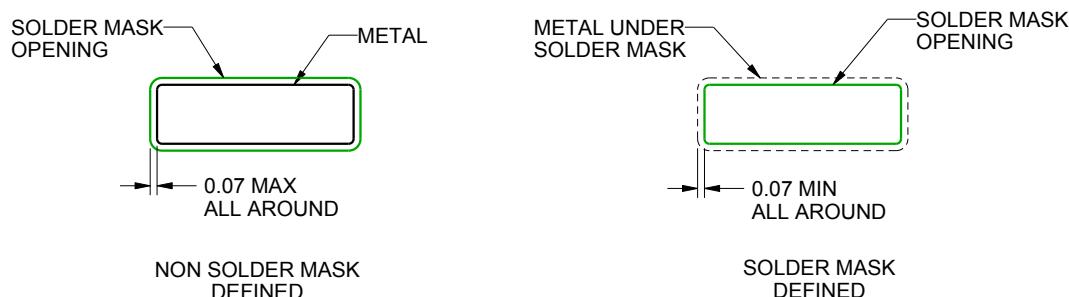
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
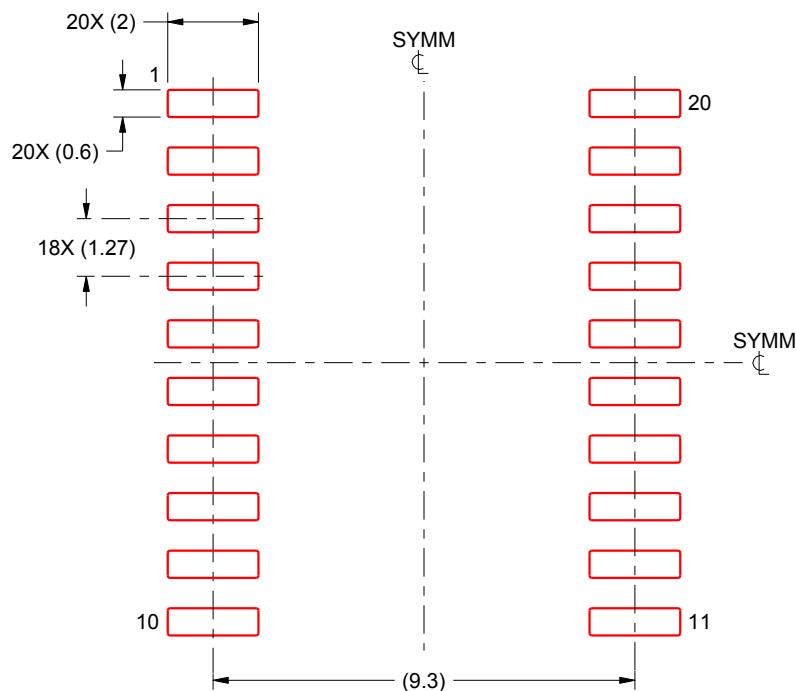
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.