

## 3-W High-Voltage Switchmode Regulator

### FEATURES

- 10- to 70-V Input Range
- Current-Mode Control
- On-Chip 150-V, 5- $\Omega$  MOSFET Switch
- Reference Selection  
Si9100 –  $\pm 1\%$
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$  and  $\overline{\text{RESET}}$

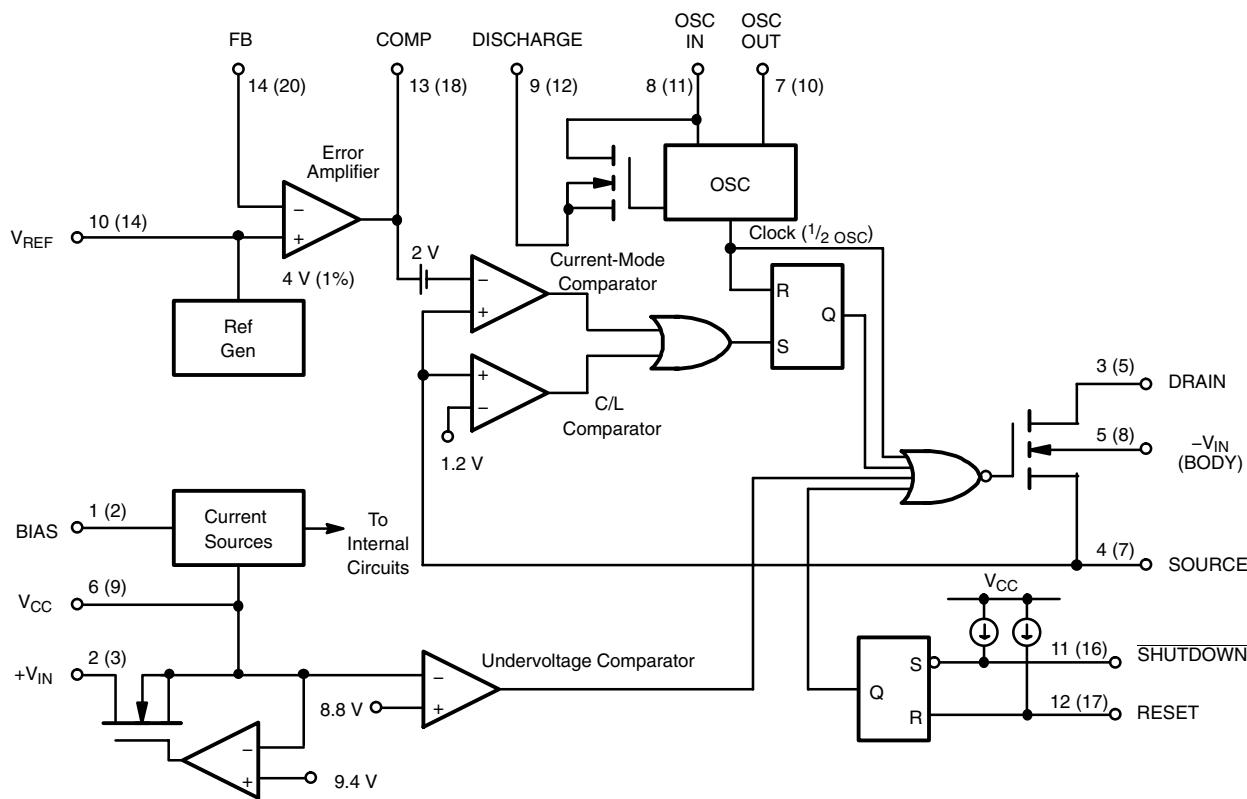
### DESCRIPTION

The Si9100 high-voltage switchmode regulators are monolithic BiC/DMOS integrated circuits which contain most of the components necessary to implement high-efficiency dc-to-dc converters up to 3 watts. They can either be operated from a low-voltage dc supply, or directly from a 10- to 70-V unregulated dc power source. The Si9100 may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward),

or by using a level shift circuit can generate a +5-V or a -5-V non-isolated output from a -48-V source.

The Si9100 is available in both standard and lead (Pb)-free 14-pin plastic DIP and 20-pin PLCC packages which are specified to operate over the industrial temperature range of -40°C to 85°C.

### FUNCTIONAL BLOCK DIAGRAM



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Applications information, see AN702 and AN713.

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ( $V_{CC} < +V_{IN} + 0.3$ V)	
$V_{CC}$	15 V
$+V_{IN}$	70 V
$V_{DS}$	150 V
$I_D$ (Peak) (Note: 300 $\mu$ s pulse, 2% duty cycle)	2.5 A
$I_D$ (rms)	350 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN)	-0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE)	-0.3 V to 7 V
HV Pre-Regulator Input Current (continuous)	3 mA
Storage Temperature	-65 to 125°C
Operating Temperature	-40 to 85°C

Junction Temperature ( $T_J$ )	150°C
Power Dissipation (Package) <sup>a</sup>	
14-Pin Plastic DIP (J Suffix) <sup>b</sup>	750 mW
20-Pin PLCC (N Suffix) <sup>c</sup>	1400 mW
Thermal Impedance ( $\Theta_{JA}$ )	
14-Pin Plastic DIP	167°C/W
20-Pin PLCC	90°C/W

## Notes

- a. Device mounted with all leads soldered or welded to PC board.
- b. Derate 6 mW/°C above 25°C
- c. Derate 11.2 mW/°C above 25°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$							
$V_{CC}$	9.5 V to 13.5 V	$R_{OSC}$	24 k $\Omega$ to 1 M $\Omega$				
$+V_{IN}$	10 V to 70 V	Linear Inputs	0 to 7 V				
$f_{OSC}$	40 kHz to 1 MHz	Digital Inputs	0 to $V_{CC}$				

SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified  DISCHARGE = $-V_{IN} = 0$ V $V_{CC} = 10$ V, $+V_{IN} = 48$ V $R_{BIAS} = 390$ k $\Omega$ , $R_{OSC} = 330$ k $\Omega$	$Temp^b$	Limits			Unit
				Min <sup>c</sup>	Typ <sup>d</sup>	Max <sup>c</sup>	
<b>Reference</b>							
Output Voltage	$V_R$	OSC IN = $-V_{IN}$ (OSC Disabled), $R_L = 10$ M $\Omega$	Room	3.92	4.0	4.08	V
Output Impedance <sup>e</sup>	$Z_{OUT}$		Room	15	30	45	k $\Omega$
Short Circuit Current	$I_{SREF}$	$V_{REF} = -V_{IN}$	Room	70	100	130	$\mu$ A
Temperature Stability <sup>e</sup>	$T_{REF}$		Full		0.5	1.0	mV/°C
<b>Oscillator</b>							
Maximum Frequency <sup>e</sup>	$f_{MAX}$	$R_{OSC} = 0$	Room	1	3		MHz
Initial Accuracy	$f_{OSC}$	$R_{OSC} = 330$ k $\Omega$ , See Note f	Room	80	100	120	kHz
		$R_{OSC} = 150$ k $\Omega$ , See Note f	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5$ V) - f, (9.5 V)/f(9.5 V)	Room		10	15	%
Temperature Coefficient <sup>e</sup>	$T_{osc}$		Full		200	500	ppm/°C
<b>Error Amplifier</b>							
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP OSC In = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	$I_{FB}$	OSC IN = $-V_{IN}$ , $V_{FB} = 4$ V	Room		25	500	nA
Input OFFSET Voltage	$V_{os}$	OSC IN = $-V_{IN}$ , (OSC Disabled)	Room		$\pm 15$	$\pm 40$	mV
Open Loop Voltage Gain <sup>e</sup>	$A_{VOL}$		Room	60	80		dB
Unity Gain Bandwidth <sup>e</sup>	$BW$		Room		1		MHz
Dynamic Output Impedance <sup>e</sup>	$Z_{OUT}$		Room		1000	2000	$\Omega$
Output Current	$I_{OUT}$	SOURCE ( $V_{FB} = 3.4$ V)	Room		-2.0	-1.4	mA
		SINK ( $V_{FB} = 4.5$ V)	Room	0.12	0.15		
Power Supply Rejection	$PSRR$	OSC IN = $-V_{IN}$ , (OSC Disabled)	Room	50	70		dB

**SPECIFICATIONS<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ , $R_{OSC} = 330\text{ k}\Omega$	Temp <sup>b</sup>	Limits			Unit
				Min <sup>c</sup>	Typ <sup>d</sup>	Max <sup>c</sup>	
<b>Current Limit</b>							
Threshold Voltage	$V_{SOURCE}$	$R_L = 100\text{ }\Omega$ from DRAIN to $V_{CC}$ $V_{FB} = 0\text{ V}$	Room	1.0	1.2	1.4	V
Delay to Output <sup>e</sup>	$t_d$	$R_L = 100\text{ }\Omega$ from DRAIN to $V_{CC}$ $V_{SOURCE} = 1.5\text{ V}$ , See Figure 1	Room		100	200	ns
<b>Pre-Regulator/Start-Up</b>							
Input Voltage	$+V_{IN}$	$I_{IN} = 10\text{ }\mu\text{A}$	Room			70	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq 10\text{ V}$	Room			10	$\mu\text{A}$
Pre-Regulator Start-Up Current	$I_{START}$	Pulse Width $\leq 300\text{ }\mu\text{s}$ $V_{CC} = V_{UVLO}$	Room	8	15		mA
$V_{CC}$ Pre-Regulator Turn-Off Threshold Voltage	$V_{REG}$	$I_{PRE-REGULATOR} = 10\text{ }\mu\text{A}$	Room	7.8	9.4	9.7	V
Undervoltage Lockout	$V_{UVLO}$	$R_L = 100\text{ }\Omega$ from DRAIN to $V_{CC}$ See Detailed Description	Room	7.0	8.8	9.2	
$V_{REG} - V_{UVLO}$	$V_{DELTA}$		Room	0.3	0.6		
<b>Supply</b>							
Supply Current	$I_{CC}$		Room	0.45	0.6	1.0	mA
Bias Current	$I_{BIAS}$		Room	10	15	20	$\mu\text{A}$
<b>Logic</b>							
SHUTDOWN Delay <sup>e</sup>	$t_{SD}$	$V_{SOURCE} = -V_{IN}$ , See Figure 2	Room		50	100	ns
SHUTDOWN Pulse Width <sup>e</sup>	$t_{SW}$	See Figure 3	Room	50			
RESET Pulse Width <sup>e</sup>	$t_{RW}$		Room	50			
Latching Pulse Width SHUTDOWN and RESET Low	$t_{LW}$		Room	25			
Input Low Voltage	$V_{IL}$		Room			2.0	V
Input High Voltage	$V_{IH}$		Room	8.0			
Input Current, Input Voltage High	$I_{IH}$	$V_{IN} = 10\text{ V}$	Room		1	5	
Input Current, Input Voltage Low	$I_{IL}$	$V_{IN} = 0\text{ V}$	Room	-35	-25		$\mu\text{A}$
<b>MOSFET Switch</b>							
Breakdown Voltage	$V_{(BR)DSS}$	$V_{SOURCE} = \bar{S}\text{HUTDOWN} = 0\text{ V}$ $I_{DRAIN} = 100\text{ }\mu\text{A}$	Full	150	180		V
Drain-Source On Resistance <sup>g</sup>	$r_{DS(on)}$	$V_{SOURCE} = 0\text{ V}$ , $I_{DRAIN} = 100\text{ mA}$	Room		3	5	$\Omega$
Drain Off Leakage Current	$I_{DSS}$	$V_{SOURCE} = \bar{S}\text{HUTDOWN} = 0\text{ V}$ $V_{DRAIN} = 100\text{ V}$	Room			10	$\mu\text{A}$
Drain Capacitance	$C_{DS}$	$V_{SOURCE} = \bar{S}\text{HUTDOWN} = 0\text{ V}$	Room		35		pF

## Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room =  $25^\circ\text{C}$ , Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- $C_{STRAY}$  Pin 8 =  $\leq 5\text{ pF}$
- Temperature coefficient of  $r_{DS(on)}$  is 0.75% per  $^\circ\text{C}$ , typical.

### TIMING WAVEFORMS

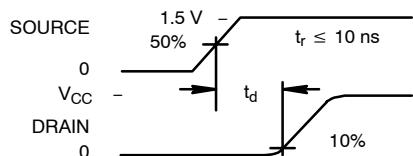


FIGURE 1.

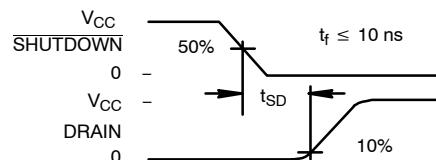


FIGURE 2.

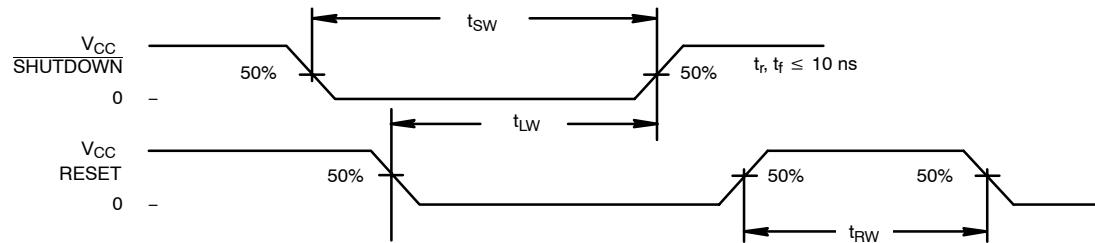


FIGURE 3.

### TYPICAL CHARACTERISTICS

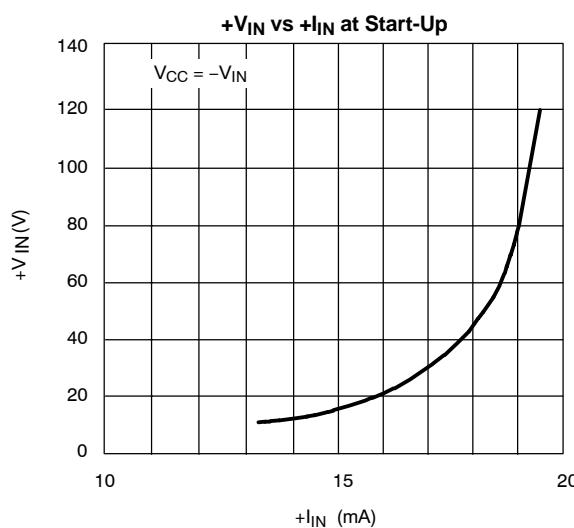


FIGURE 4.

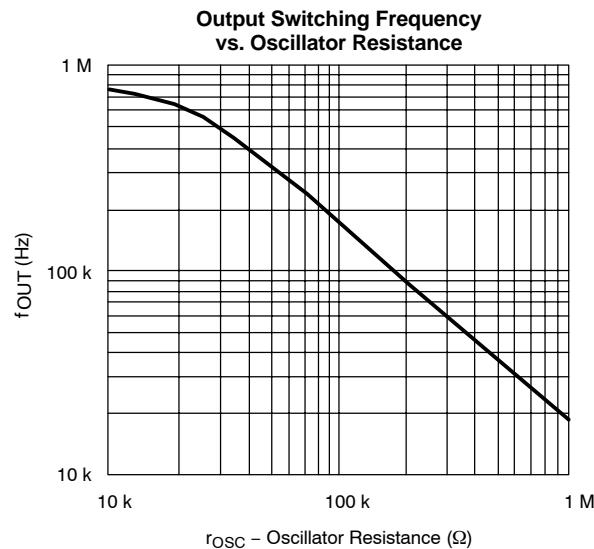
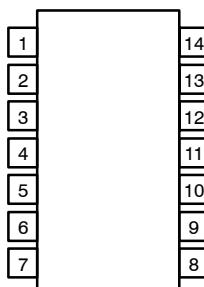


FIGURE 5.

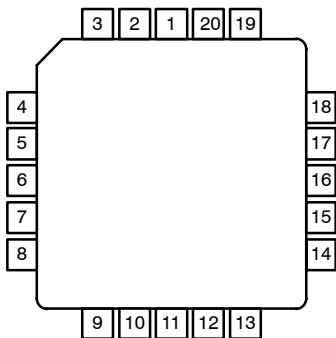
## PIN CONFIGURATIONS

PDIP-14



Top View

PLCC-20



Top View

PIN DESCRIPTION		
Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
+V <sub>IN</sub>	2	3
DRAIN	3	5
SOURCE	4	7
-V <sub>IN</sub>	5	8
V <sub>CC</sub>	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V <sub>REF</sub>	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20

\*Pins 1, 4, 6, 13, 15, and 19 = N/C

## ORDERING INFORMATION

Standard Part Number	Lead (Pb)-Free Part Number	Temperature Range	Package
Si9100DJ02	Si9100DJ02—E3	-40 to 85 °C	PDIP-14
Si9100DN02	Si9100DN02—E3		PLCC-20

## DETAILED DESCRIPTION

### Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, +V<sub>IN</sub> will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V<sub>IN</sub> and V<sub>CC</sub>. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V<sub>CC</sub> pin. The constant current is

disabled when V<sub>CC</sub> exceeds 9.4 V. If V<sub>CC</sub> is not forced to exceed the 9.4-V threshold, then V<sub>CC</sub> will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V<sub>CC</sub> exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V<sub>CC</sub> such that the constant current source is always disabled.

## DETAILED DESCRIPTION (CONT'D)

**Note:** During start-up or when  $V_{CC}$  drops below 9.4 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the  $V_{CC}$  supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

### BIAS

To properly set the bias for the Si9100, a 390-k $\Omega$  resistor should be tied from BIAS to  $-V_{IN}$ . This determines the magnitude of bias current in all of the analog sections and the pull-up current for the SHUTDOWN and RESET pins. The current flowing in the bias resistor is nominally 15  $\mu$ A.

### Reference Section

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. During the reference trimming procedure the error amplifier is connected for unity gain in order to compensate for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

### Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input leakage current. The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

### Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an

external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5- $\mu$ s pulse width, typical values would be 100 pF in series with 3 k $\Omega$  to OSC IN.

### SHUTDOWN and RESET

SHUTDOWN and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is off whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

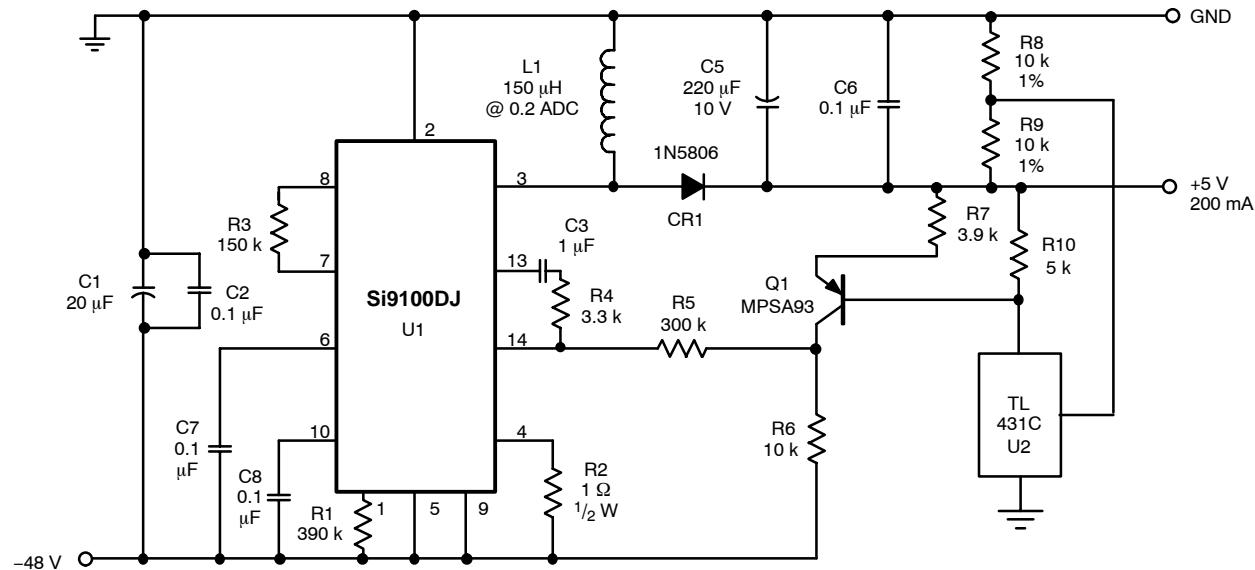
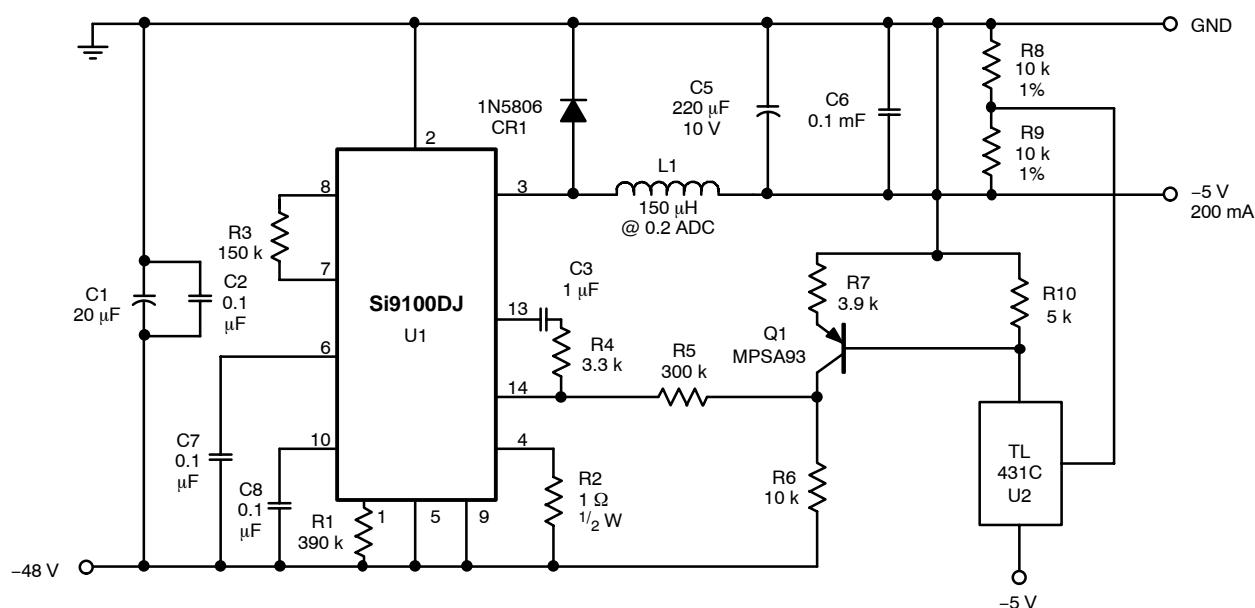
Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

**Table 1.** Truth Table for the SHUTDOWN and RESET Pins

SHUTDOWN	RESET	Output
H	H	Normal Operation
H	1	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
1	L	Off (Latched, No Change)

### Output Switch

The output switch is a 5- $\Omega$ , 150-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to  $-V_{IN}$  and is independent of the SOURCE.

**APPLICATIONS**

**FIGURE 6.** Buck-Boost, Non-Isolated 1-W Supply

**FIGURE 7.** Non-Isolated 1-W Supply (Buck)

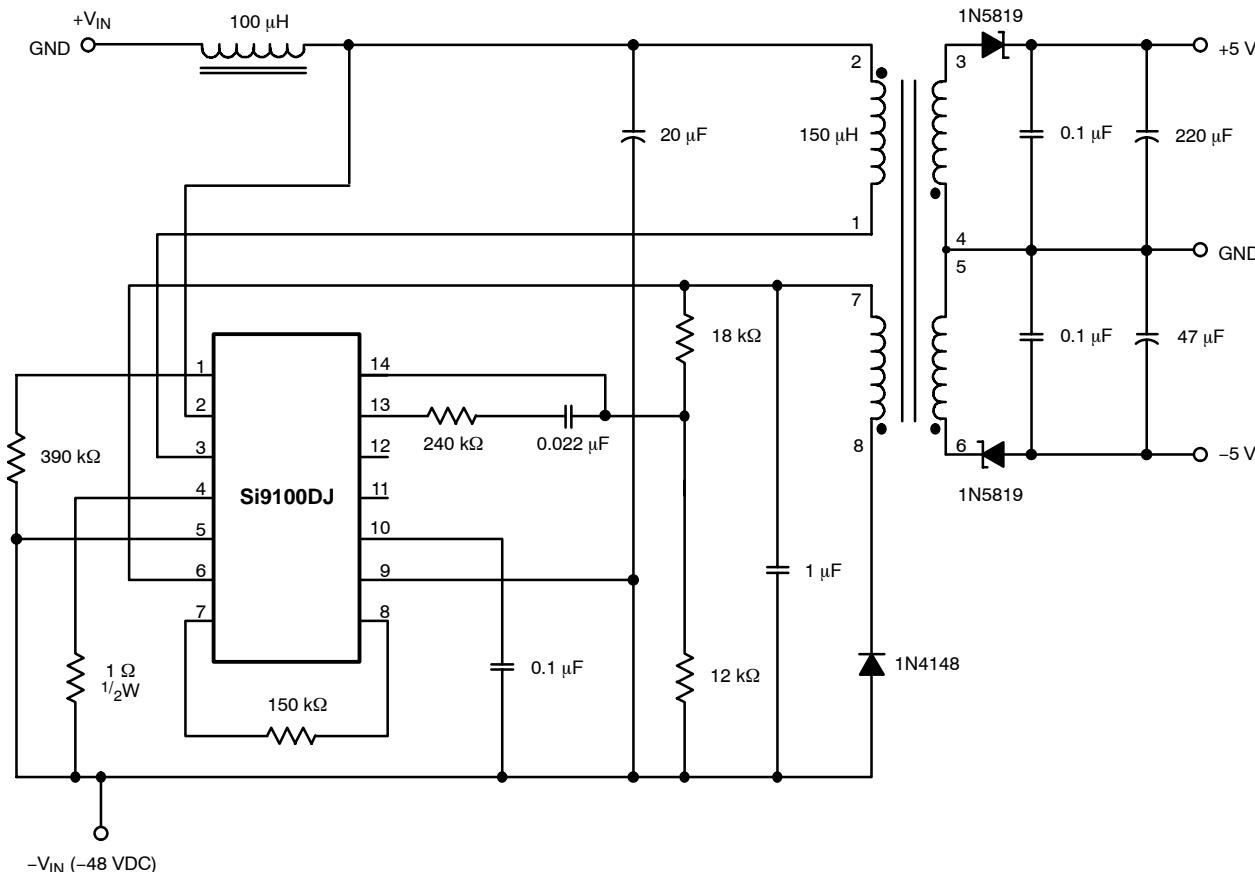
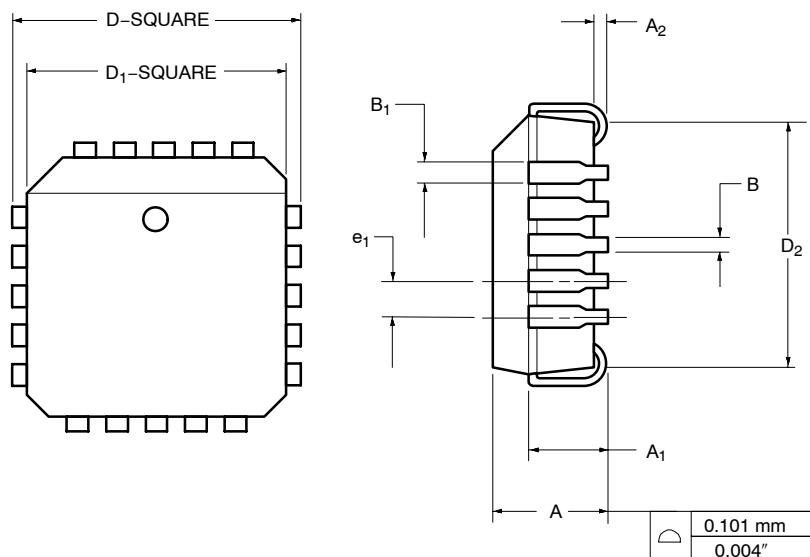


FIGURE 8. 1-W Flyback Converter for Telecommunications Power Supplies\*

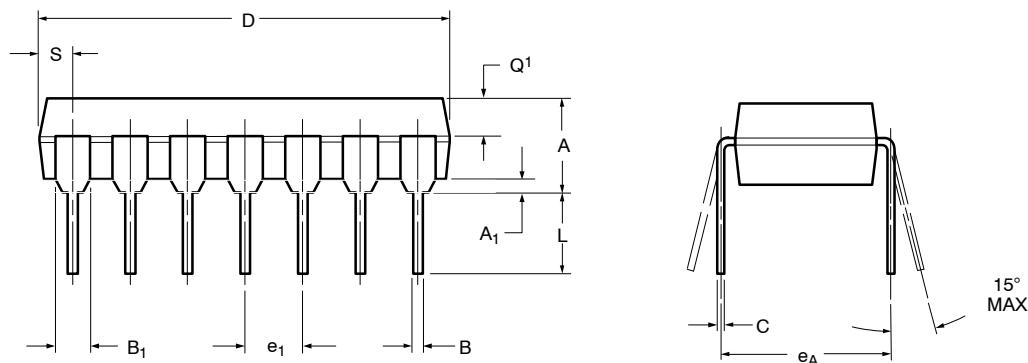
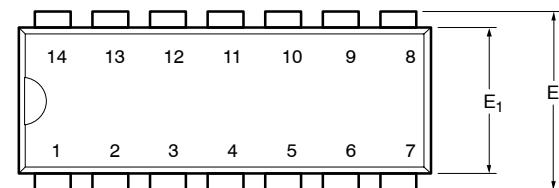
\* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN713 and AN702.

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**PLCC: 20-LEAD (POWER IC ONLY)**


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	4.20	4.57	0.165	0.180
<b>A<sub>1</sub></b>	2.29	3.04	0.090	0.120
<b>A<sub>2</sub></b>	0.51	—	0.020	—
<b>B</b>	0.331	0.553	0.013	0.021
<b>B<sub>1</sub></b>	0.661	0.812	0.026	0.032
<b>D</b>	9.78	10.03	0.385	0.395
<b>D<sub>1</sub></b>	8.890	9.042	0.350	0.356
<b>D<sub>2</sub></b>	7.37	8.38	0.290	0.330
<b>e<sub>1</sub></b>	1.27 BSC		0.050 BSC	

ECN: S-40081—Rev. A, 02-Feb-04  
DWG: 5917

**PDIP: 14-LEAD (POWER IC ONLY)**


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	17.27	19.30	0.680	0.760
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	1.02	2.03	0.040	0.080
ECN: S-40081—Rev. A, 02-Feb-04				
DWG: 5919				

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