Low Voltage/Low Skew, 1:4 PCI/PCI-X Zero Delay Clock Generator

87604I

DATA SHEET

General Description

The 87604I is a 1:4 PCI/PCI-X Clock Generator. The 87604I has a selectable REF_IN or crystal input. The REF_IN input accepts LVCMOS or LVTTL input levels. The 87604I has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiply-ing and regenerating clocks with “zero delay”. The PLL’s VCO has an operating range of 250MHz - 500MHz, allowing this device to be used in a variety of general purpose clocking applications. For PCI/PCI-X applications in particular, the VCO frequency should be set to 400MHz. This can be accomplished by supplying 33.33MHz, 25MHz, 20MHz, or 16.66MHz on the reference clock or crystal input and by selecting ÷12, ÷16, ÷20, or ÷24, respectively as the feedback divide value. The divider on the output bank can then be configured to generate 33.33MHz (÷12), 66.66MHz (÷6), 100MHz (÷4), or 133.33MHz (÷3).

The 87604I is characterized to operate with its core supply at 3.3V and the bank supply at 3.3V or 2.5V. The 87604I is packaged in a small 6.1mm x 9.7mm TSSOP body, making it ideal for use in space-constrained applications.

Features

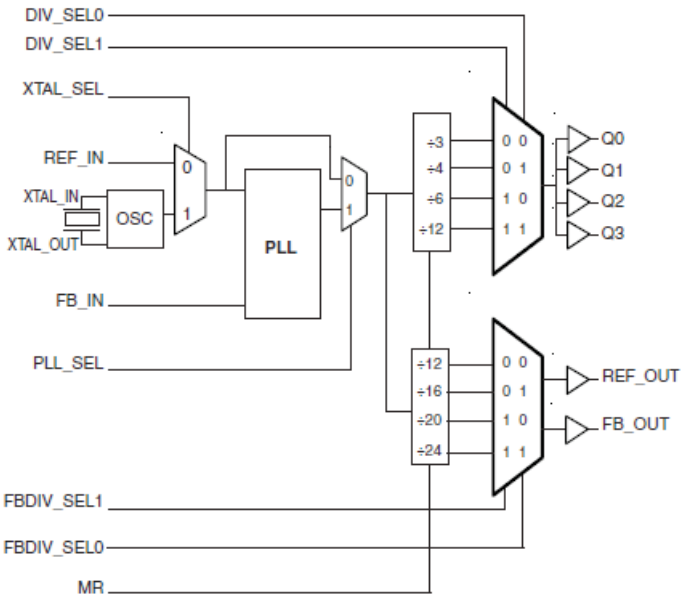
- Fully integrated PLL
- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_IN clock input
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF_IN input frequency: 41.67MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz
- Separate feedback control for generating PCI / PCI-X frequencies from a 16.66MHz or 20MHz crystal, or 25MHz or 33.33MHz reference frequency
- VCO range: 250MHz to 500MHz
- Cycle-to-cycle jitter: 120ps (maximum)
- Period jitter, RMS: 20ps (maximum)
- Output skew: 65ps (maximum)
- Static phase offset: 160ps ± 160ps
- Voltage Supply Modes:

  $V_{DD}/V_{DDA}/V_{DDO}$

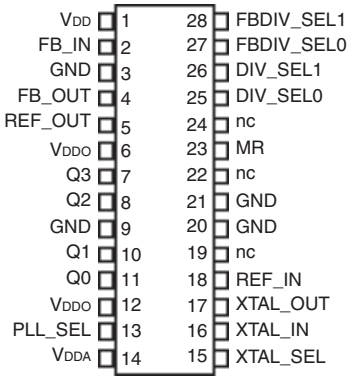
  3.3/3.3/3.3

  3.3/3.3/2.5
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



87604I
28-Lead TSSOP, 240MIL
6.1mm x 9.7mm x 0.92mm
body package
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DD}	Power		Core supply pin.
2	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
3, 9, 20, 21	GND	Power		Power supply ground.
4	FB_OUT	Output		Feedback output. Connect to FB_IN. LVCMOS / LVTTL interface levels.
5	REF_OUT	Output		Reference clock output. LVCMOS / LVTTL interface levels.
6, 12	V_{DDO}	Power		Output supply pin
7, 8, 10, 11	Q3, Q2, Q1, Q0	Output		Clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
13	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
14	V_{DDA}	Power		Analog supply pin. See Applications Note for filtering.
15	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_IN when LOW. LVCMOS / LVTTL interface levels.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
18	REF_IN	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
19, 22, 24	nc	Unused		No connect.
23	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
25, 26	DIV_SEL0, DIV_SEL1	Input	Pulldown	Selects divide value for clock outputs as described in Table 3. LVCMOS / LVTTL interface levels.
27, 28	FBDIV_SEL0, FBDIV_SEL1	Input	Pulldown	Selects divide value for reference clock output and feedback output. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor				51	kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51	kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			9	pF
		V_{DD}, V_{DDA} = 3.465V; V_{DDO} = 2.625V			11	pF
R_{OUT}	Output Impedance			15		Ω

Table 3A. Output Control Pin Function Table

Inputs	Outputs	
MR	Q0:Q3	FB_OUT, REF_OUT
1	LOW	LOW
0	Active	Active

Table 3B. Operating Mode Function Table

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

Table 3C. PLL Input Function Table

Inputs	
XTAL_SEL	PLL Input
0	REF_IN
1	XTAL Oscillator

Table 3D. Control Function Table

Inputs					Outputs		
					PLL_SEL=1	Frequency	
FBDIV_SEL1	FBDIV_SEL0	DIV_SEL1	DIV_SEL0	Reference Frequency Range (MHz)	Q0:Q3	Q0:Q3 (MHz)	FB_OUT (MHz)
0	0	0	0	16.67 - 41.67	x 4	66.68 - 166.68	16.67 - 41.67
0	0	0	1	16.67 - 41.67	x 3	50 - 125	16.67 - 41.67
0	0	1	0	16.67 - 41.67	x 2	33.34 - 83.34	16.67 - 41.67
0	0	1	1	16.67 - 41.67	x 1	16.67 - 41.67	16.67 - 41.67
0	1	0	0	12.5 - 31.25	x 5.33	66.63 - 166.56	12.5 - 31.25
0	1	0	1	12.5 - 31.25	x 4	50 - 125	12.5 - 31.25
0	1	1	0	12.5 - 31.25	x 2.667	33.34 - 83.34	12.5 - 31.25
0	1	1	1	12.5 - 31.25	x 1.33	16.63 - 41.56	12.5 - 31.25
1	0	0	0	10 - 25	x 6.667	66.67 - 166.68	10 - 25
1	0	0	1	10 - 25	x 5	50 - 125	10 - 25
1	0	1	0	10 - 25	x 3.33	33.30 - 83.25	10 - 25
1	0	1	1	10 - 25	x 1.66	16.60 - 41.50	10 - 25
1	1	0	0	8.33 - 20.83	x 8	66.64 - 166.64	8.33 - 20.83
1	1	0	1	8.33 - 20.83	x 6	50 - 125	8.33 - 20.83
1	1	1	0	8.33 - 20.83	x 4	33.32 - 83.32	8.33 - 20.83
1	1	1	1	8.33 - 20.83	x 2	16.66 - 41.66	8.33 - 20.83

NOTE: VCO frequency range for all configurations above is 250MHz to 500MHz.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	
XTAL_IN	0V to V_{DD}
Other Inputs	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	64.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ or $2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				185	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				20	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ or $2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		2		V + 0.3	V
		REF_IN		2		V + 0.3	V
V_{IL}	Input Low Voltage	MR, DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		-0.3		0.8	V
		REF_IN		-0.3		1.3	V
I_{IH}	Input High Current	DIV_ SEL0, DIV_SEL1, FB-DIV_SEL0, FBDIV_SEL1, MR, FB_IN	V =V = 3.465V			150	µA
		XTAL_SEL, PLL_SEL	V =V = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_ SEL0, DIV_SEL1, FB-DIV_SEL0, FBDIV_SEL1, MR, FB_IN		-5			µA
		XTAL_SEL, PLL_SEL		-150			µA
V_{OH}	Output High Voltage; NOTE 1		V =V = 3.465V	2.6			V
			V =V = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V =V = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance			7		pF
Drive Level				1	mW

TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		8.33		41.67	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	0	160	325	ps
tsk(o)	Output Skew; NOTE 2, 5				65	ps
tjit(cc)	Cycle-to-Cycle Jitter; 5				120	ps
tjit(per)	Period Jitter, RMS; NOTE 3, 5, 6				20	ps
tsl(o)	Slew Rate		1		4	V/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 4		48		52	%

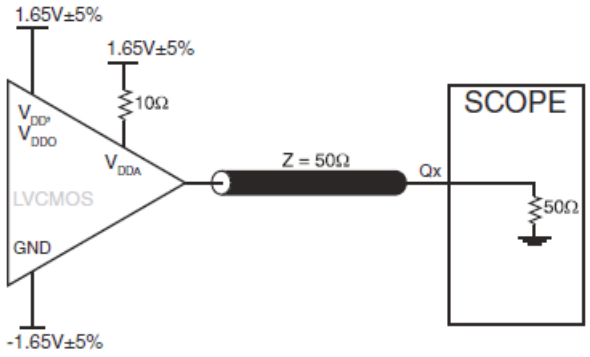
NOTE: All parameters measured with feedback and output dividers set to DIV by 12 unless otherwise noted.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Jitter performance using LVCMOS inputs.
NOTE 4: Measured using REF_IN. For XTAL input, refer to Application Note.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: This parameter is defined as an RMS value.

TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

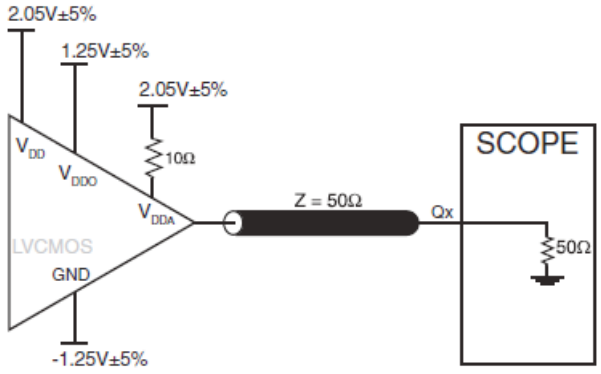
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	-365	-105	160	ps
tsk(o)	Output Skew; NOTE 2, 5				50	ps
tjit(cc)	Cycle-to-Cycle Jitter; 5				170	ps
tjit(per)	Period Jitter, RMS; NOTE 3, 5, 6				20	ps
tsl(o)	Slew Rate		1		4	V/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 4		48		52	%

See Table 7A for notes.

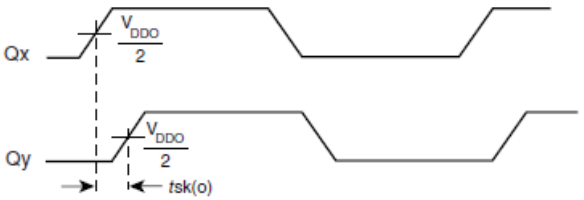
Parameter Measurement Information



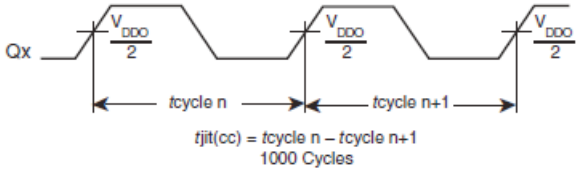
3.3V Output Load AC Test Circuit



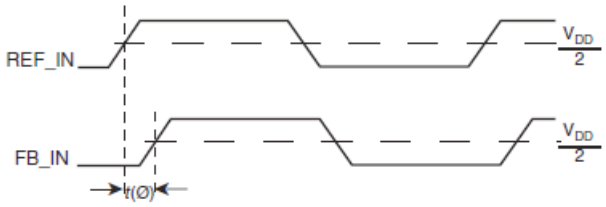
3.3V/2.5V Output Load AC Test Circuit



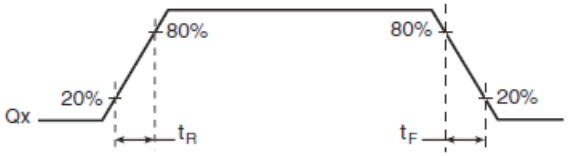
Output Skew



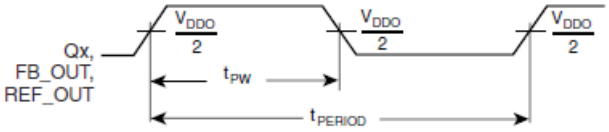
Cycle-to-Cycle Jitter



Static Phase Offset



Output Rise/Fall Time



Output Pulse Width/Pulse Width Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 87604I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

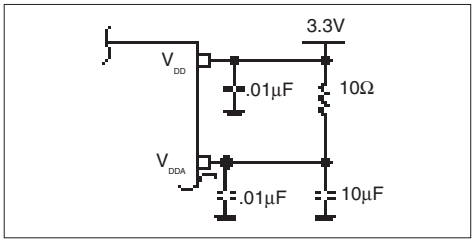


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Crystal Input Interface

The 87604I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the frequency ppm error. The optimum C1 and C2 values can be slightly adjusted for optimum frequency accuracy.

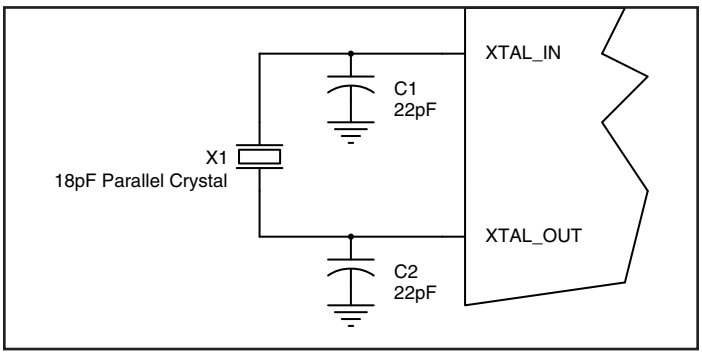


Figure 2. Crystal Input Interface

Overdriving the Crystal Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than .2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50 applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. Figure 2 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

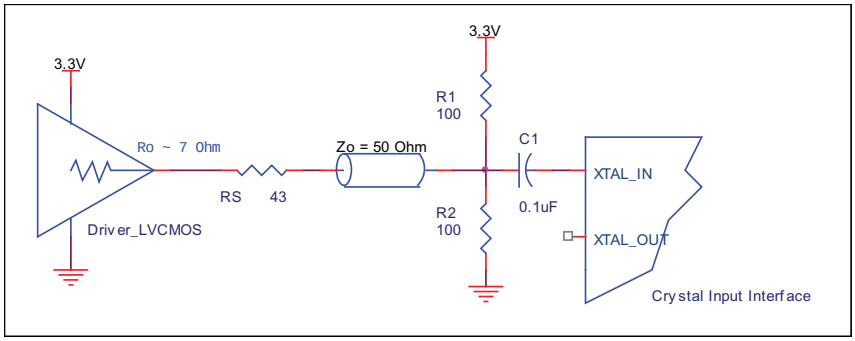


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

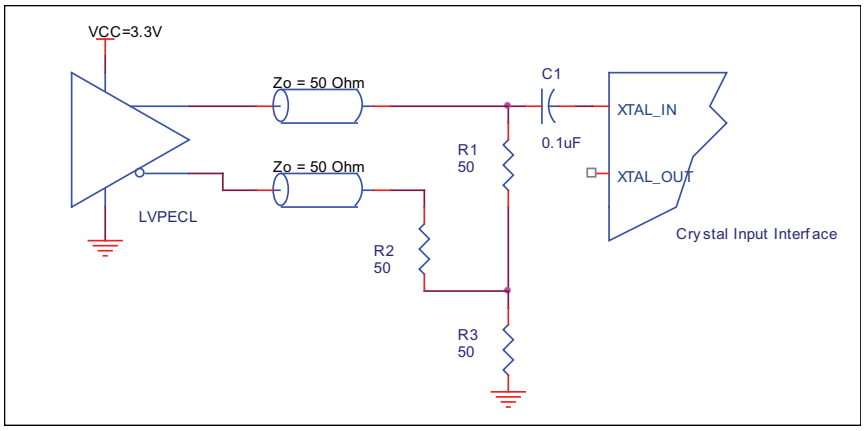


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Example

Figure 4 shows a schematic example of the 87604I. Series termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 25MHz crystal is used. The C1=22pF and C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy. The logic control inputs are either pull up or pull down depending on the application requirement. If there is space available, it is recommended to provide spare footprints as shown in the schematic for flexibility of choosing pull up or pull down.

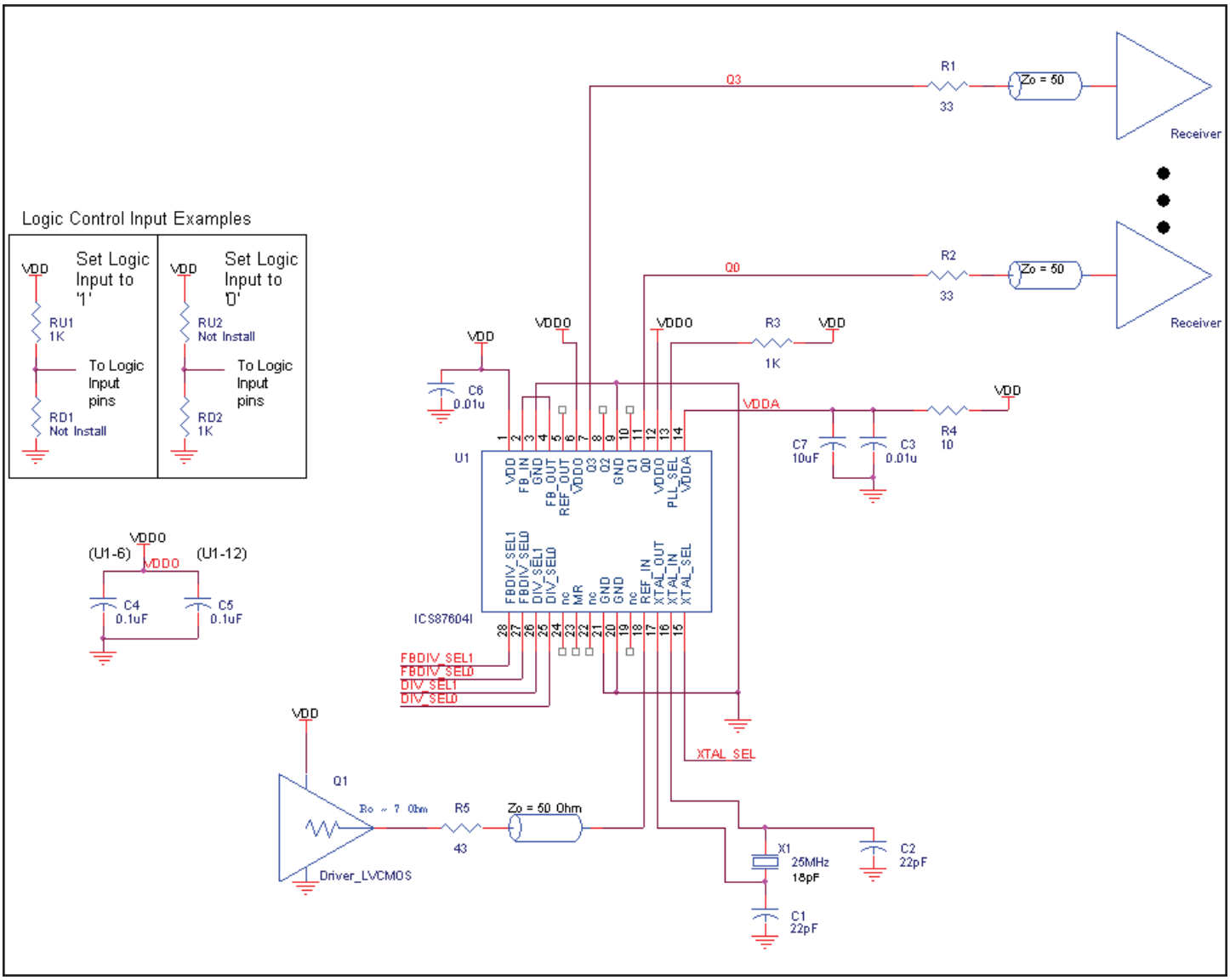


Figure 4. ICS87604I Schematic Example

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 28 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	64.5°C/W	60.4°C/W	58.5°C/W

Transistor Count

The transistor count for 87604I is: 5495

Package Outline and Package Dimensions

Package Outline - G Suffix for 28 Lead TSSOP

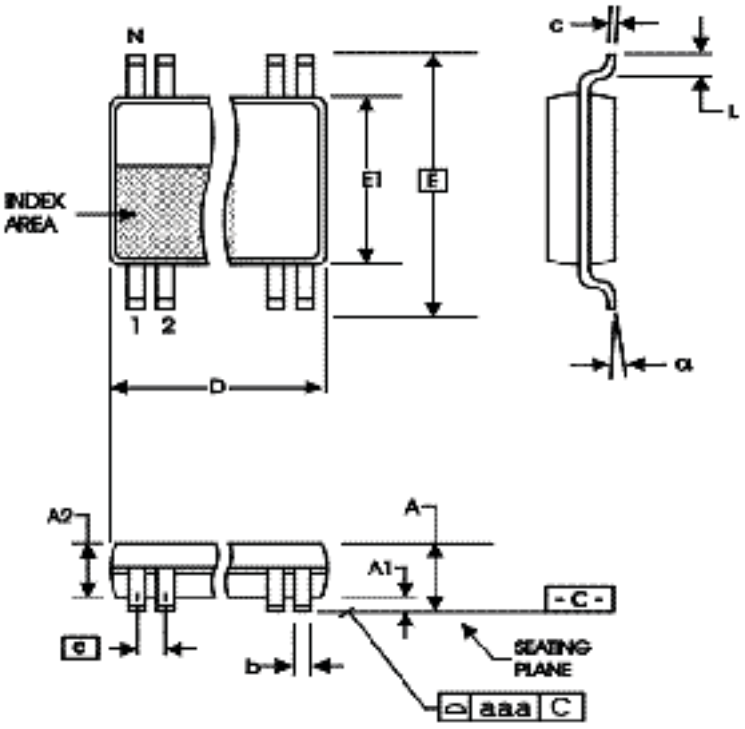


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	8.10 BASIC	
E1	6.00	6.20
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87604AGILF	ICS87604AGILF	28 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
87604AGILFT	ICS87604AGILF	28 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T7A & T7B	5	AC Characteristics Tables - corrected note sequence.	3/18/05
A	10	10	Ordering Information Table - added marking.	4/12/05
B	T5 T9	1 5 6 8 10	Pin Assignment and General Description - corrected package dimension. Crystal Characteristics - added Drive Level. Updated Output Load AC Test Circuit Diagrams. Application Information - added LVCMOS to XTAL Interface and Recommendations for Unused Input and Output Pins sections. Package Dimensions - corrected “E” and “E1” dimensions.	3/8/06
B	T9	1 10	Pin Assignment and General Description - corrected package dimension. Package Dimensions - corrected “E” and “E1” dimensions.	8/18/06
B		4 9 10	Absolute Maximum Ratings - updated Package Thermal Impedance. Added Schematic Layout. Reliability Information - updated Package Thermal Impedance.	1/11/08
B	T7A T10	1 5 8 11	Pin Assignment, corrected 173-MIL to 240-MIL. AC Characteristics Table, added Thermal Note. Updated the Overdriving the Crystal Interface section. Ordering Information Table - deleted “ICS” prefix from Part/Order Number column. Added new Header/Footer in datasheet.	4/1/10
B	T10	11	Ordering Information - removed leaded devices. Updated data sheet format.	11/11/15

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 or +408-284-8200
Fax: 408-284-2775
www.IDT.com

Technical Support
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IDT (Integrated Device Technology):

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