12-BIT, 210 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

FEATURES

- **Maximum Sample Rate: 210 MSPS**
- **12-Bit Resolution**
- **No Missing Codes**
- **Total Power Dissipation 1.23 W**
- **Internal Sample and Hold**
- **70.5-dBFS SNR at 70-MHz IF**
- **84-dBc SFDR at 70-MHz IF, 0-dB gain**
- **High Analog Bandwith up to 800 MHz**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Programmable Gain up to 6 dB for SNR/SFDR Trade-Off at High IF**
- **Reduced Power Modes at Lower Sample Rates**
- **Supports Input Clock Amplitude Down to 400 mV_{PP}**
- **Clock Duty Cycle Stabilizer**
- **No External Reference Decoupling Required**
- **Internal and External Reference Support**
- **Programmable Output Clock Position to Ease Data Capture**
- **3.3-V Analog and Digital Supply**
- **48-QFN Package (7 mm × 7 mm)**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

ADS5527 is a high performance 12-bit, 210-MSPS A/D converter. It offers state-of-the art functionality and performance using advanced techniques to minimize board space. With high analog bandwidth and low jitter input clock buffer, the ADC supports both high SNR and high SFDR at high input frequencies. It features programmable gain options that can be used to improve SFDR performance at lower full-scale analog input ranges.

In a compact 48-pin QFN, the device offers fully differential LVDS DDR (Double Data Rate) interface while parallel CMOS outputs can also be selected. Flexible output clock position programmability is available to ease capture and trade-off setup for hold times. At lower sampling rates, the ADC can be operated at scaled down power with no loss in performance. The ADS5527 includes an internal reference, while eliminating the traditional reference pins and associated external decoupling. The device also supports an external reference mode.

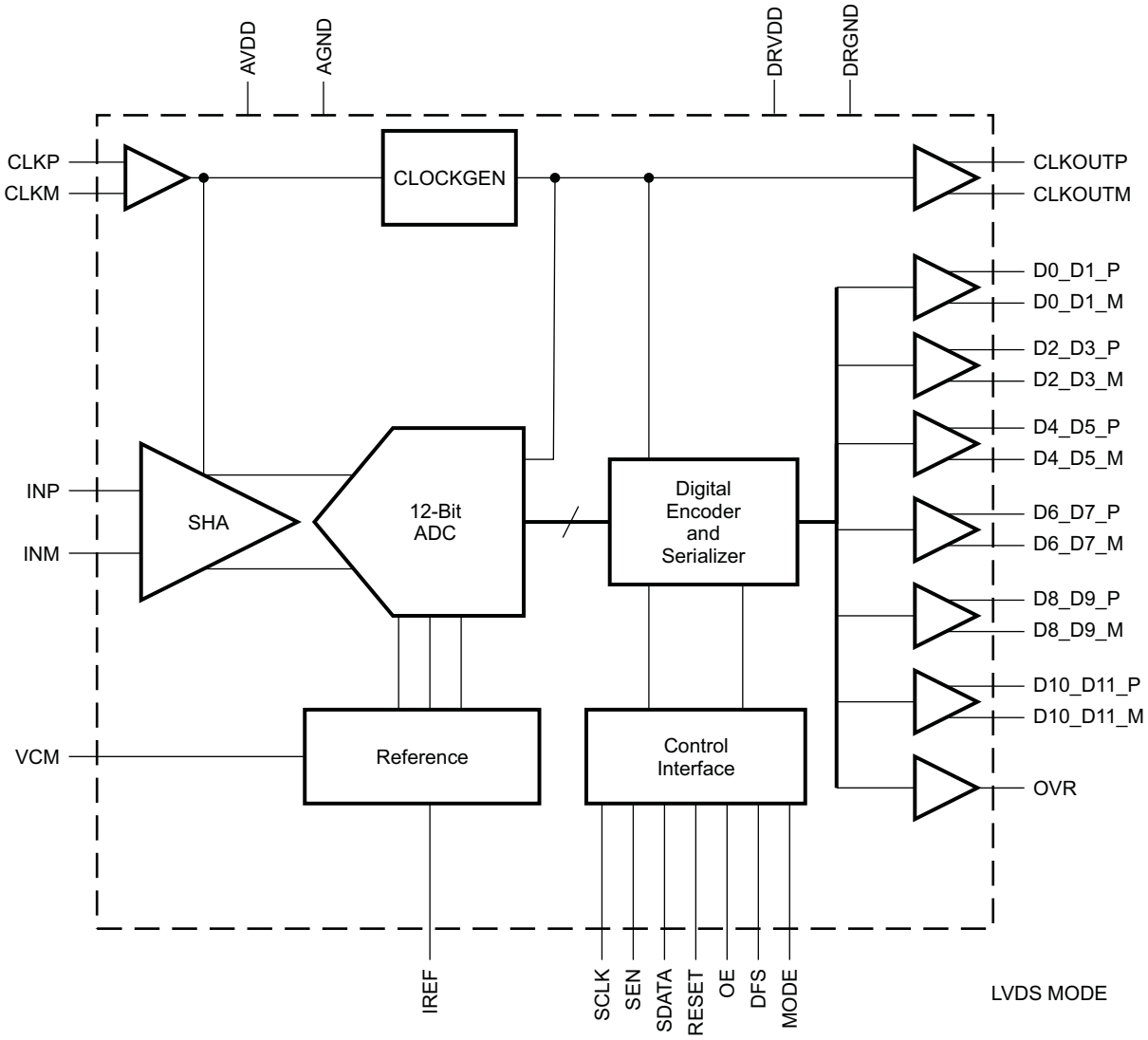
The device is specified over the industrial temperature range (-40°C to 85°C).

ADS5527 PRODUCT FAMILY

	210 MSPS	190 MSPS	170 MSPS
14 bit	ADS5547	ADS5546	ADS5545
12 bit	ADS5527	-	ADS5525

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5527	QFN-48(2)	RGZ	–40°C to 85°C	AZ5527	ADS5527IRGZT	Tape and Reel, 250
					ADS5527IRGZR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 25.41°C/W (0 LFM air flow), θ_{JC} = 16.5°C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in x 3 in (7.62 cm x 7.62 cm) PCB.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage range, AVDD	–0.3 V to 3.9	V
	Supply voltage range, DRVDD	–0.3 V to 3.9	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD	-0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	-0.3 to 1.8	V
	Voltage applied to analog input pins, INP and INM	–0.3 V to minimum (3.6, AVDD + 0.3 V)	V
	Voltage applied to input clock pins, CLKP and CLKM	-0.3 V to AVDD + 0.3 V	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
SUPPLIES					
	Analog supply voltage, AVDD	3	3.3	3.6	V
	Digital supply voltage, DRVDD	3	3.3	3.6	V
ANALOG INPUTS					
	Differential input voltage range		2		V_{PP}
	Input common-mode voltage		1.5 ±0.1		V
	Voltage applied on VCM in external reference mode	1.45	1.5	1.55	V
CLOCK INPUT					
	Input clock sample rate (1)				MSPS
	DEFAULT SPEED mode	50		210	MSPS
	LOW SPEED mode	1		60	
	Input clock amplitude differential ($V_{(CLKP)}$ - $V_{(CLKM)}$)				
	Sine wave, ac-coupled	0.4	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle (See Figure 31)	35%	50%	65%	
DIGITAL OUTPUTS					
C_L	Maximum external load capacitance from each output pin to DRGND (LVDS and CMOS modes)				
	Without internal termination (default after reset)		5		pF
	With 100 Ω internal termination (2)		10		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
	Operating free-air temperature	–40		85	°C

(1) See the section on *Low Sampling Frequency Operation* for more information.
(2) See the section on *LVDS Buffer Internal termination* for more information.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-db gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		bits
ANALOG INPUT						
	Differential input voltage range			2		V_{PP}
	Differential input capacitance			7		pF
	Analog input bandwidth			800		MHz
	Analog input common mode current (per input pin)			342		µA
REFERENCE VOLTAGES						
$V_{(REFB)}$	Internal reference bottom voltage	Internal reference mode		0.5		V
$V_{(REFT)}$	Internal reference top voltage	Internal reference mode		2.5		V
$\Delta V_{(REF)}$	Internal reference error	$V_{(REFT)}$ - $V_{(REFB)}$	-60	±25	60	mV
V_{CM}	Common mode output voltage	Internal reference mode		1.5		V
	VCM output current capability	Internal reference mode		±4		mA
DC ACCURACY						
	No Missing Codes			Assured		
DNL	Differential non-linearity		-0.8	0.5	1.0	LSB
INL	Integral non-linearity		-2	1	2	LSB
	Offset error		-10	5	10	mV
	Offset temperature coefficient			0.002		ppm/°C
	Gain error due to internal reference error alone	($\Delta V_{(REF)}$ / 2.0V)%	-3	±1	3	%FS
	Gain error excluding internal reference error(1)		-2	± 1	2	%FS
	Gain temperature coefficient			0.01		Δ%/°C
PSRR	DC Power supply rejection ratio			0.6		mV/V
POWER SUPPLY						
$I_{(AVDD)}$	Analog supply current			306		mA
$I_{(DRVDD)}$	Digital supply current	LVDS mode, I_O = 3.5 mA, R_L = 100 Ω, C_L = 5 pF		66		mA
		CMOS mode, F_{IN} = 2.5 MHz, C_L = 5 pF		47		mA
I_{CC}	Total supply current	LVDS mode		372		mA
	Total power dissipation	LVDS mode		1.23	1.375	W
	Standby power	In STANDBY mode with clock stopped		100	150	mW
	Clock stop power	With input clock stopped		100	150	mW

(1) Gain error is specified from design and characterization; it is not tested in production.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-db gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC CHARACTERISTICS							
SNR	Signal to noise ratio	F_{IN} = 20 MHz			70.7		dBFS
		F_{IN} = 70 MHz		68	70.5		
		F_{IN} = 100 MHz			70.3		
		F_{IN} = 170 MHz			69.5		
		F_{IN} = 230 MHz	0 dB gain, 2 V_{PP} FS(1)		69.4		
			3 dB gain, 1.4 V_{PP} FS		68		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		68.5		
			3 dB gain, 1.4 V_{PP} FS		67.4		
		F_{IN} = 400 MHz	0 dB gain, 2 V_{PP} FS		67.3		
			3 dB gain, 1.4 V_{PP} FS		66.4		
	RMS output noise	Inputs tied to common-mode			0.35		LSB
SFDR	Spurious free dynamic range	F_{IN} = 20 MHz			86		dBc
		F_{IN} = 70 MHz		75	84		
		F_{IN} = 100 MHz			78		
		F_{IN} = 170 MHz			79		
		F_{IN} = 230 MHz	0 dB gain, 2 V_{PP} FS		75		
			3 dB gain, 1.4 V_{PP} FS		78		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		74		
			3 dB gain, 1.4 V_{PP} FS		76		
		F_{IN} = 400 MHz	0 dB gain, 2 V_{PP} FS		68		
			3 dB gain, 1.4 V_{PP} FS		70		
SINAD	Signal to noise and distortion ratio	F_{IN} = 20 MHz			70.5		dBFS
		F_{IN} = 70 MHz		67.5	70.2		
		F_{IN} = 100 MHz			69.3		
		F_{IN} = 170 MHz			68.0		
		F_{IN} = 230 MHz	0 dB gain, 2 V_{PP} FS		67.4		
			3 dB gain, 1.4 V_{PP} FS		67.1		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		66.4		
			3 dB gain, 1.4 V_{PP} FS		66.3		
		F_{IN} = 400 MHz	0 dB gain, 2 V_{PP} FS		63.5		
			3 dB gain, 1.4 V_{PP} FS		65.0		
HD2	Second harmonic	F_{IN} = 20 MHz			91		dBc
		F_{IN} = 70 MHz		75	88		
		F_{IN} = 100 MHz			87		
		F_{IN} = 170 MHz			87		
		F_{IN} = 230 MHz	0 dB gain, 2 V_{PP} FS		86		
			3 dB gain, 1.4 V_{PP} FS		88		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		78		
			3 dB gain, 1.4 V_{PP} FS		80		
		F_{IN} = 400 MHz	0 dB gain, 2 V_{PP} FS		69		
			3 dB gain, 1.4 V_{PP} FS		71		

(1) FS = Full scale range

ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0-db gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD3	Third harmonic	F_{IN} = 20 MHz			86		dBc
		F_{IN} = 70 MHz		75	84		
		F_{IN} = 100 MHz			78		
		F_{IN} = 170 MHz			79		
		F_{IN} = 230 MHz	0 dB gain, 2 V_{PP} FS		75		
			3 dB gain, 1.4 V_{PP} FS		78		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		74		
			3 dB gain, 1.4 V_{PP} FS		76		
		F_{IN} = 400 MHz	0 dB gain, 2 V_{PP} FS		68		
			3 dB gain, 1.4 V_{PP} FS		70		
Worst harmonic (other than HD2, HD3)		F_{IN} = 20 MHz			95		dBc
		F_{IN} = 70 MHz			92		
		F_{IN} = 100 MHz			92		
		F_{IN} = 170 MHz			90		
		F_{IN} = 230 MHz			90		
		F_{IN} = 300 MHz			88		
		F_{IN} = 400 MHz			87		
THD	Total harmonic distortion	F_{IN} = 20 MHz			83		dBc
		F_{IN} = 70 MHz		73	82		
		F_{IN} = 100 MHz			76		
		F_{IN} = 170 MHz			77		
		F_{IN} = 230 MHz			73		
		F_{IN} = 300 MHz			72		
		F_{IN} = 400 MHz			65		
ENOB	Effective number of bits	F_{IN} = 70 MHz		10.9	11.4		bits
IMD	Two-tone intermodulation distortion	F_{IN1} = 50.03 MHz, F_{IN2} = 46.03 MHz, -7 dBFS each tone			91		dBFS
		F_{IN1} = 190.1 MHz, F_{IN2} = 185.02 MHz, -7 dBFS each tone			86		
PSRR	AC power supply rejection ratio	30 MHz, 200 mV_{PP} signal on 3.3-V supply			35		dBc
	Voltage overload recovery time	Recovery to 1% (of final value) for 6-dB overload with sine-wave input at Nyquist frequency			1		Clock cycles

DIGITAL CHARACTERISTICS[1]

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = DRVDD = 3.3 V, I_O = 3.5 mA, R_L = 100 Ω[2]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS – CMOS MODE					
High-level output voltage			3.3		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from each output to ground		2		pF
DIGITAL OUTPUTS – LVDS MODE					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$		225	350	425	mV
V_{OS} Output offset voltage, single-ended	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) All LVDS and CMOS specifications are characterized, but not tested at production.
(2) I_O refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

TIMING CHARACTERISTICS – LVDS AND CMOS MODES[1]

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF[2], I_O = 3.5 mA, R_L = 100 Ω[3], no internal termination, unless otherwise noted.

For timings at lower sampling frequencies, see the *Output Timing* section in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			1.2		ns
t_j	Aperture jitter			150		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode			100	µs
		Time to valid data after stopping and restarting the input clock			100	
	Latency			14		clock cycles
DDR LVDS MODE[4]						
t_{su}	Data setup time[5]	Data valid [6] to zero-cross of CLKOUTP	1.0	1.5		ns
t_h	Data hold time[5]	Zero-cross of CLKOUTP to data becoming invalid[6]	0.35	0.8		ns

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_L is the effective external single-ended load capacitance between each output pin and ground.
(3) I_O refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
(6) Data valid refers to logic high of +50 mV and logic low of –50 mV.

TIMING CHARACTERISTICS – LVDS AND CMOS MODES (continued)

For timings at lower sampling frequencies, see the *Output Timing* section in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDI}	Clock propagation delay(7)	Input clock rising edge zero-cross to output clock rising edge zero-cross	3.7	4.4	5.1	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 80 ≤ Fs ≤ 210 MSPS	45%	50%	55%	
t_r , t_f	Data rise time, Data fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 210 MSPS	50	100	200	ps
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 210 MSPS	50	100	200	ps
	Output clock jitter	Cycle-to-cycle jitter		120		ps pp
t_{OE}	Output enable (OE) to valid data delay	Time to valid data after OE becomes active			1	µs
PARALLEL CMOS MODE						
t_{su}	Data setup time (5)	Data valid(8) to 50% of CLKOUT rising edge	1.8	2.6		ns
t_h	Data hold time (9)	50% of CLKOUT rising edge to data becoming invalid(10)	0.4	0.8		ns
t_{PDI}	Clock propagation delay(11)	Input clock rising edge zero-cross to 50% of CLKOUT rising edge	2.6	3.4	4.2	ns
	Output clock duty cycle	Duty cycle of output clock (CLKOUT) 80 ≤ Fs ≤ 210 MSPS		45%		
t_r , t_f	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 210 MSPS	0.8	1.5	2.0	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 210 MSPS	0.4	0.8	1.2	ns
t_{OE}	Output enable (OE) to valid data delay	Time to valid data after OE becomes active			50	ns

(7) To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay (t_D) to get the desired setup and hold times. Use either of these equations to calculate t_D:
Desired setup time = t_D - (t_{PDI} - t_{su})
Desired hold time = (t_{PDI} + t_h) - t_D

(8) Data valid refers to logic high of 2 V and logic low of 0.8 V

(9) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.

(10) Data valid refers to logic high of 2 V and logic low of 0.8 V

(11) To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay (t_D) to get the desired setup and hold times. Use either of these equations to calculate t_D:
Desired setup time = t_D - (t_{PDI} - t_{su})
Desired hold time = (t_{PDI} + t_h) - t_D

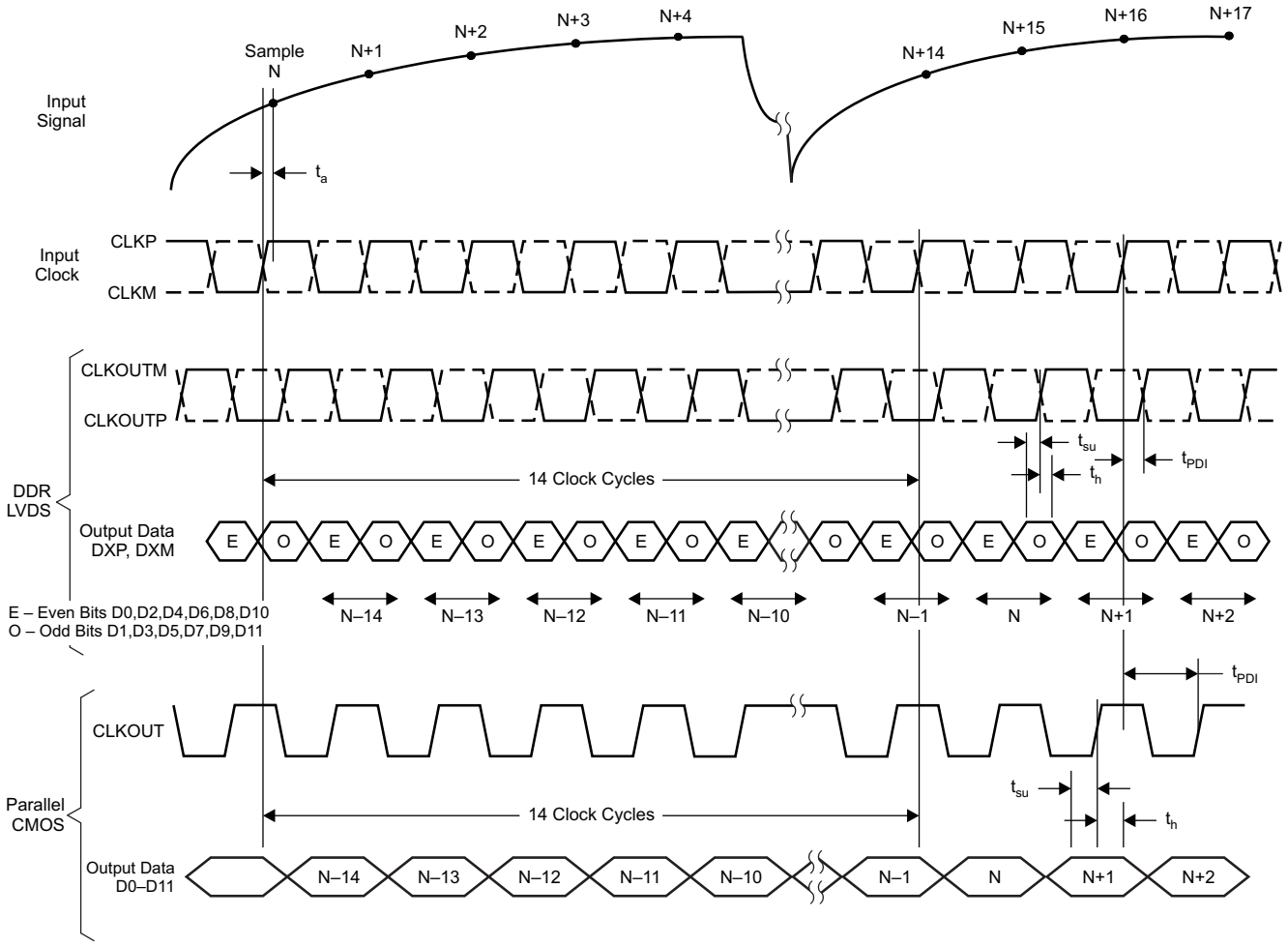
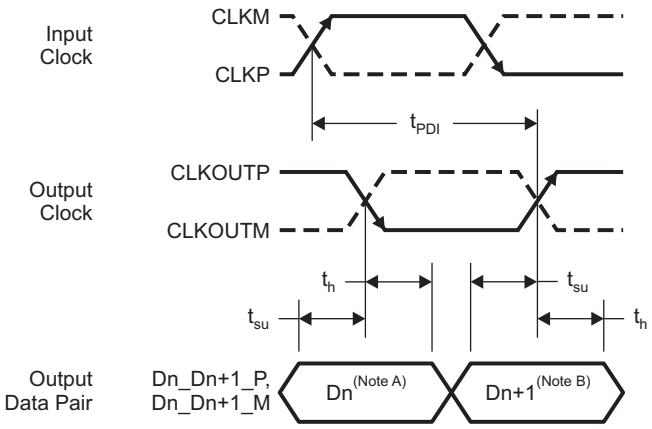


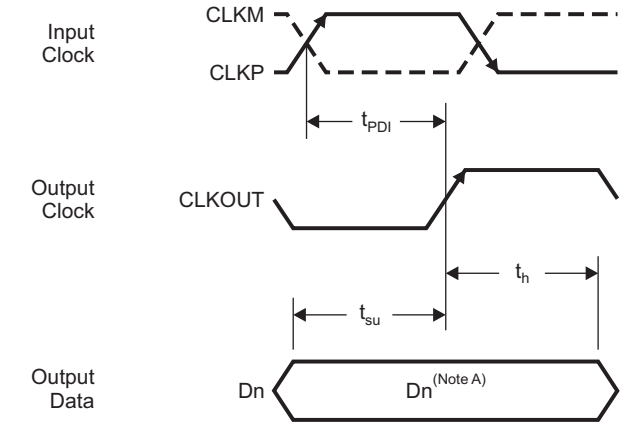
Figure 1. Latency



A. Dn – Bits D0, D2, D4, D6, D8, and D10

B. Dn+1 – Bits D1, D3, D5, D7, D9, and D11

Figure 2. LVDS Mode Timing



A. Dn – Bits D0–D11

Figure 3. CMOS Mode Timing

DEVICE PROGRAMMING MODES

ADS5527 offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either parallel interface control or serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table (Table 2). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to **high** (DRVDD). Pins DFS, MODE, SEN, SCLK, and SDATA are used to directly control certain modes of the ADC. The device is configured by connecting the parallel pins to the correct voltage levels (as described in Table 3 to Table 7). There is no need to apply reset.

In this mode, SEN, SCLK, and SDATA function as parallel interface control pins. Frequently used functions are controlled in this mode—standby, selection between LVDS/CMOS output format, internal/external reference, two's complement/straight binary output format, and position of the output clock edge.

Table 1 has a description of the modes controlled by the four parallel pins.

Table 1. Parallel Pin Definition

PIN	CONTROL MODES
DFS	DATA FORMAT and the LVDS/CMOS output interface
MODE	Internal or external reference
SEN	CLKOUT edge programmability
SCLK	LOW SPEED mode control for low sampling frequencies (< 50 MSPS)
SDATA	STANDBY mode – Global (ADC, internal references and output buffers are powered down)

USING SERIAL INTERFACE PROGRAMMING ONLY

To program using the serial interface, the internal registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on the RESET pin, or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

Since the parallel pins DFS and MODE are not used in this mode, they must be tied to ground.

USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (DFS, MODE) can also be used to configure the device.

The serial registers must first be reset to their default values and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

The parallel interface control pins DFS and MODE are used and their function is determined by the appropriate voltage levels as described in Table 6 and Table 7. The voltage levels are derived by using a resistor string as illustrated in Figure 4. Since some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table (Table 2).

Table 2. Priority Between Parallel Pins and Serial Registers

PIN	FUNCTIONS SUPPORTED	PRIORITY
MODE	Internal/External reference	When using the serial interface, bit <REF> (register 0x6D, bit D4) controls this mode, ONLY if the MODE pin is tied low.
DFS	DATA FORMAT	When using the serial interface, bit <DF> (register 0x63, bit D3) controls this mode, ONLY if the DFS pin is tied low.
	LVDS/CMOS	When using the serial interface, bit <ODI> (register 0x6C, bits D3-D4) controls LVDS/CMOS selection independent of the state of DFS pin

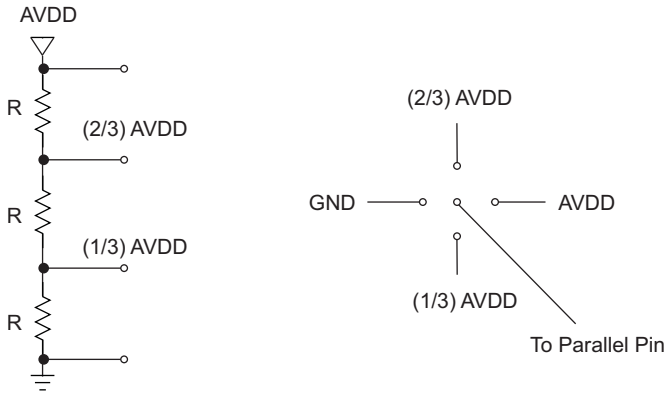


Figure 4. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS

Table 3. SCLK Control Pin

SCLK (Pin 29)	DESCRIPTION
0	LOW SPEED mode Disabled - Use for sampling frequencies above 50 MSPS.
DRVDD	LOW SPEED mode Enabled - Use for sampling frequencies below 50 MSPS.

Table 4. SDATA Control Pin

SDATA (Pin 28)	DESCRIPTION
0	Normal operation (Default)
DRVDD	STANDBY. This is a global power down, where ADC, internal references and the output buffers are powered down.

Table 5. SEN Control Pin

SEN (Pin 27)	DESCRIPTION
0	**CMOS mode**: CLKOUT edge later by (3/12)Ts (1); **LVDS mode**: CLKOUT edge aligned with data transition
(1/3)DRVDD	**CMOS mode**: CLKOUT edge later by (2/12)Ts ; **LVDS mode**: CLKOUT edge aligned with data transition
(2/3)DRVDD	**CMOS mode**: CLKOUT edge later by (1/12)Ts ; **LVDS mode**: CLKOUT edge earlier by (1/12)Ts
DRVDD	Default CLKOUT position

(1) Ts = 1/Sampling Frequency

Table 6. DFS Control Pin

DFS (Pin 6)	DESCRIPTION
0	2's complement data and DDR LVDS output (Default)
(1/3)DRVDD	2's complement data and parallel CMOS output
(2/3)DRVDD	Offset binary data and parallel CMOS output
DRVDD	Offset binary data and DDR LVDS output

Table 7. MODE Control Pin

MODE (Pin 23)	DESCRIPTION
0	Internal reference
(1/3)AVDD	External reference
(2/3)AVDD	External reference
AVDD	Internal reference

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits form the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 5.

   OR

2. By applying software reset. Using the serial interface, set the <RST> bit (D1 in register 0x6C) to **high**. This initializes the internal registers to their default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

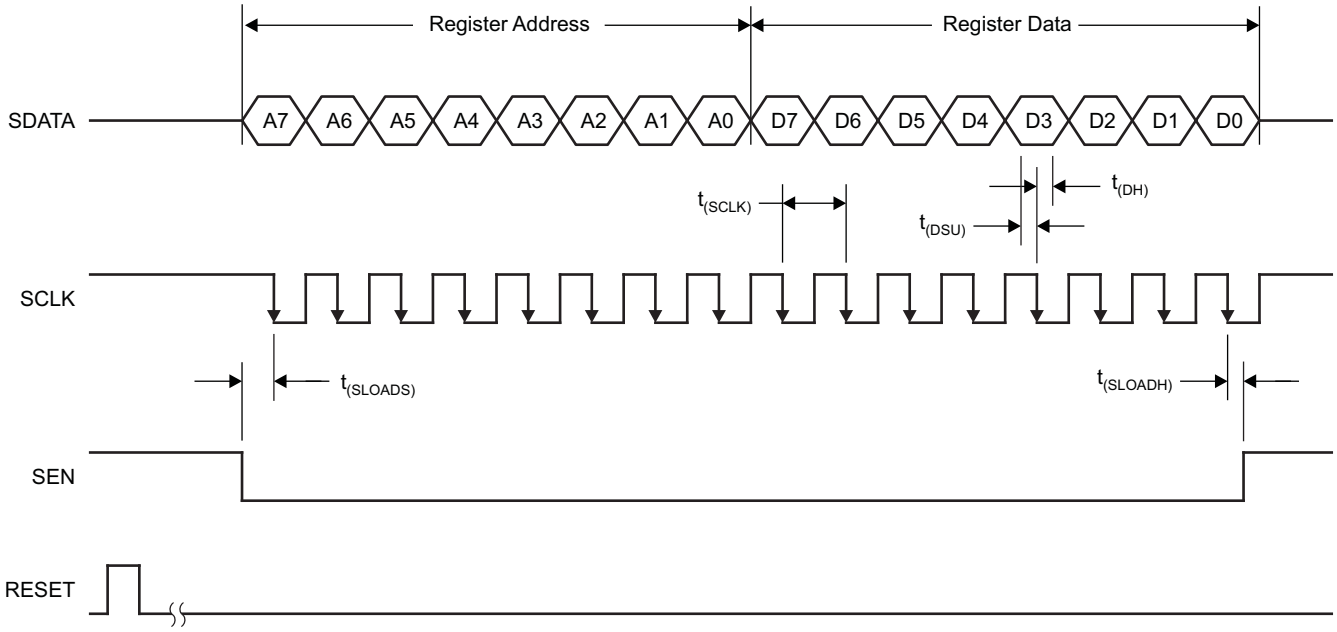


Figure 5. Serial Interface Timing Diagram

SERIAL INTERFACE TIMING CHARACTERISTICS

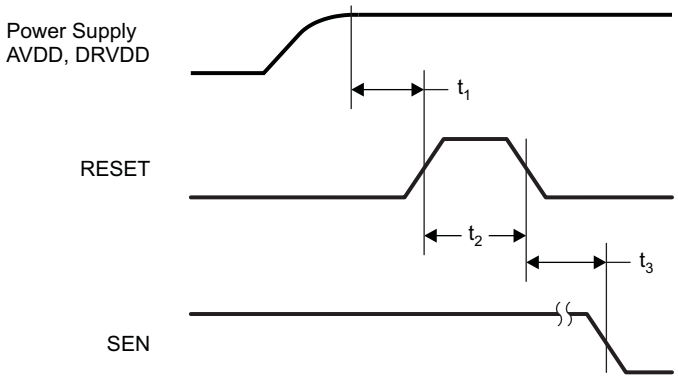
Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time		25		ns
t_{SLOADH}	SCLK to SEN hold time		25		ns
t_{DSU}	SDATA setup time		25		ns
t_{DH}	SDATA hold time		25		ns

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		6.5		ms



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 6. Reset Timing Diagram

SERIAL REGISTER MAP

Table 8 gives a summary of all the modes that can be programmed through the serial interface.

Table 8. Summary of Functions Supported by Serial Interface (1)(2)

REGISTER ADDRESS IN HEX	REGISTER FUNCTIONS							
A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
62		**<DATA POSN>** OUTPUT DATA POSITION PROGRAMMABILITY		**<CLKOUT POSN>** OUTPUT CLOCK POSITION PROGRAMMABILITY				
63	**<STBY>** GLOBAL POWER DOWN			**<LOW SPEED>** ENABLE LOW SAMPLING FREQUENCY OPERATION	**<DF>** DATA FORMAT - 2's COMP or STRAIGHT BINARY			
65	**<TEST PATTERN>** – ALL 0S, ALL 1s, TOGGLE, RAMP, CUSTOM PATTERN							
68					**<GAIN>** GAIN PROGRAMMING <GAIN> - 1 dB to 6 dB			
69	**<CUSTOM A>** CUSTOM PATTERN (D7 TO D0)							
6A			**<CUSTOM B>** CUSTOM PATTERN (D13 TO D8)					
6B			**<CLKIN GAIN>** INPUT CLOCK BUFFER GAIN PROGRAMMABILITY					
6C				**<ODI>** OUTPUT DATA INTERFACE - DDR LVDS or PARALLEL CMOS			**<RST>** SOFTWARE RESET	
6D	**<SCALING>** POWER SCALING			**<REF>** INTERNAL or EXTERNAL REFERENCE				
7E	**<DATA TERM>** INTERNAL TERMINATION – DATA OUTPUTS			**<CLKOUT TERM>** INTERNAL TERMINATION – OUTPUT CLOCK			**<LVDS CURR>** LVDS CURRENT PROGRAMMABILITY	
7F	**<CURR DOUBLE>** LVDS CURRENT DOUBLE							

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as '0'.
(2) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

Each register function is explained in detail below.

Table 9. Serial Register A

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
62		**<DATA POSN>** OUTPUT DATA POSITION PROGRAMMABILITY		**<CLKOUT POSN>** OUTPUT CLOCK POSITION PROGRAMMABILITY				

D4 - D0	**<CLKOUT POSN> Output clock position programmability**
00001	Default CLKOUT position after reset. Setup/hold timings with this clock position are specified in the timing characteristics table.
XX011	**CMOS** – Rising edge later by (1/12) Ts
	LVDS – Rising edge earlier by (1/12) Ts
XX101	**CMOS** – Rising edge later by (3/12) Ts
	LVDS – Rising edge aligned with data transition
XX111	**CMOS** – Rising edge later by (2/12) Ts
	LVDS – Rising edge aligned with data transition
01XX1	**CMOS** – Rising edge later by (1/12) Ts
	LVDS – Rising edge earlier by (1/12) Ts
10XX1	**CMOS** – Rising edge later by (3/12) Ts
	LVDS – Rising edge aligned with data transition
11XX1	**CMOS** – Rising edge later by (2/12) Ts
	LVDS – Rising edge aligned with data transition

D6 – D5	**<DATA POSN> Output Switching Noise and Data Position Programmability (in CMOS mode ONLY) (Only in CMOS mode)**
00	Data Position 1 - Default output data position after reset. Setup/hold timings with this data position are specified in the timing characteristics table.
01	Data Position 2 - Setup time increases by (2/36) Ts
10	Data Position 3 - Setup time increases by (5/36) Ts
11	Data Position 4 - Setup time decreases by (6/36) Ts

Table 10. Serial Register B

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
63	**<STBY>** GLOBAL POWER DOWN			**<LOW SPEED>** ENABLE LOW SAMPLING FREQUENCY OPERATION	**<DF>** DATA FORMAT 2's COMP or STRAIGHT BINARY			

D3	<DF> Output data format
0	2's complement
1	Straight binary

D4	<LOW SPEED> Low sampling frequency operation
0	Default SPEED mode for 50 < Fs ≤ 190 MSPS
1	Low SPEED mode 1≤ Fs ≤ 50 MSPS

D7	<STBY> Global power down
0	Normal operation
1	Global power down (includes ADC, internal references and output buffers)

Table 11. Serial Register C

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
65	**<TEST PATTERNS>**— ALL 0S, ALL 1s, TOGGLE, RAMP, CUSTOM PATTERN							

D7 - D5	<TEST PATTERN> Outputs selected test pattern on data lines
000	Normal operation
001	All 0s
010	All 1s
011	Toggle pattern – alternate 1s and 0s on each data output and across data outputs
100	Ramp pattern – Output data ramps from 0x0000 to 0x3FFF by one code every clock cycle
101	Custom pattern – Outputs the custom pattern in CUSTOM PATTERN registers A and B
111	Unused

Table 12. Serial Register D

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
68					**<GAIN>** GAIN PROGRAMMING <GAIN> - 1 dB to 6 dB			

D3 - D0	<GAIN> Gain programmability
1000	0 dB gain, default after reset
1001	1 dB
1010	2 dB
1011	3 dB
1100	4 dB
1101	5 dB
1110	6 dB

Table 13. Serial Register E

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
69	**<CUSTOM A>** CUSTOM PATTERN (D7 TO D0)							
6A			**<CUSTOM B>** CUSTOM PATTERN (D13 TO D8)					

Reg 69	D7 – D0	Program bits D7 to D0 of custom pattern
Reg 6A	D5 – D0	Program bits D13 to D8 of custom pattern

Table 14. Serial Register F

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
6B			**<CLKIN GAIN>** INPUT CLOCK BUFFER GAIN PROGRAMMABILITY					

D5 - D0	<CLKIN GAIN> Input clock buffer gain programming
110010	Gain 4, maximum gain
101010	Gain 3
100110	Gain 2
100000	Gain1, default after reset
100011	Gain 0 minimum gain

Table 15. Serial Register G

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
6C				**<ODI>** OUTPUT DATA INTERFACE - DDR LVDS OR PARALLEL CMOS			**<RST>** SOFTWARE RESET	

D1	<RST> Software resets the ADC
1	Resets all registers to default values

D4 - D3	<ODI> Output data interface
00	DDR LVDS outputs, default after reset
01	DDR LVDS outputs
11	Parallel CMOS outputs

Table 16. Serial Register H

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
6D	**<SCALING>** POWER SCALING			**<REF>** INTERNAL or EXTERNAL REFERENCE				

D4	<REF> Reference
0	Internal reference
1	External reference mode, force voltage on Vcm to set reference.

D7 - D5	<SCALING> Program power scaling at lower sampling frequencies
001	Use for Fs > 150 MSPS, default after reset
011	Power Mode 1, use for 105 < Fs ≤ 150 MSPS
101	Power Mode 2, use for 50 < Fs ≤ 105
111	Power Mode 3, use for Fs ≤ 50 MSPS

Table 17. Serial Register I

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
7E	**<DATA TERM>** INTERNAL TERMINATION – DATA OUTPUTS			**<CLKOUT TERM>** INTERNAL TERMINATION – OUTPUT CLOCK			**<LVDS CURR>** LVDS CURRENT PROGRAMMABILITY	

D1 - D0	<LVDS CURR> LVDS buffer current programming
00	3.5 mA, default
01	2.5 mA
10	4.5 mA
11	1.75 mA

D4 - D2	<CLKOUT TERM> LVDS internal termination for output clock pin (CLKOUT)
000	No internal termination
001	325
010	200
011	125
100	170
101	120
110	100
111	75

D7 - D5	<DATA TERM> LVDS internal termination for output data pins
000	No internal termination
001	325
010	200
011	125
100	170
101	120
110	100
111	75

Table 18. Serial Register J

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
7F	**<CURR DOUBLE>** LVDS CURRENT DOUBLE							

D7 - D6	<CURR DOUBLE> LVDS buffer current double
00	Value specified by <LVDS CURR>
01	2x data, 2x clockout currents
10	1x data, 2x clockout currents
11	2x data, 4x clockout currents

PIN CONFIGURATION (LVDS MODE)

RGZ PACKAGE
(TOP VIEW)

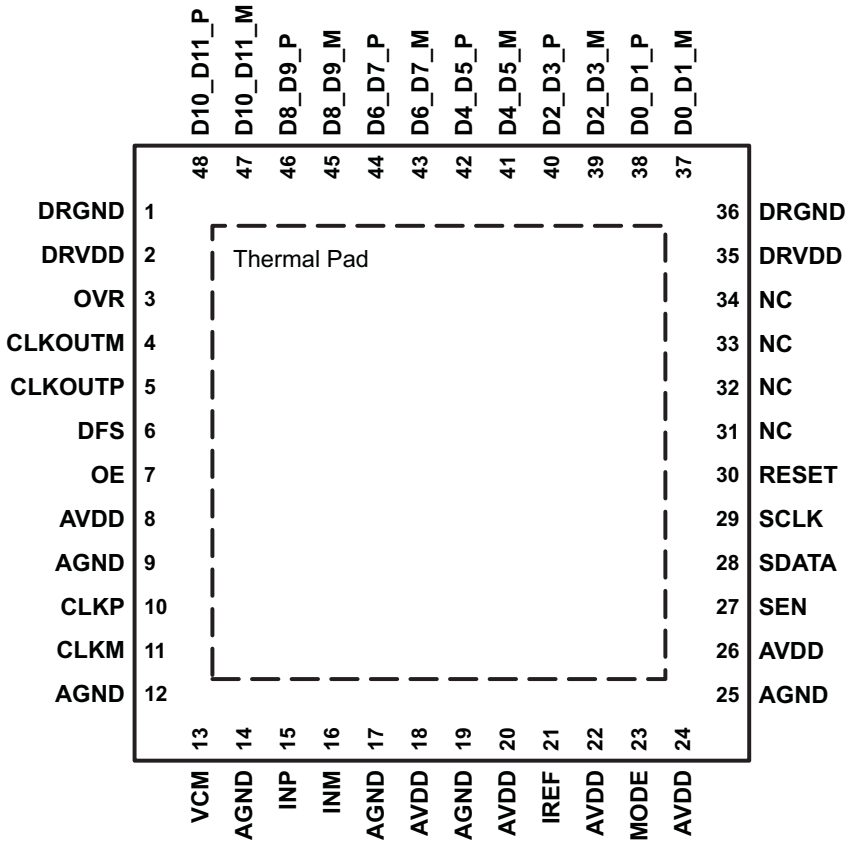


Figure 7. LVDS Mode Pinout

PIN ASSIGNMENTS – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100-kΩ pull-down resistor.	I	30	1

PIN CONFIGURATION (LVDS MODE) (continued)

PIN ASSIGNMENTS – LVDS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as LOW SPEED control pin when RESET is tied high. Tie SCLK to LOW for Fs > 50 MSPS and SCLK to HIGH for Fs ≤ 50 MSPS. See Table 3. The pin has an internal 100-kΩ pull-down resistor.	I	29	1
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 5 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 6 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the Internal or External reference mode. See Table 7 for detailed information.	I	23	1
CLKOUTP	Differential output clock, true	O	5	1
CLKOUTM	Differential output clock, complement	O	4	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	38	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	37	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	40	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	39	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	42	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	41	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	44	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	43	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	46	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	45	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	48	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	47	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
NC	Do not connect		31, 32, 33, 34	4
PAD	Connect the pad to the ground plane. See *Board Design Considerations* in application information section.		0	1

PIN CONFIGURATION (CMOS MODE)

RGZ PACKAGE
(TOP VIEW)

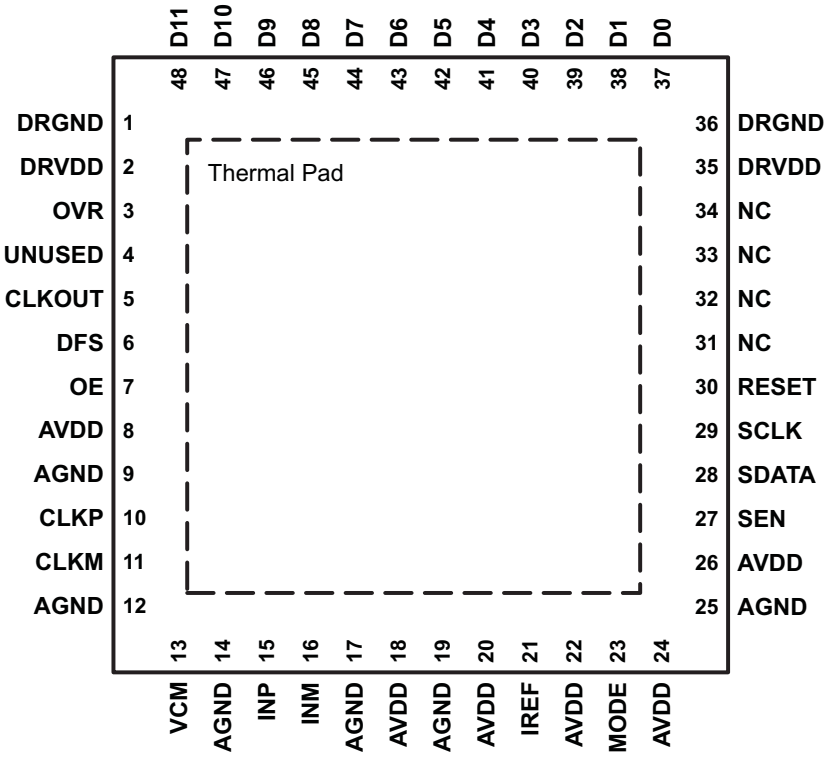


Figure 8. CMOS Mode Pinout

PIN ASSIGNMENTS – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode). The pin has an internal 100-kΩ pull-down resistor.	I	30	1
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as LOW SPEED control pin when RESET is tied high. Tie SCLK to LOW for Fs > 50 MSPS and SCLK to HIGH for Fs ≤ 50 MSPS. See Table 3. The pin has an internal 100-kΩ pull-down resistor.	I	29	1

PIN CONFIGURATION (CMOS MODE) (continued)

PIN ASSIGNMENTS – CMOS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 5 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 6 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the internal or external reference mode. See Table 7 for detailed information.	I	23	1
CLKOUT	CMOS output clock	O	5	1
D0	CMOS output data D0	O	37	1
D1	CMOS output data D1	O	38	1
D2	CMOS output data D2	O	39	1
D3	CMOS output data D3	O	40	1
D4	CMOS output data D4	O	41	1
D4	CMOS output data D5	O	42	1
D6	CMOS output data D6	O	43	1
D7	CMOS output data D7	O	44	1
D8	CMOS output data D8	O	45	1
D9	CMOS output data D9	O	46	1
D10	CMOS output data D10	O	47	1
D11	CMOS output data D11	O	48	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
UNUSED	Unused pin in CMOS mode		4	1
NC	Do not connect		31, 32, 33, 34	4
PAD	Connect the pad to the ground plane. See *Board Design Considerations* in application information section.		0	1

TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

FFT for 30 MHz INPUT SIGNAL

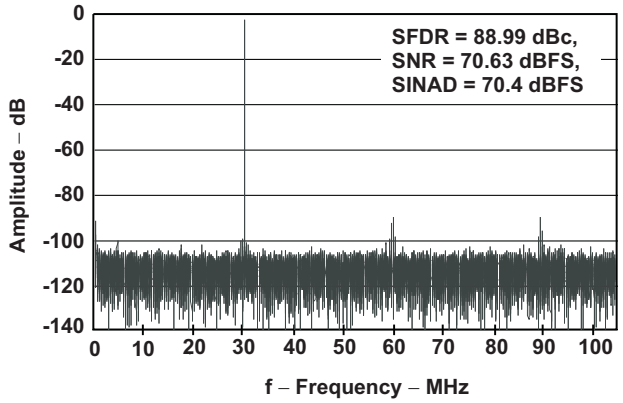


Figure 9.

FFT for 70 MHz INPUT SIGNAL

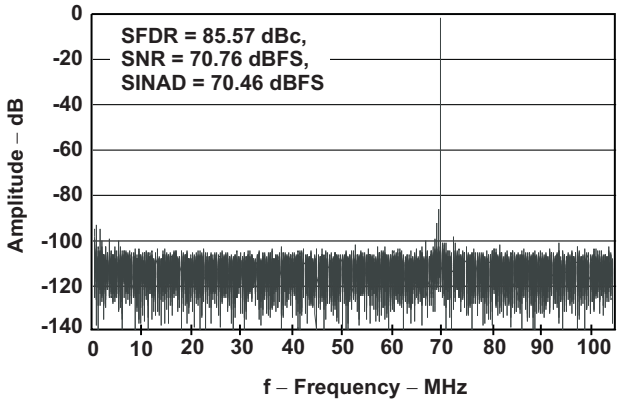


Figure 10.

FFT for 100 MHz INPUT SIGNAL

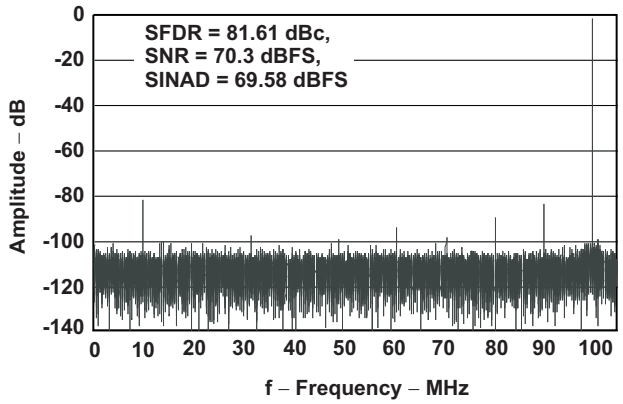


Figure 11.

FFT for 170 MHz INPUT SIGNAL

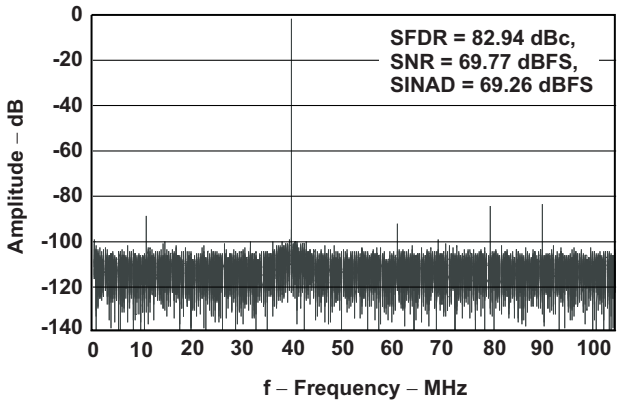


Figure 12.

FFT for 220 MHz INPUT SIGNAL

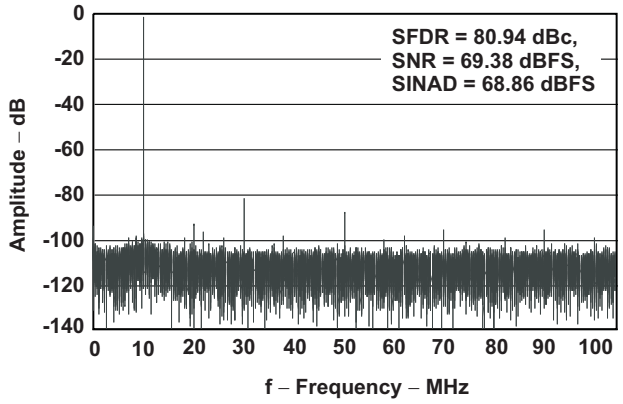


Figure 13.

FFT for 300 MHz INPUT SIGNAL

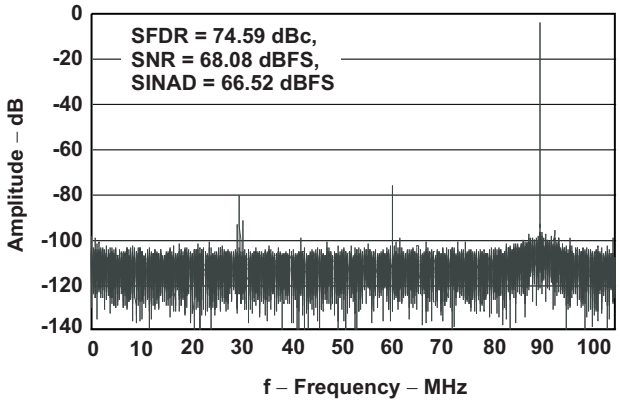


Figure 14.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

FFT for 400 MHz INPUT SIGNAL

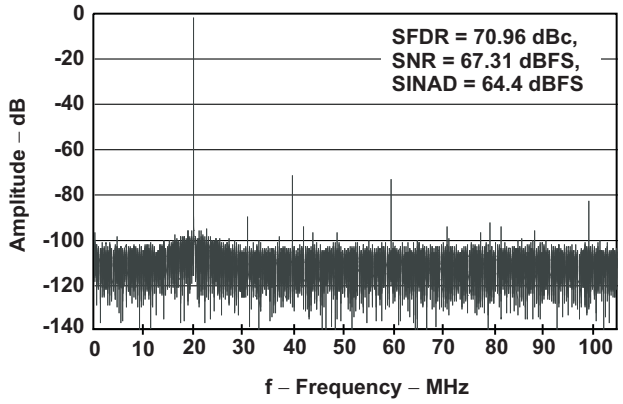


Figure 15.

FFT for 600 MHz INPUT SIGNAL

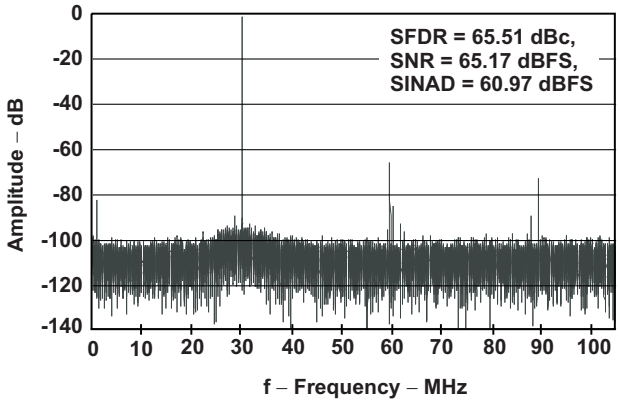


Figure 16.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

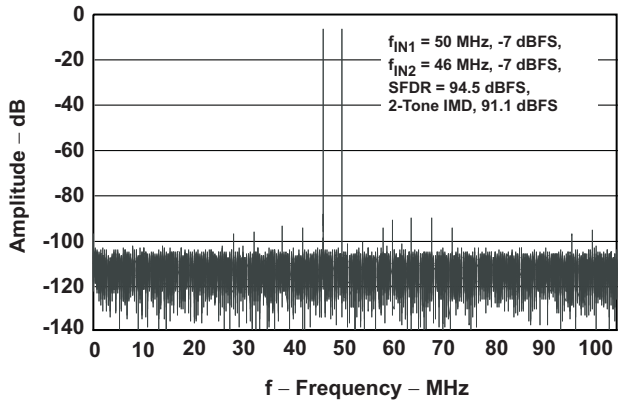


Figure 17.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

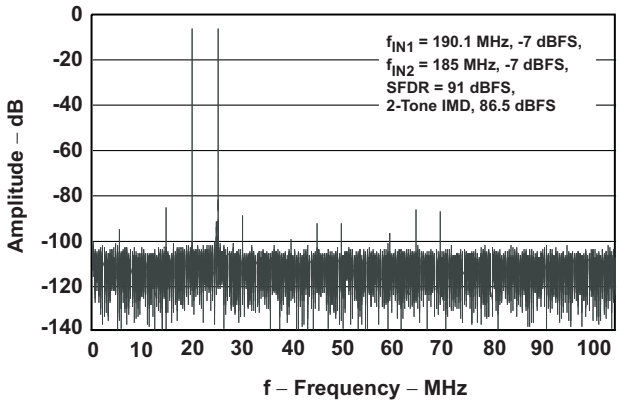


Figure 18.

SFDR vs INPUT FREQUENCY

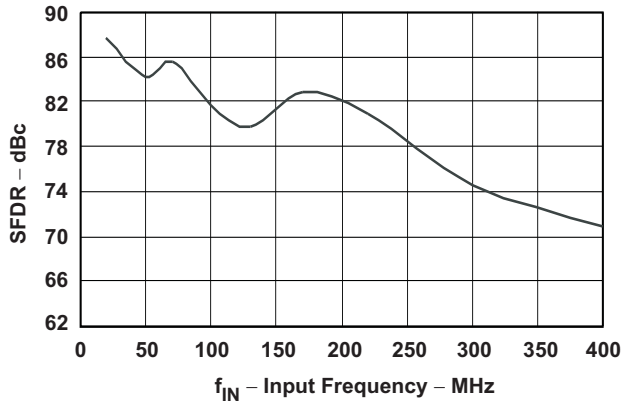


Figure 19.

SNR vs INPUT FREQUENCY

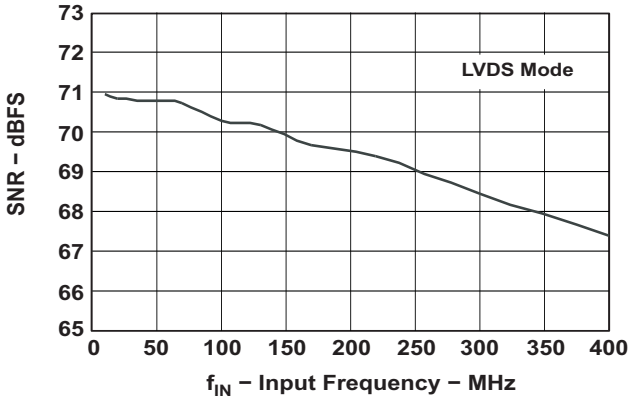


Figure 20.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

SNR vs INPUT FREQUENCY

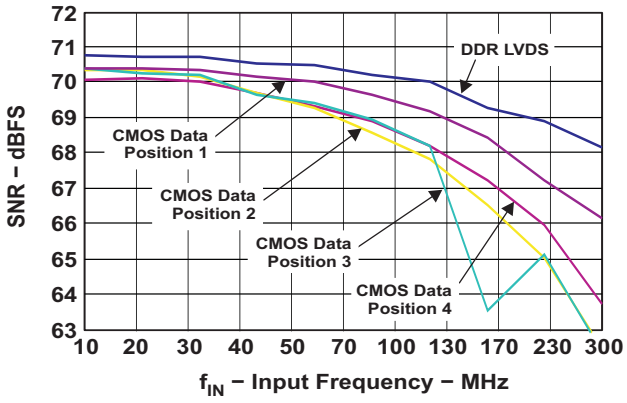


Figure 21.

SFDR vs GAIN

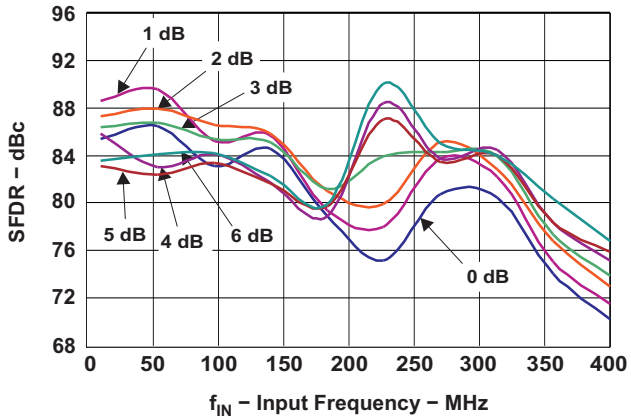


Figure 22.

SNR vs GAIN

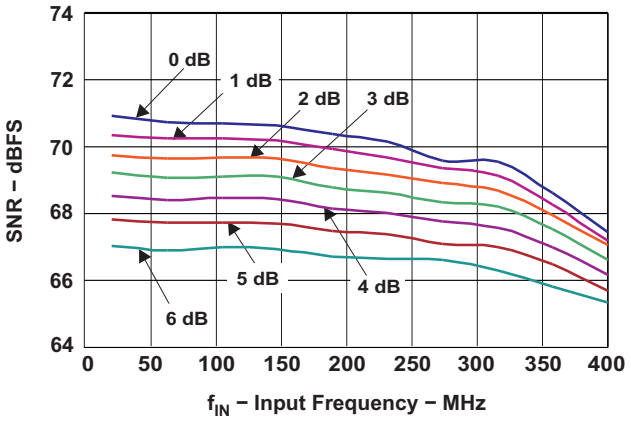


Figure 23.

PERFORMANCE vs AVDD

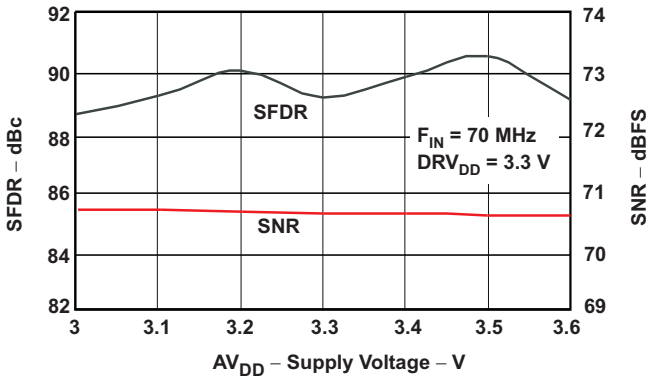


Figure 24.

PERFORMANCE vs DRVDD

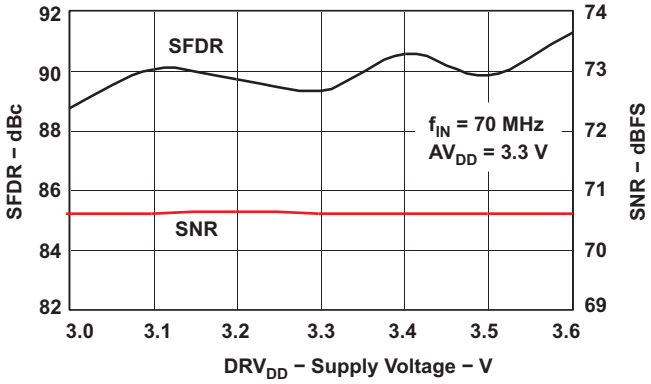


Figure 25.

PERFORMANCE vs TEMPERATURE

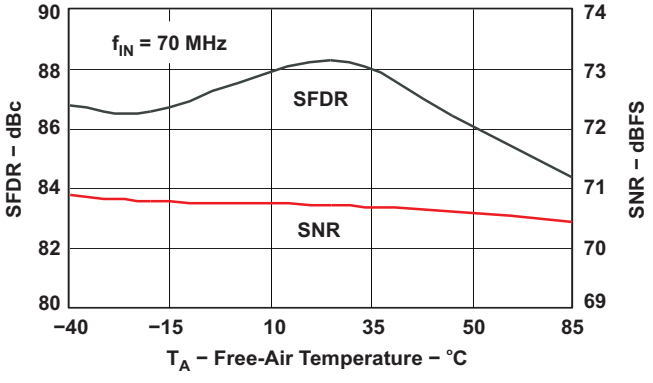


Figure 26.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

SNR vs SAMPLING FREQUENCY ACROSS POWER SCALING MODES

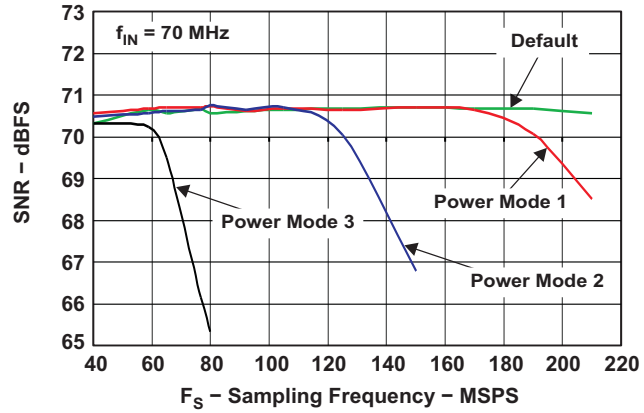


Figure 27.

POWER DISSIPATION vs SAMPLING FREQUENCY

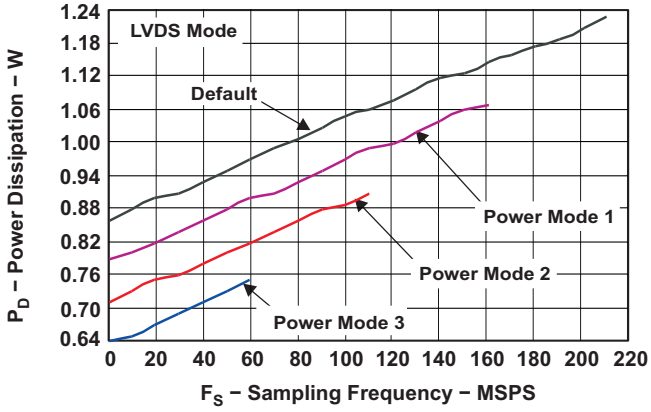


Figure 28.

PERFORMANCE vs INPUT AMPLITUDE

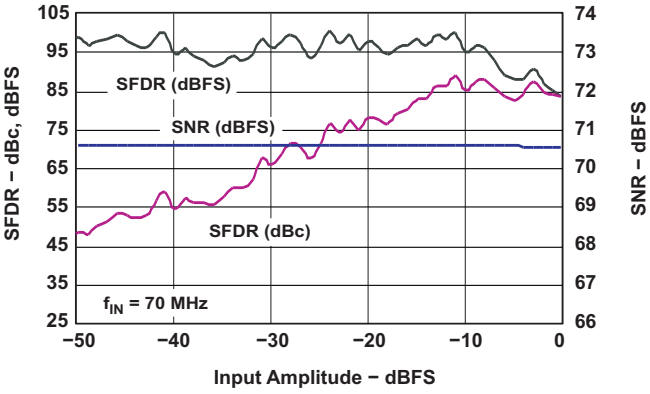


Figure 29.

PERFORMANCE vs CLOCK AMPLITUDE

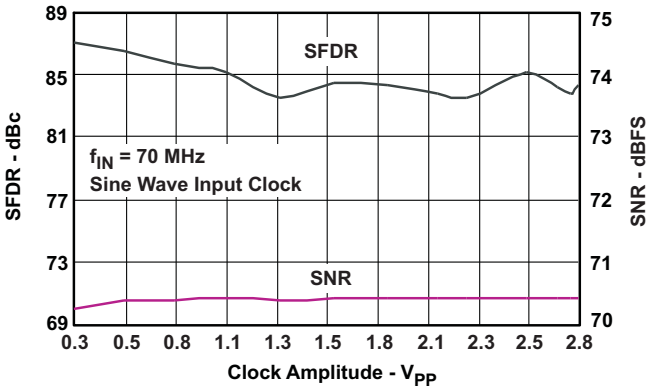


Figure 30.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

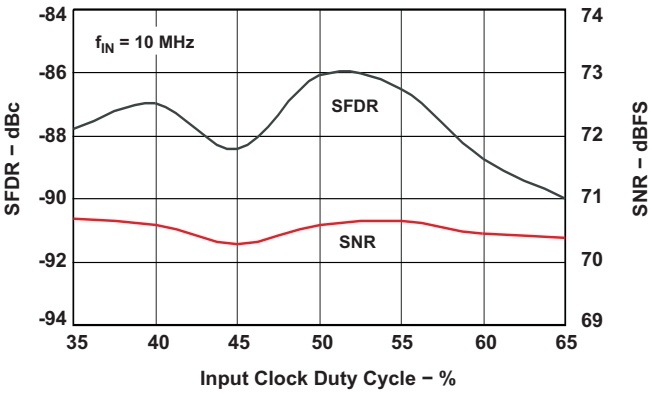


Figure 31.

OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE

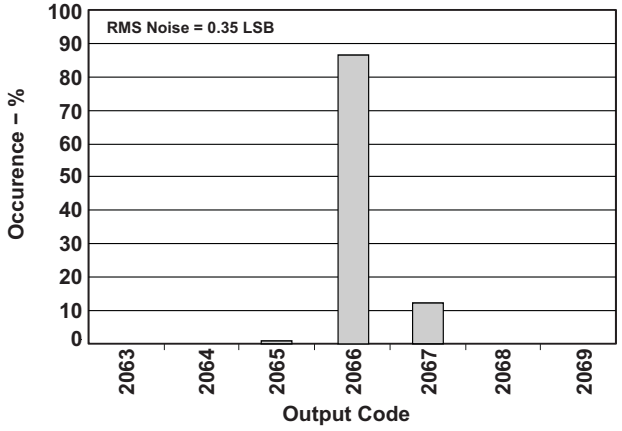


Figure 32.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

PERFORMANCE IN EXTERNAL REFERENCE MODE

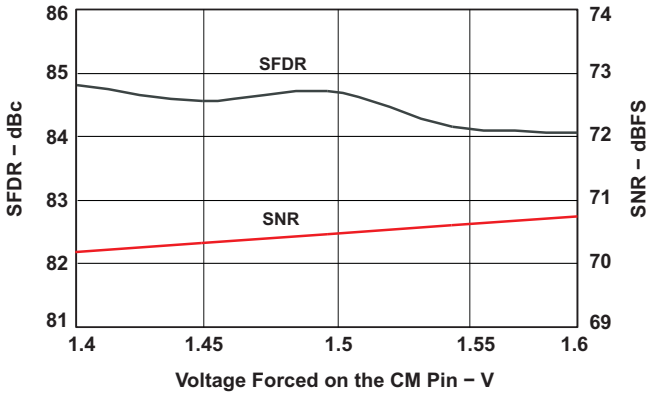


Figure 33.

COMMON-MODE REJECTION RATIO vs FREQUENCY

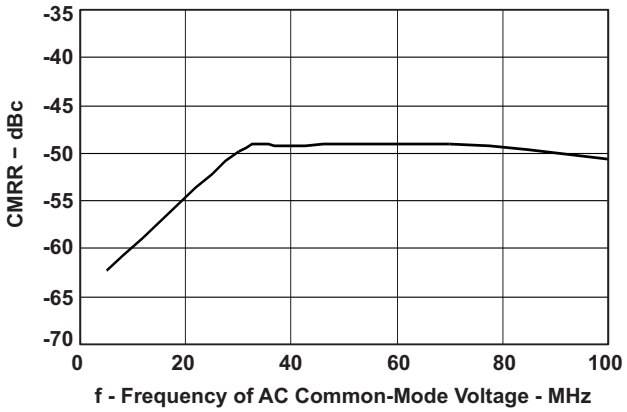


Figure 34.

POWER DISSIPATION vs
SAMPLING FREQUENCY (DDR LVDS)

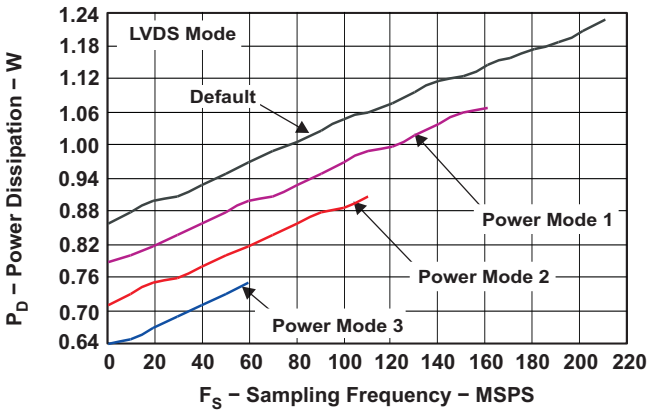


Figure 35.

DIGITAL CURRENT vs
SAMPLING FREQUENCY (Parallel CMOS)

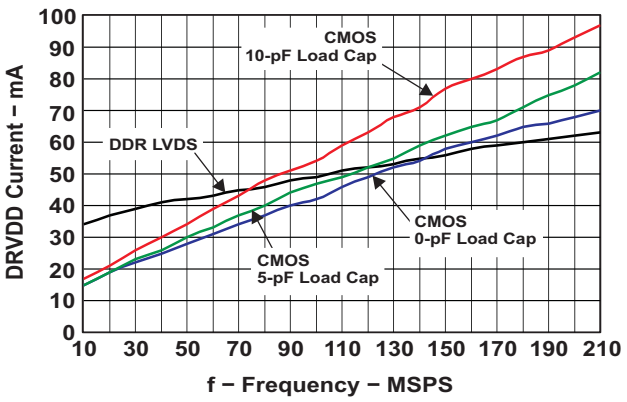


Figure 36.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 210 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

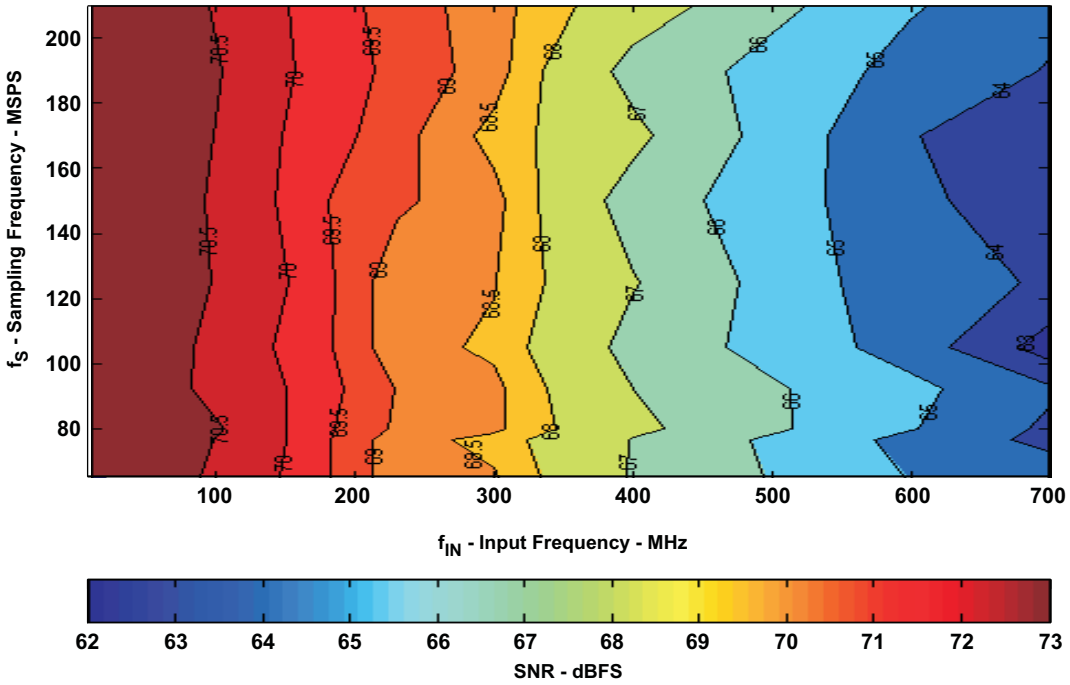


Figure 37. SNR Contour in dBFS

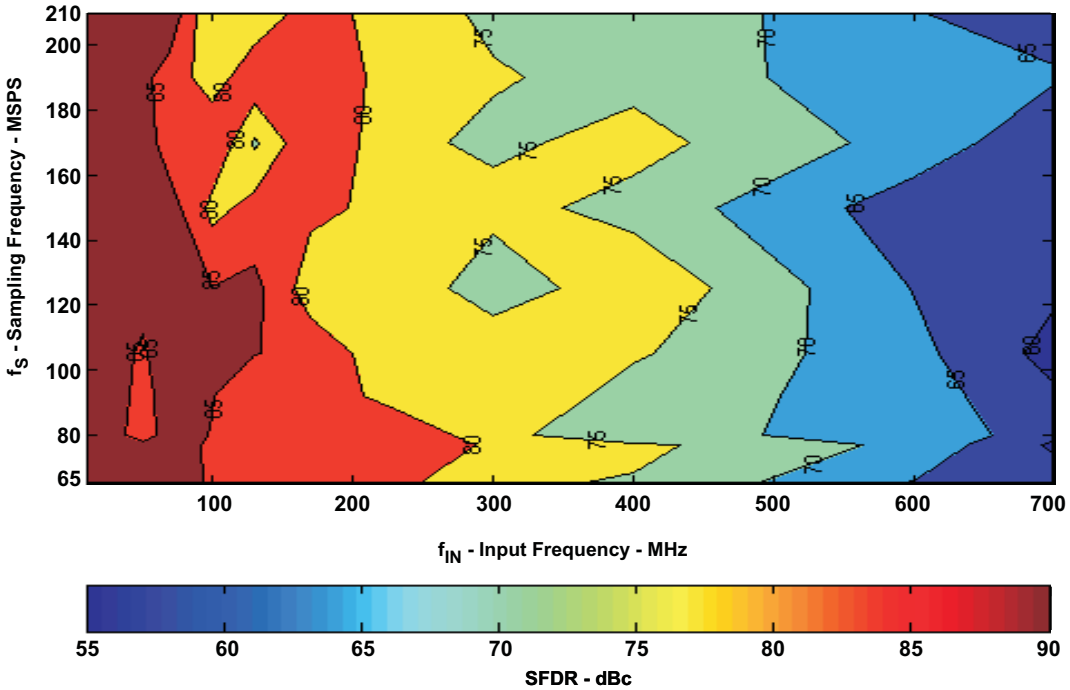


Figure 38. SFDR Contour in dBc

APPLICATION INFORMATION

THEORY OF OPERATION

ADS5527 is a low power 12-bit 210 MSPS pipeline ADC in a CMOS process. ADS5527 is based on switched capacitor technology and runs off a single 3.3-V supply. The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 14 clock cycles. The output is available as 12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2's complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 39.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

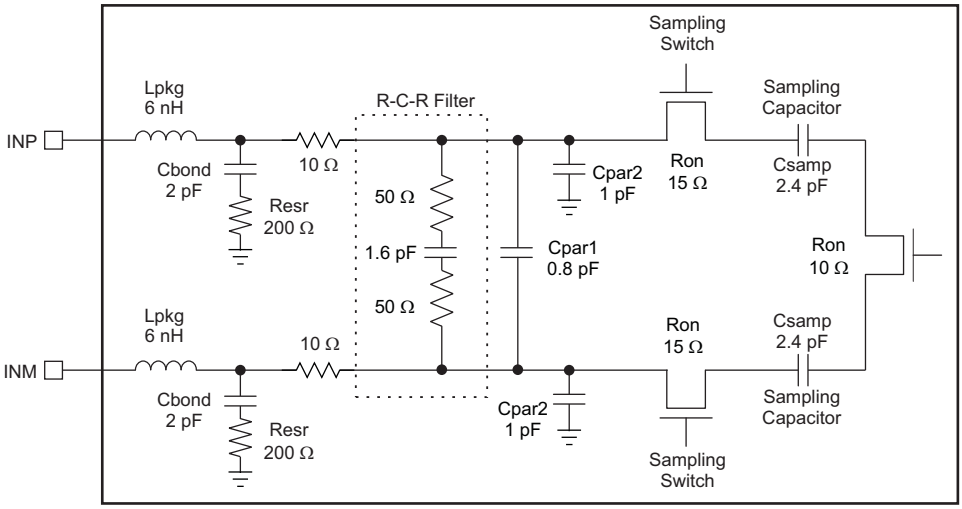


Figure 39. Input Stage

The input sampling circuit has a high 3-dB bandwidth that extends up to 800 MHz (measured from the input pins to the voltage across the sampling capacitors)

Drive Circuit Requirements

The input sampling circuit of the ADS5527 has a high 3-dB analog bandwidth of 800 MHz making it possible to sample input signals up to very high frequencies. To get best performance, it is recommended to have an external R-C-R filter across the input pins (Figure 40). This helps to filter the glitches due to the switching of the sampling capacitors. The R-C-R filter has to be designed to provide adequate filtering (for good performance) and at the same time ensure sufficient bandwidth over the desired frequency range.

In addition, it is recommended to have a 15-Ω series resistor on each input line to damp out ringing caused by the package parasitic. At higher input frequencies (> 100 MHz), a lower series resistance around 5 Ω to 10 Ω should be used. It is also necessary to present low impedance (< 50 Ω) for the common-mode switching currents. For example, this could be achieved by using two resistors from each input terminated to the common-mode voltage (Vcm).

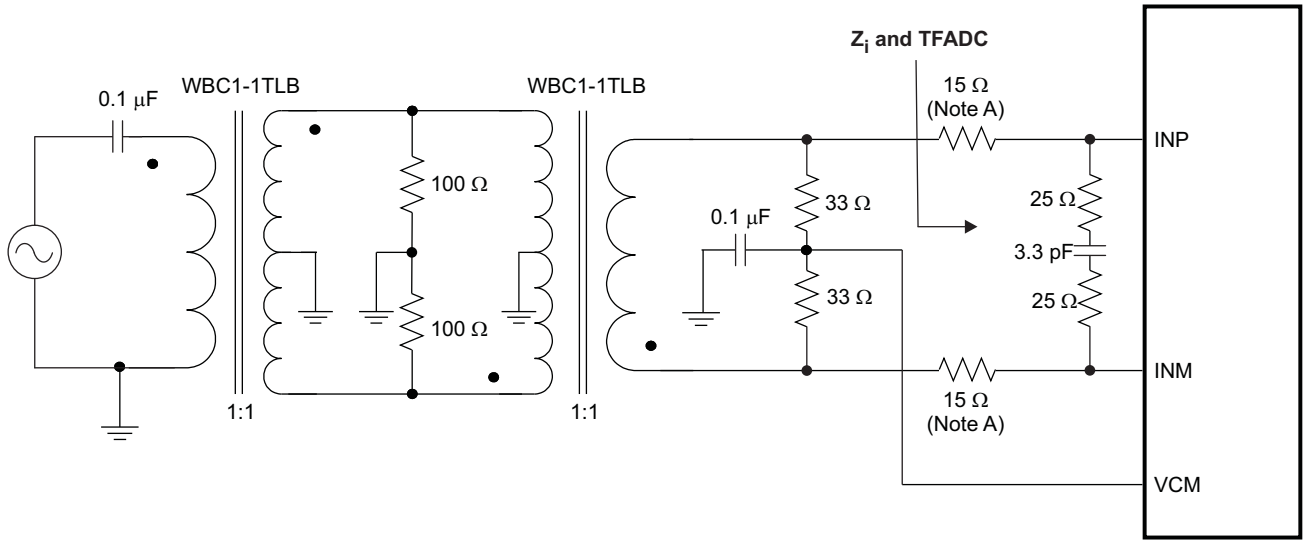
APPLICATION INFORMATION (continued)

Using 10-Ω series resistance and 25 Ω-3.3 pF-25 Ω as the R-C-R filter, high effective bandwidth (700 MHz) can be achieved, (see Figure 41, transfer function from the analog input pins to the voltage across the sampling capacitors).

In addition to the above ADC requirements, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. For this, the ADC input impedance has to be taken into account (Figure 42).

Example Drive Circuits

A suitable configuration using RF transformers and including the R-C-R filter is shown in Figure 40. Note the 15-Ω series resistors and the low common-mode impedance (using 33-Ω resistors terminated to VCM).



A. Use lower series resistance (≈ 5 Ω to 10 Ω) at high input frequencies (> 100 MHz)

Figure 40. Example Drive Circuit With RF Transformers

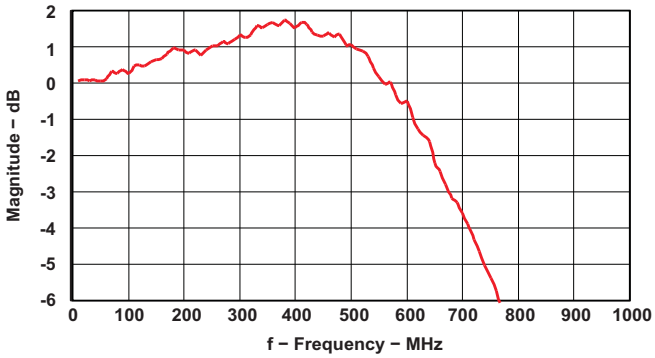


Figure 41. Analog Input Bandwidth, TFADC (Actual Silicon Data)

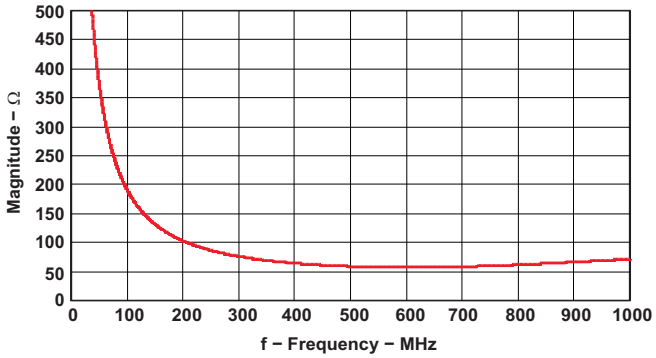


Figure 42. Input Impedance, Z_I

APPLICATION INFORMATION (continued)

Using RF transformers

For optimum performance, the analog inputs have to be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common-mode (VCM pin 13).

At higher input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair (Figure 40) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground. (Note that the drive circuit has to be tuned to account for this additional termination, to get the desired S11 and impedance match).

Using Differential Amplifier Drive Circuits

Figure 43 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to differential output that can be interface to the ADC analog input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB in Figure 43). R_{FIL} helps to isolate the amplifier outputs from the switching input of the ADC. Together with C_{FIL} it also forms a low-pass filter that band-limits the noise (& signal) at the ADC input. As the amplifier output is ac-coupled, the common-mode voltage of the ADC input pins is set using two 200 Ω resistors connected to VCM.

The amplifier output can also be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4 V and -1 V supplies for the THS4509 so that its output common-mode voltage (1.5 V) is at mid-supply.

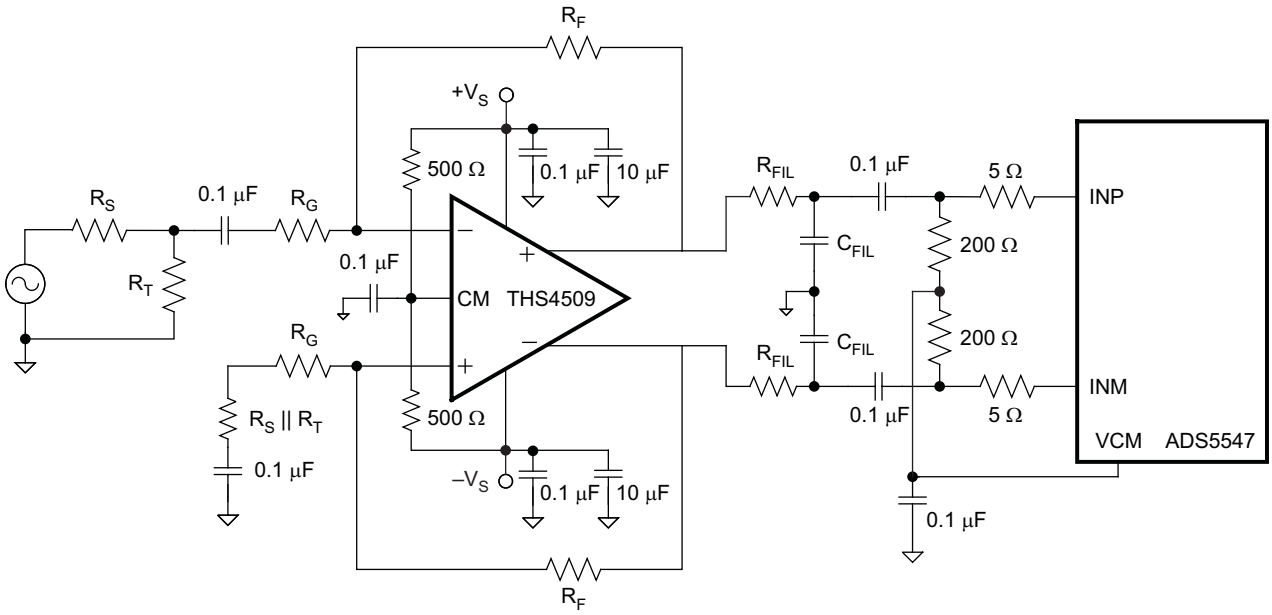


Figure 43. Drive Circuit Using the THS4509

See the EVM User Guide (SLWU028) for more information.

APPLICATION INFORMATION (continued)

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-μF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 342 μA (at 210 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{(342\ \mu A)\ x\ Fs}{210\ MSPS} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

Reference

ADS5527 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by controlling the MODE pin 23 (see Table 7 for details) or by programming the serial interface register bit **<REF>** (Table 16).

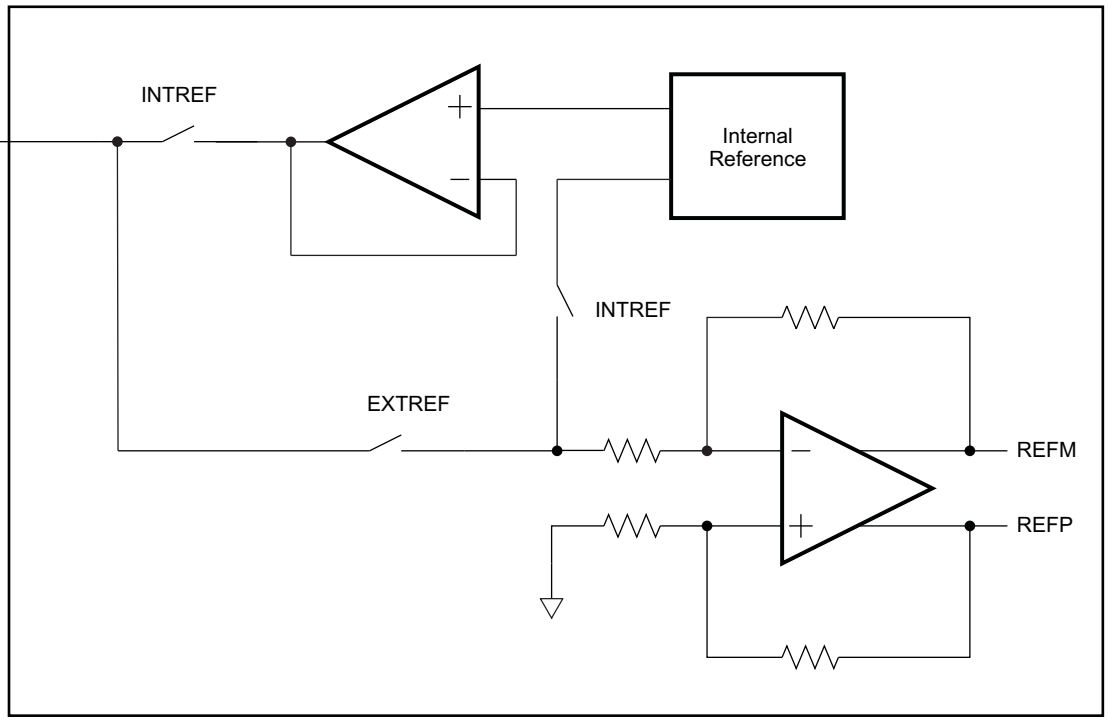


Figure 44. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

APPLICATION INFORMATION (continued)

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

$$\text{Full−scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the 1.5 V common-mode voltage to bias the input pins has to be generated externally. There is no change in performance compared to internal reference mode.

Low Sampling Frequency Operation

For best performance at high sampling frequencies, ADS5527 uses a clock generator circuit to derive internal timing for the ADC. The clock generator operates from 210 MSPS down to 50 MSPS in the DEFAULT SPEED mode. The ADC enters this mode after applying reset (with serial interface configuration) or by tying SCLK pin to **low** (with parallel configuration).

For low sampling frequencies (below 50 MSPS), the ADC must be put in the LOW SPEED mode. This mode can be entered by:

- setting the register bit **<LOW SPEED>** through the serial interface, OR
- tying the SCLK pin to **high** (see Table 3) using the parallel configuration.

Clock Input

ADS5527 clock inputs can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 45. This allows the use of transformer-coupled drive circuits for sine wave clock, or ac-coupling for LVPECL, LVDS clock sources (Figure 46 and Figure 47)

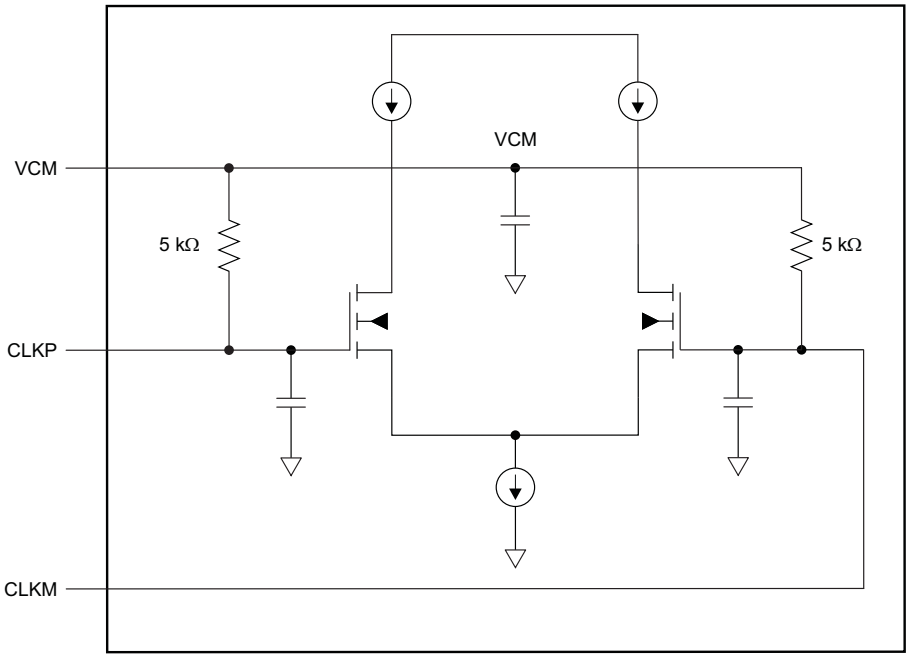


Figure 45. Internal Clock Buffer

APPLICATION INFORMATION (continued)

For best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1-µF capacitors, as shown in Figure 46.

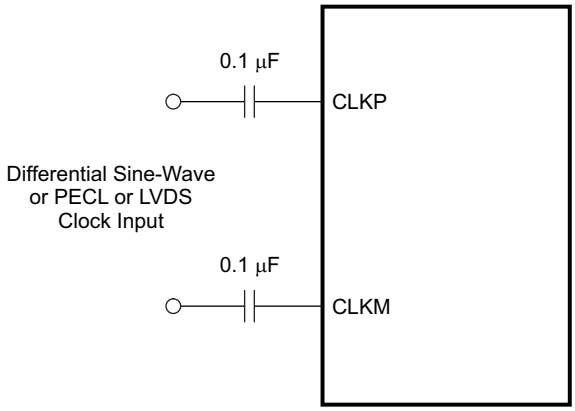


Figure 46. Differential Clock Driving Circuit

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin 11) connected to ground with a 0.1-µF capacitor, as shown in Figure 47.

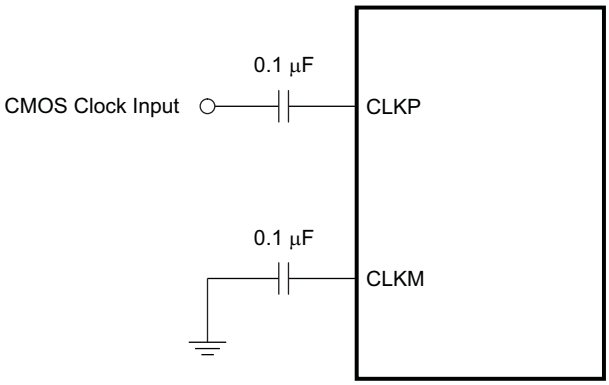


Figure 47. Single-Ended Clock Driving Circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, the use a clock source with very low jitter is recommended. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 31 shows the performance variation of the ADC versus clock duty cycle

Clock Buffer Gain

When using a sinusoidal clock input, the noise contributed by clock jitter improves as the clock amplitude is increased. Therefore, using a large amplitude clock is recommended. In addition, the clock buffer has a programmable gain option to amplify the input clock. The clock buffer gain can be set by programming the register bits **<CLKIN GAIN>** (Table 14). The clock buffer gain decreases monotonically from Gain 4 to Gain 0 settings.

APPLICATION INFORMATION (continued)

Programmable Gain

ADS5527 has programmable gain from 0 dB to 6 dB in steps of 1 dB. The corresponding full-scale input range varies from 2 V_{PP} down to 1 V_{PP}, with 0 dB being the default gain. At high IF, this is especially useful as the SFDR improvement is significant with marginal degradation in SNR.

The gain can be programmed using the serial interface (bits D3-D0 in register 0x68).

Power Down

ADS5527 has three power-down modes – global STANDBY, output buffer disabled, and input clock stopped.

Global STANDBY

This mode can be initiated by controlling SDATA (pin 28) or by setting the register bit **<STBY>** (Table 10) through the serial interface. In this mode, the A/D converter, reference block and the output buffers are powered down and the total power dissipation reduces to about 100 mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid normal mode is maximum 100 µs.

Output Buffer Disable

The output buffers can be disabled using OE pin 7 in both the LVDS and CMOS modes, reducing the total power by about 100 mW. With the buffers disabled, the outputs are in high impedance state. The wake-up time from this mode to data becoming valid in normal mode is maximum 1 µs in LVDS mode and 50 ns in CMOS mode.

Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 100 mW and the wake-up time from this mode to data becoming valid in normal mode is maximum 100 µs.

APPLICATION INFORMATION (continued)

Power Scaling Modes

ADS5527 has a power scaling mode in which the device can be operated at reduced power levels at lower sampling frequencies with no difference in performance. (See Figure 27)(1) There are four power scaling modes for different sampling clock frequency ranges, using the serial interface register bits **<SCALING>** (Table 16). Only the AVDD power is scaled, leaving the DRVDD power unchanged.

Table 19. Power Scaling vs Sampling Speed

Sampling Frequency MSPS	Power Scaling Mode	Analog Power (Typical)	Analog Power in Default Mode
> 150	Default	1010 mW at 210 MSPS	1010 mW at 210 MSPS
105 to 150	Power Mode 1	841 mW at 150 MSPS	917 mW at 150 MSPS
50 to 105	Power Mode 2	670 mW at 105 MSPS	830 mW at 105 MSPS
< 50	Power Mode 3	525 mW at 50 MSPS	760 mW at 50 MSPS

(1) The performance in the power scaling modes is from characterization and not tested in production.

Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

Digital Output Information

ADS5527 provides 12-bit data, an output clock synchronized with the data and an out-of-range indicator that goes high when the output reaches the full-scale limits. In addition, output enable control (OE pin 7) is provided to power down the output buffers and put the outputs in high-impedance state.

Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the DFS (see Table 6) or the serial interface register bit **<ODI>** (Table 15).

DDR LVDS Outputs

In this mode, the 12 data bits and the output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair as shown in Figure 48. So, there are 6 LVDS output pairs for the 12 data bits and 1 LVDS output pair for the output clock.

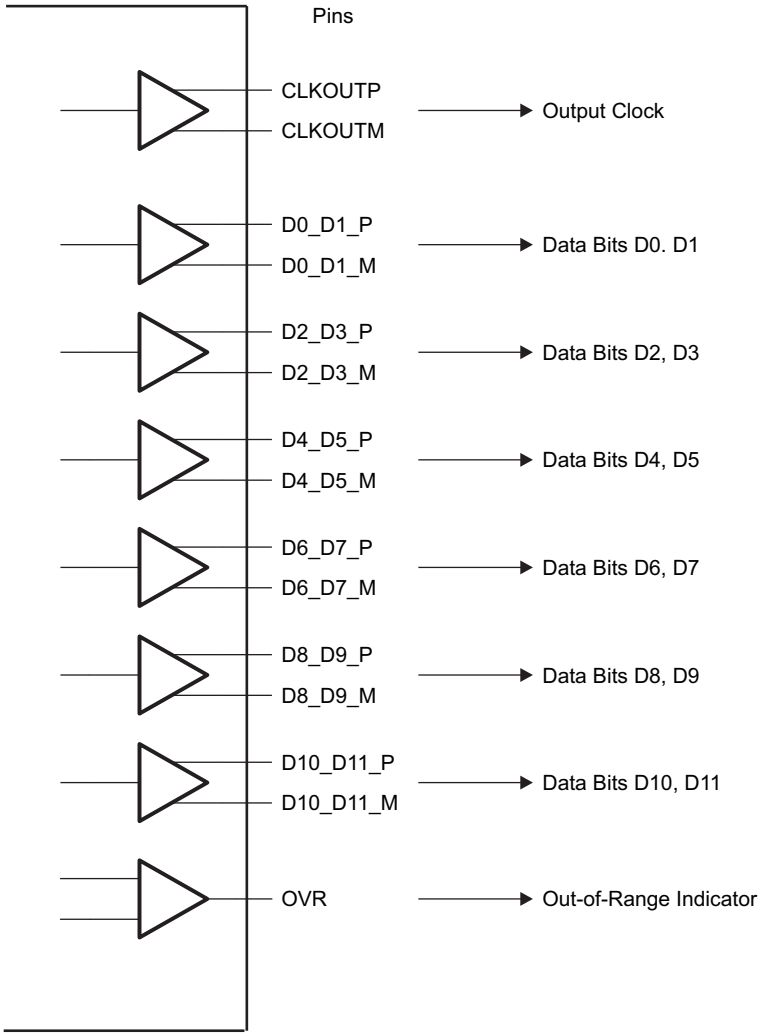


Figure 48. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8, and D10 are output at the falling edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, and D11 are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the 12 data bits (see Figure 49).

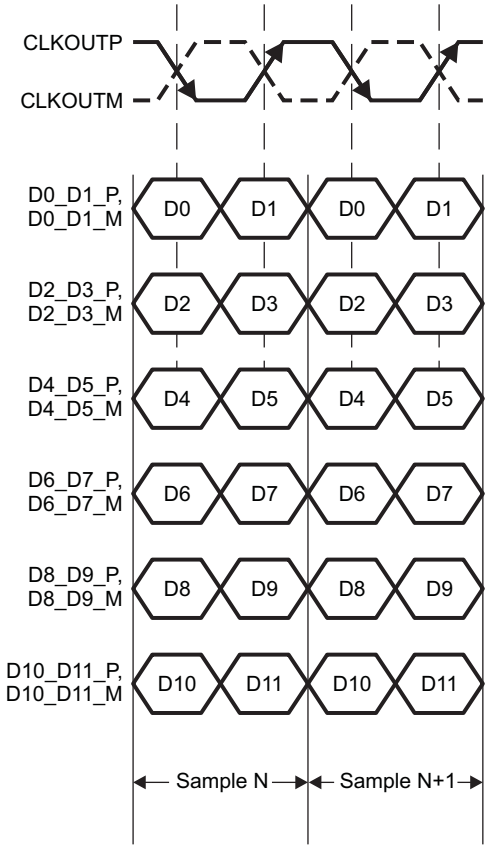


Figure 49. DDR LVDS Interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mV_{PP} differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA using the register bits **<LVDS CURR>** (Table 17). In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers (register bits **<CURR DOUBLE>**, Table 18).

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistences available are – 325, 200, and 170 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistences. This results in eight effective terminations from open (no termination) to 75 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100-Ω internal and 100-Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. Figure 50 shows the eye diagram of one of the LVDS data outputs with a 10-pF load capacitance (from each pin to ground) and 100-Ω internal termination enabled. The termination can be programmed using register bits **<DATA TERM>** and **<CLKOUT TERM>** (Table 17).

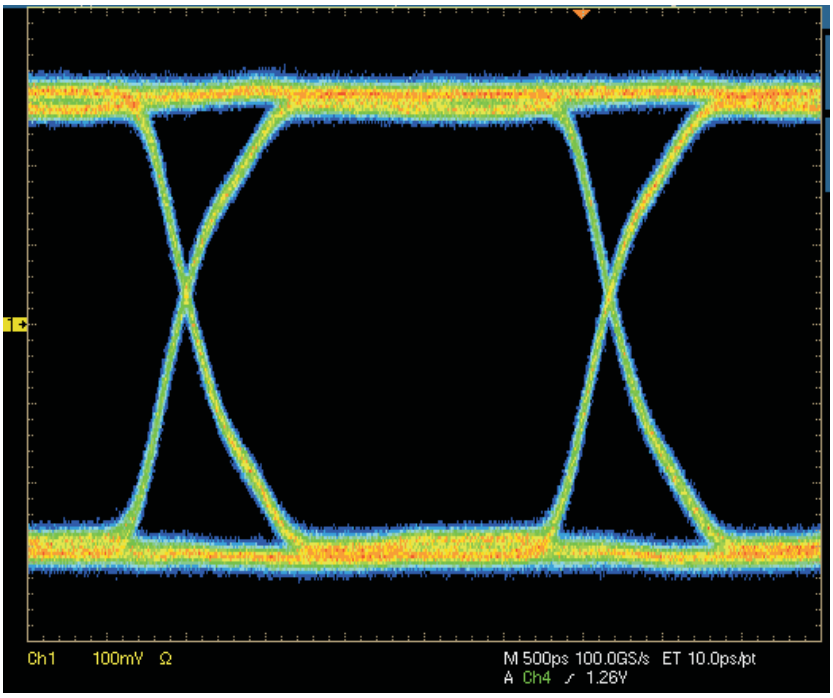


Figure 50. Eye Diagram of LVDS Data Output With Internal Termination

Parallel CMOS

In this mode, the 12 data outputs and the output clock are available as 3.3-V CMOS voltage levels. Each data bit and the output clock is available on a separate pin in parallel. By default, the data outputs are valid during the rising edge of the output clock. The output clock is CLKOUT (pin 5).

CMOS Mode Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin (see Figure 36). The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_L \times V_{DRVDD} \times (N \times F_{AVG})$

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching

Figure 36 shows the current with various load capacitances across sampling frequencies at 2MHz analog input frequency.

Output Switching Noise and Data Position Programmability (in CMOS mode ONLY)

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. To minimize this, the device includes programmable options to move the output data transitions with respect to the output clock. This can be used to position the data transitions at the optimum place away from the sampling instant and improve the SNR. Figure 21 shows the variation of SNR for different CMOS output data positions at 190 MSPS.

Note that the optimum output data position varies with the sampling frequency. The data position can be programmed using the register bits **<DATA POSN>** (Table 9).

It is recommended to put series resistors (50 to 100 Ω) on each output line placed very close to the converter pins. This helps to isolate the outputs from seeing large load capacitances and in turn reduces the amount of switching noise. For example, the data in Figure 21 was taken with 50 Ω series resistors on each output line.

Output Clock Position Programmability

In both the LVDS and CMOS modes, the output clock can be moved around its default position. This can be done using SEN pin 27 (as described in Table 5) or using the serial interface register bits **<CLKOUT POSN>** (Table 9). Using this allows to trade-off the setup and hold times leading to reliable data capture. There also exists an option to align the output clock edge with the data transition.

Note that programming the output clock position also affects the clock propagation delay times.

Output Data Format

Two output data formats are supported – 2's complement and offset binary. They can be selected using the DFS (pin 6) or the serial interface register bit **<DF>** (Table 10).

Out-of-Range Indicator (OVR)

When the input voltage exceeds the full-scale range of the ADC, OVR (pin 3) goes high, and the output code is clamped to the appropriate full-scale level for the duration of the overload. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2's complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2's complement output format. Figure 51 shows the behavior of OVR during the overload. Note that OVR and the output code react to the overload after a latency of 14 clock cycles.

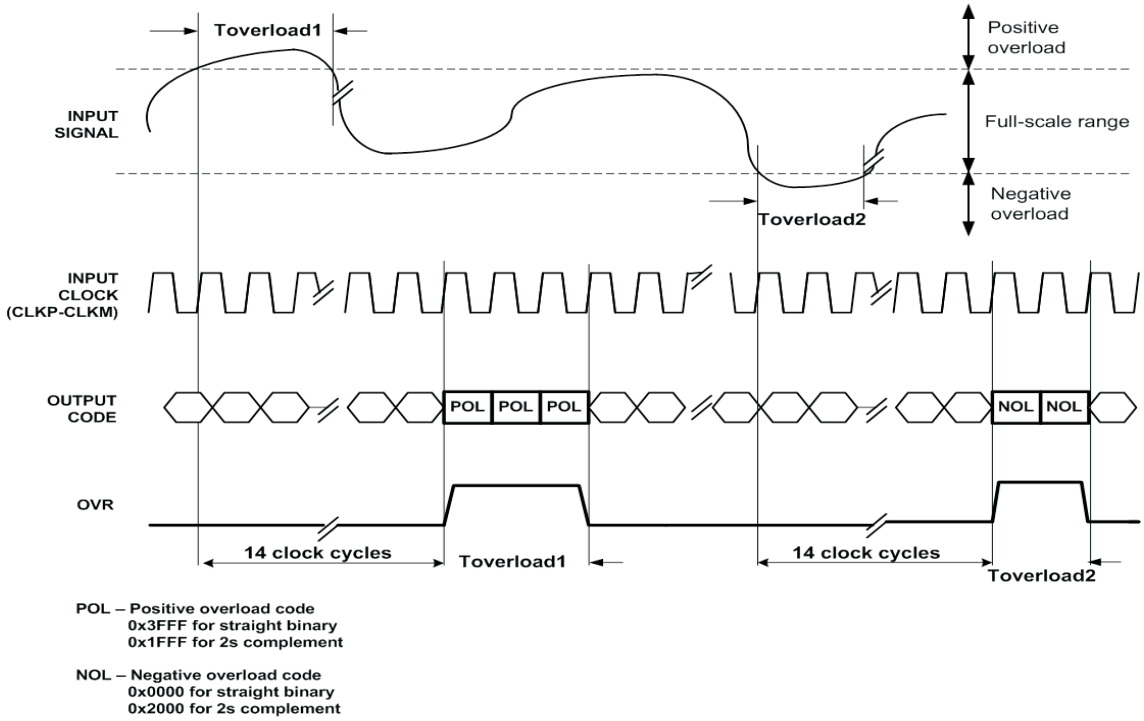


Figure 51. OVR During Input Overvoltage

Output Timing

For the best performance at high sampling frequencies, ADS5527 uses a clock generator circuit to derive internal timing for ADC. This results in optimal setup and hold times of the output data and 50% output clock duty cycle for sampling frequencies from 80 MSPS to 210 MSPS. See Table 20 for timing information above 80 MSPS.

Table 20. Timing Characteristics (80 MSPS to 210 MSPS) (1)

Fs, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
DDR LVDS									
190	1.2	1.7		0.4	0.9		4.0	4.7	5.4
170	1.3	1.8		0.5	1.0		3.9	4.6	5.3
150	1.6	2.1		0.6	1.1		4.3	5.0	5.7
130	2.0	2.5		0.8	1.3		4.5	5.2	5.9
80	3.6	4.1		1.6	2.1		4.7	5.7	6.7
PARALLEL CMOS									
190	2.2	3.0		0.5	0.9		2.4	3.2	4.0
170	2.5	3.3		0.8	1.2		1.9	2.7	3.5
150	2.8	3.6		1.2	1.6		1.7	2.5	3.3
130	3.3	4.1		1.7	2.1		1.1	1.9	2.7
80	6.0	7.0		3.7	4.1		10.8	12	13.2

(1) Timing parameters are specified by design and characterization and not tested in production.

Below 80 MSPS, the setup and hold times do not scale with the sampling frequency. The output clock duty cycle also progressively moves away from 50% as the sampling frequency is reduced from 80 MSPS.

See Table 21 for timings at sampling frequencies below 80 MSPS. Figure 52 shows the clock duty cycle across sampling frequencies in the DDR LVDS and CMOS modes.

Table 21. Timing Characteristics (1 MSPS to 80 MSPS) (1)

Fs, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
DDR LVDS									
1 to 80	3.6			1.6				5.7	
PARALLEL CMOS									
1 to 80	6			3.7				12	

(1) Timing parameters are specified by design and characterization and not tested in production.

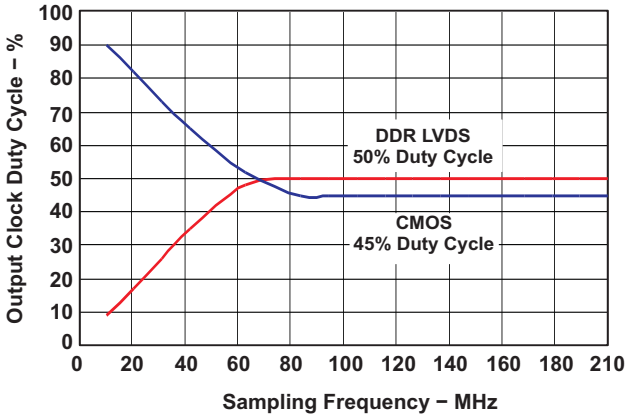


Figure 52. Output Clock Duty Cycle (Typical) vs Sampling Frequency

The latency of ADS5527 is 14 clock cycles from the sampling instant (input clock rising edge). In the LVDS mode, the latency remains constant across sampling frequencies. In the CMOS mode, the latency is 14 clock cycles above 80 MSPS and 13 clock cycles below 80 MSPS.

Board Design Considerations

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital and clock sections of the board are cleanly partitioned. Refer to the EVM User Guide (SLWU028) for details on layout and grounding.

Supply Decoupling

As the ADS5527 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help to filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

Series Resistors on Data Outputs

It is recommended to put series resistors (50 to 100 Ω) on each output line placed very close to the converter pins. This helps to isolate the outputs from seeing large load capacitances and in turn reduces the amount of switching noise.

Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes ***QFN Layout Guidelines*** (SLOA122) and ***QFN/SON PCB Attachment*** (SLUA271).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

DEFINITION OF SPECIFICATIONS (continued)

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (6)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (7)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

DEFINITION OF SPECIFICATIONS (continued)

AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If ΔV_{SUP} is the change in the supply voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (8)$$

Common Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If ΔVcm is the change in the input common-mode voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (9)$$

Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

Changes from Original (December 2006) to A Revision **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5527IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5527	Samples
ADS5527IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5527	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

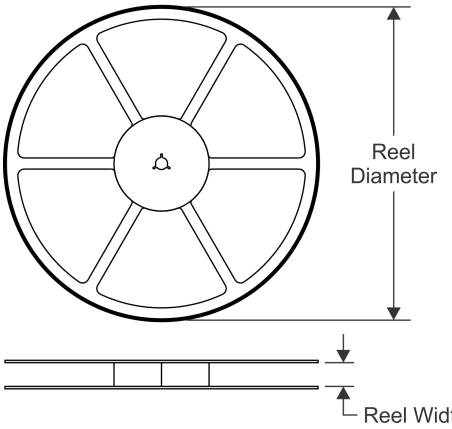
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

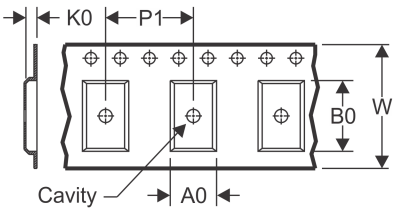
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

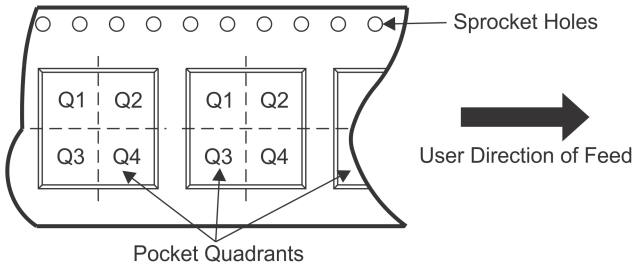


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

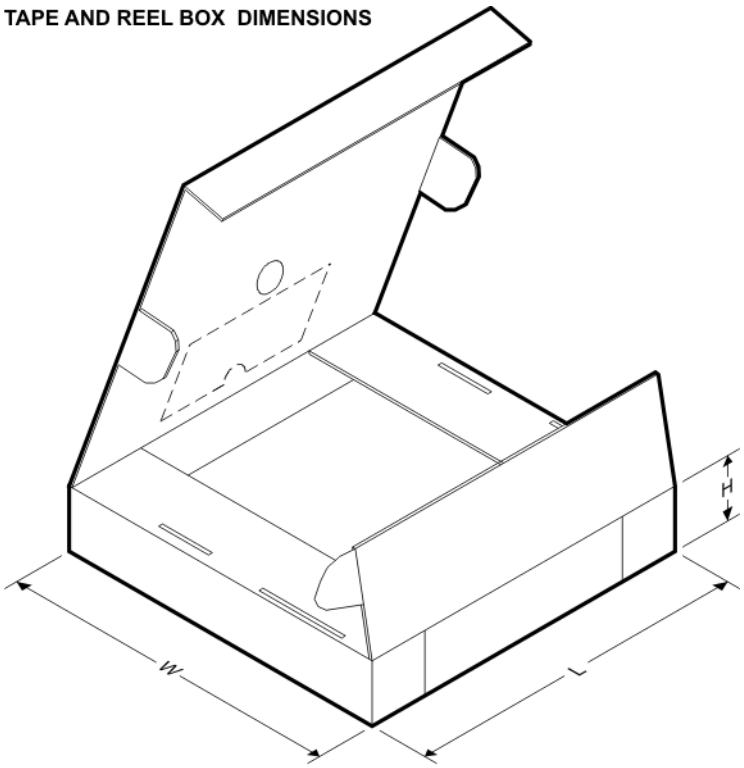
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5527IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS5527IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5527IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS5527IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

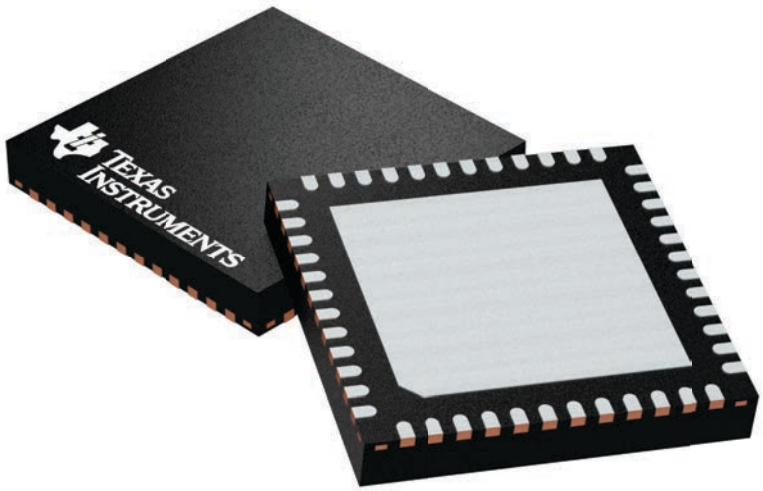
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

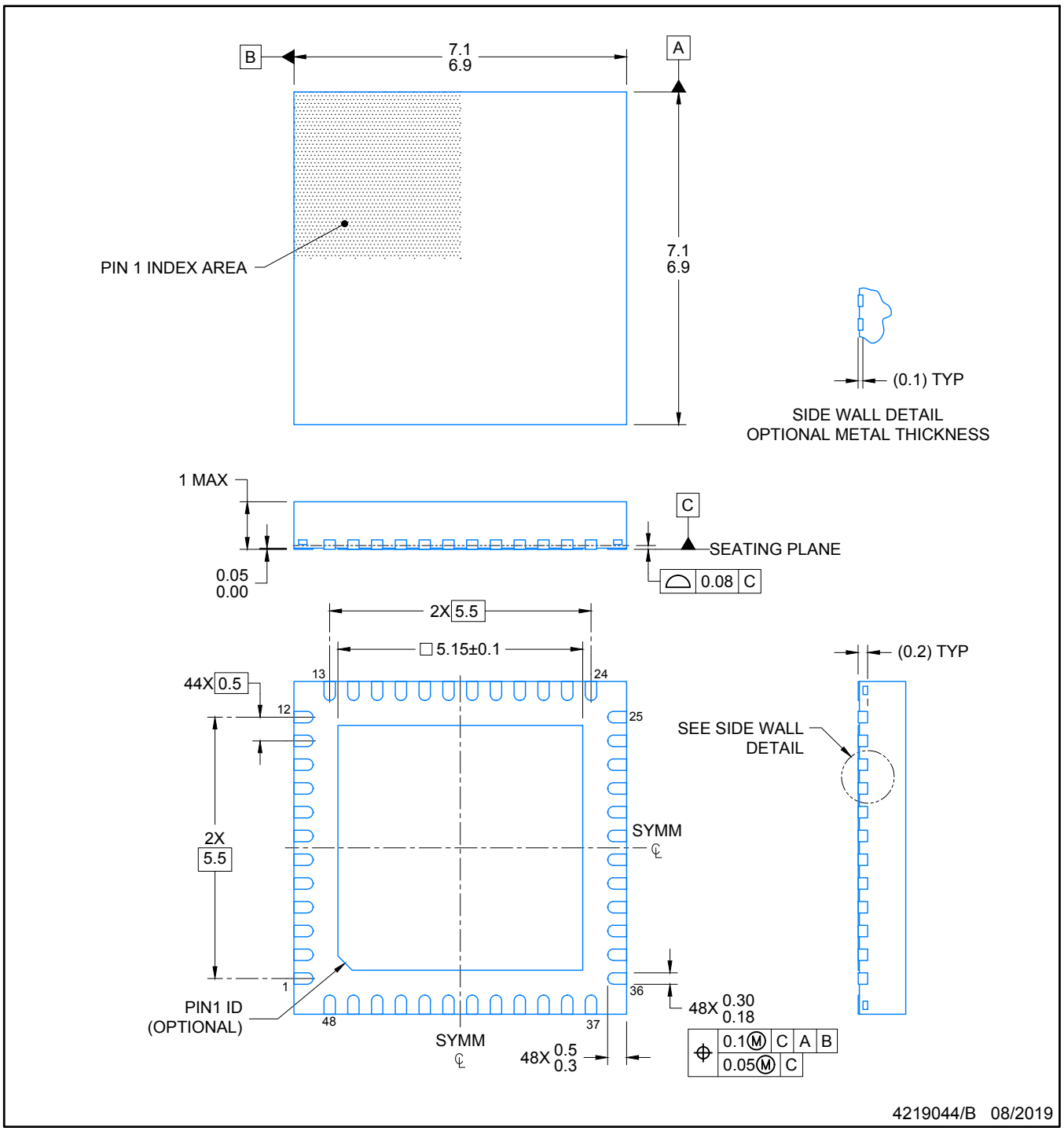
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



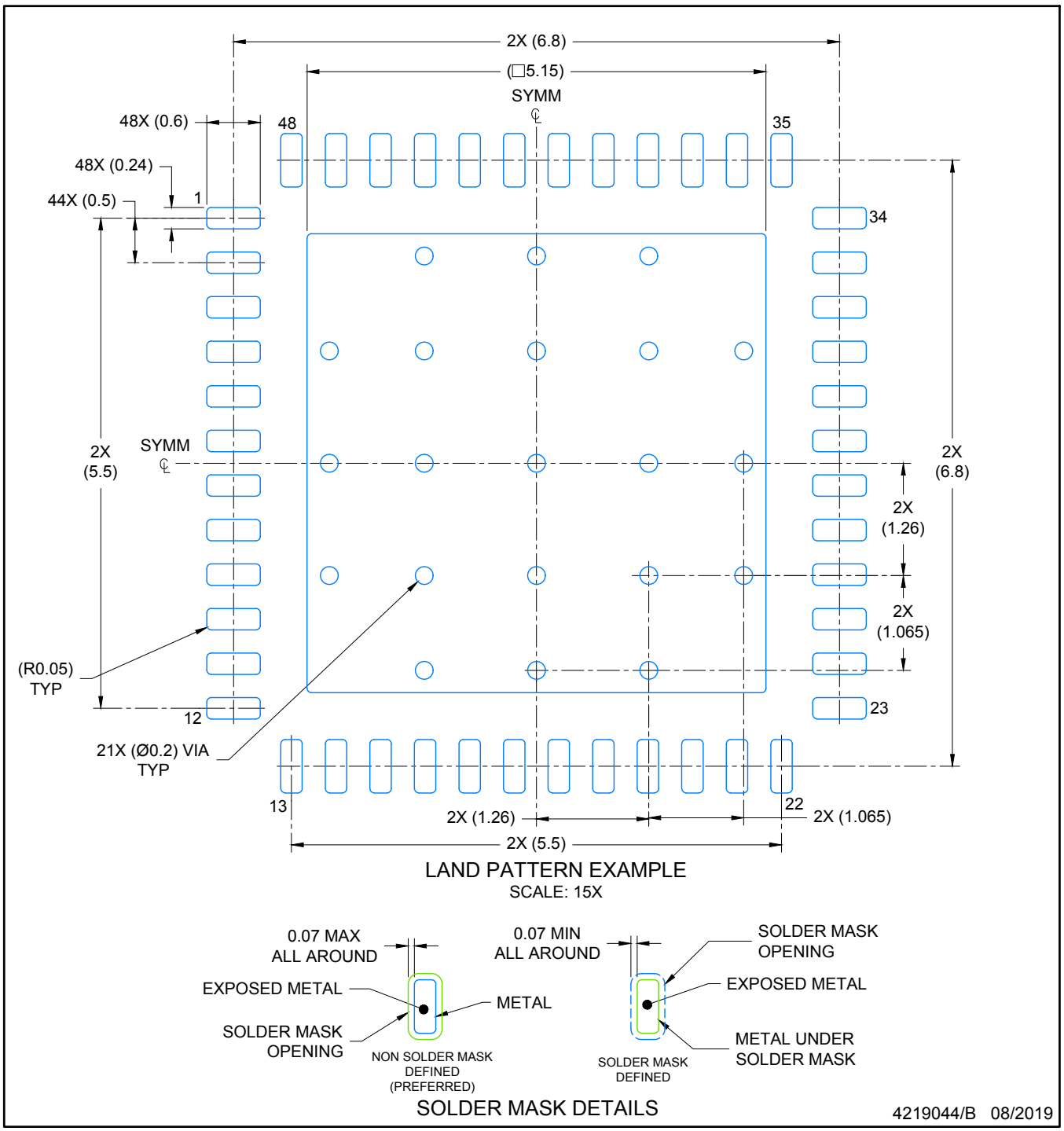
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



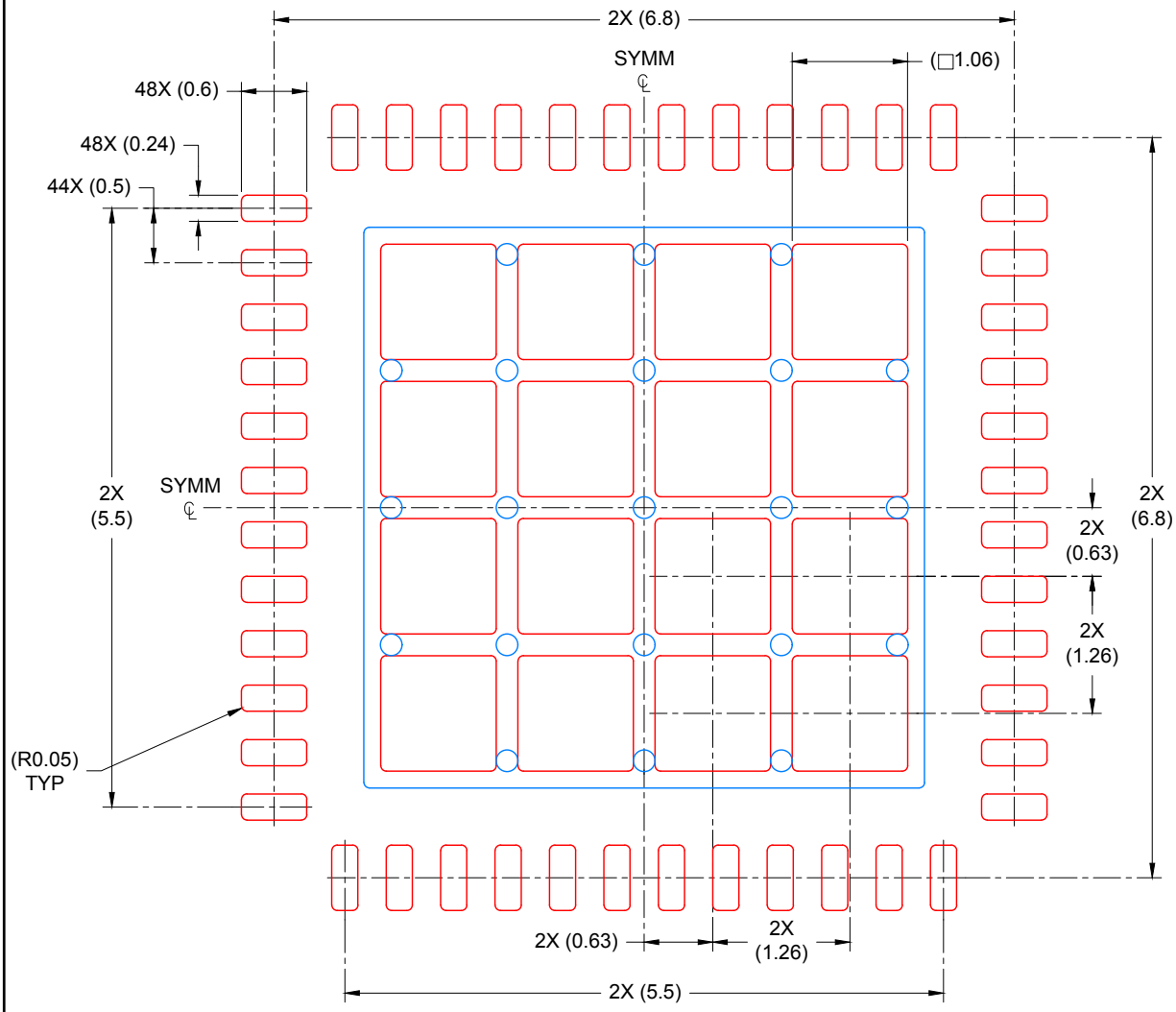
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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