74AHC132-Q100; 74AHCT132-Q100

Quad 2-input NAND Schmitt trigger

Rev. 1 — 8 November 2013 Product data sheet

1. General description

The 74AHC132-Q100; 74AHCT132-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC132-Q100; 74AHCT132-Q100 contains four 2-input NAND gates which accept standard input signals. They can transform slowly changing input signals into sharply defined, jitter free output signals. The gate switches at different points for positive-going and negative-going signals. The difference between the positive voltage V_{T+} and the negative V_{T-} is defined as the hysteresis voltage V_H.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Balanced propagation delays
- Inputs accept voltages higher than V_{CC}
- Input levels:
  - For 74AHC132-Q100: CMOS level
  - For 74AHCT132-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC132D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT132D-Q100				
74AHC132PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT132PW-Q100				
74AHC132BQ-Q100	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT132BQ-Q100				

4. Functional diagram

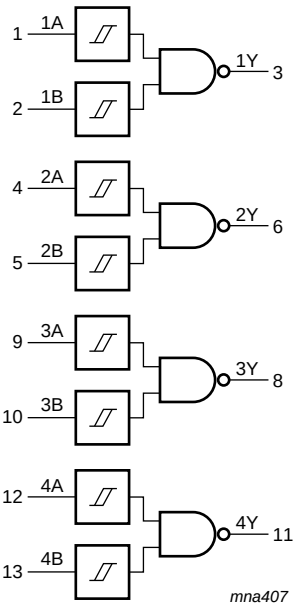


Fig 1. Logic symbol

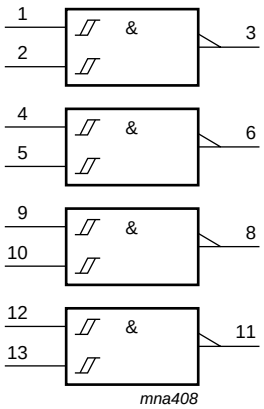


Fig 2. IEC logic symbol

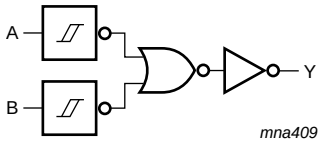


Fig 3. Logic diagram (one Schmitt trigger)

5. Pinning information

5.1 Pinning

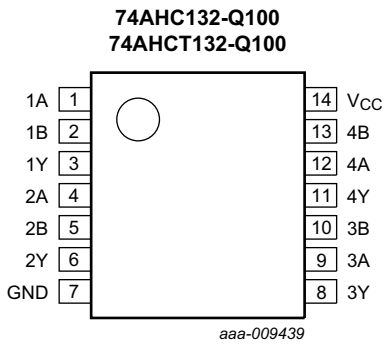
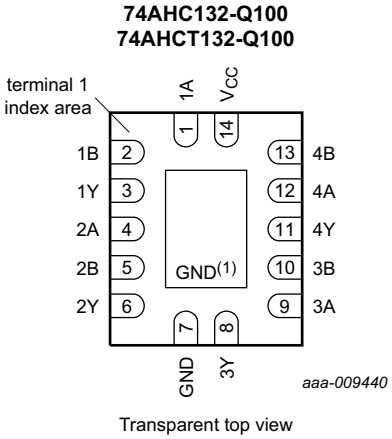


Fig 4. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input nA
1B, 2B, 3B, 4B	2, 5, 10, 13	data input nB
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output nY
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage			−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	−20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	−20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		−25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			−75	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP14 package: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN14 package: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC132-Q100						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT132-Q100						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC132-Q100										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	2.2	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	3.15	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	3.85	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF
74AHCT132-Q100										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other pins at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7.

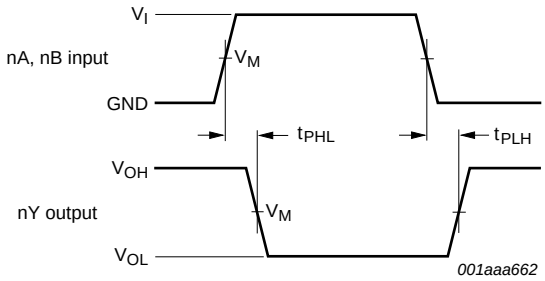
Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC132-Q100											
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	4.4	11.9	1.0	14.0	1.0	15.0	ns
		C_L = 50 pF		-	6.2	15.4	1.0	17.5	1.0	19.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.3	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF		-	4.7	9.7	1.0	11.0	1.0	12.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	11	-	-	-	-	-	pF
74AHCT132-Q100											
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]								
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.5	7.0	1.0	8.0	1.0	9.0	ns
		C_L = 50 pF		-	5.0	8.0	1.0	9.0	1.0	10.0	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	14	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



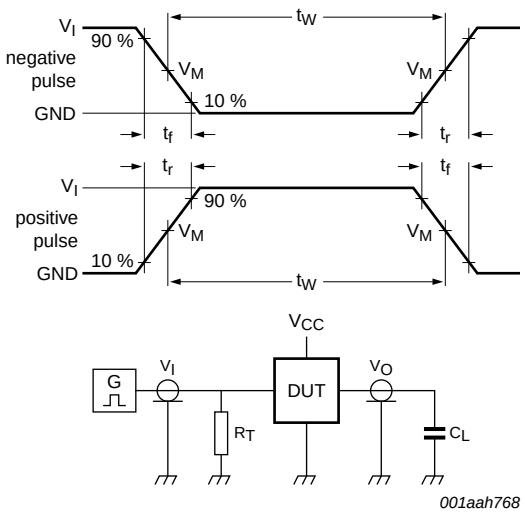
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC132-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT132-Q100	1.5 V	$0.5 \times V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC132-Q100	V_{CC}	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}
74AHCT132-Q100	3.0 V	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}

12. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC132-Q100										
V_{T+}	positive-going threshold voltage	V_{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V_{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V_{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V_{T-}	negative-going threshold voltage	V_{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V_{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V_{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V_H	hysteresis voltage	V_{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.25	1.2	V
		V_{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V_{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.45	1.6	V
74AHCT132-Q100										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	-	-	1.9	-	1.9	-	1.9	V
		V_{CC} = 5.5 V	-	-	2.1	-	2.1	-	2.1	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
		V_{CC} = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.3	-	1.4	0.3	1.4	0.3	1.4	V
		V_{CC} = 5.5 V	0.3	-	1.5	0.3	1.5	0.3	1.5	V

13. Transfer characteristics waveforms

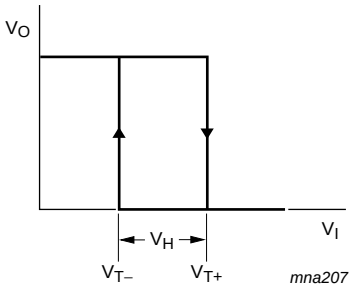


Fig 8. Transfer characteristics

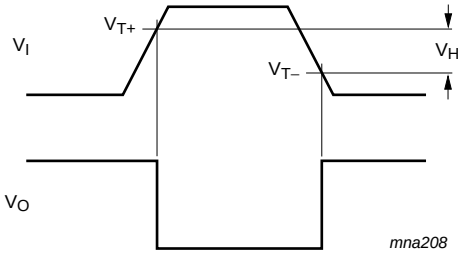
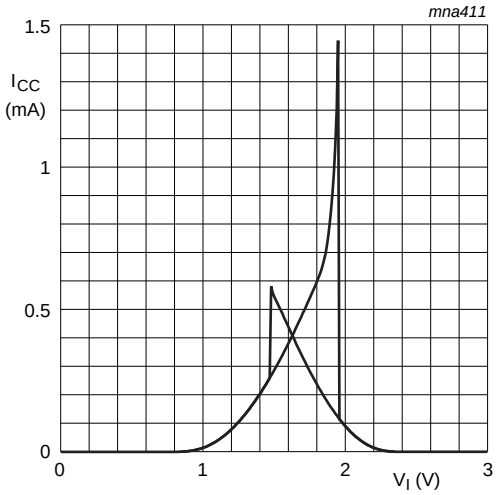
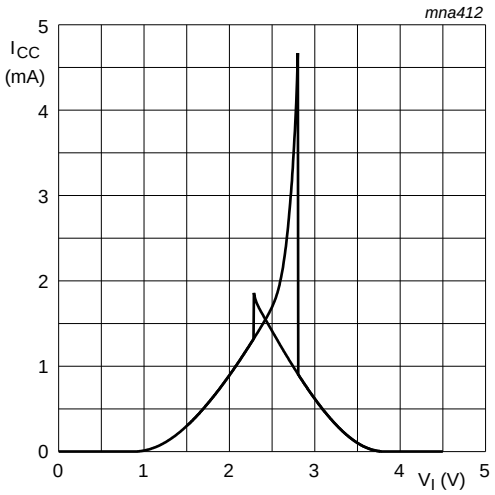


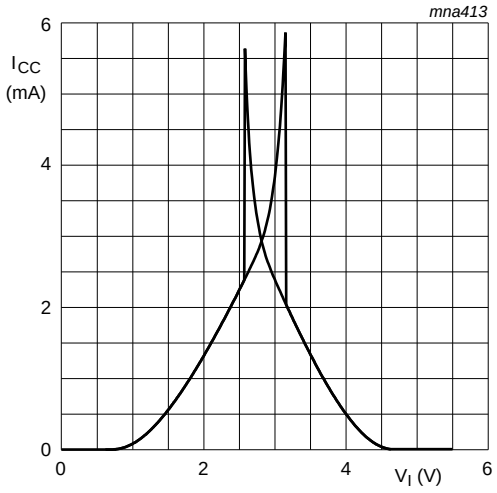
Fig 9. Definition of V_{T+}, V_{T-} and V_H



a. V_{CC} = 3.0 V

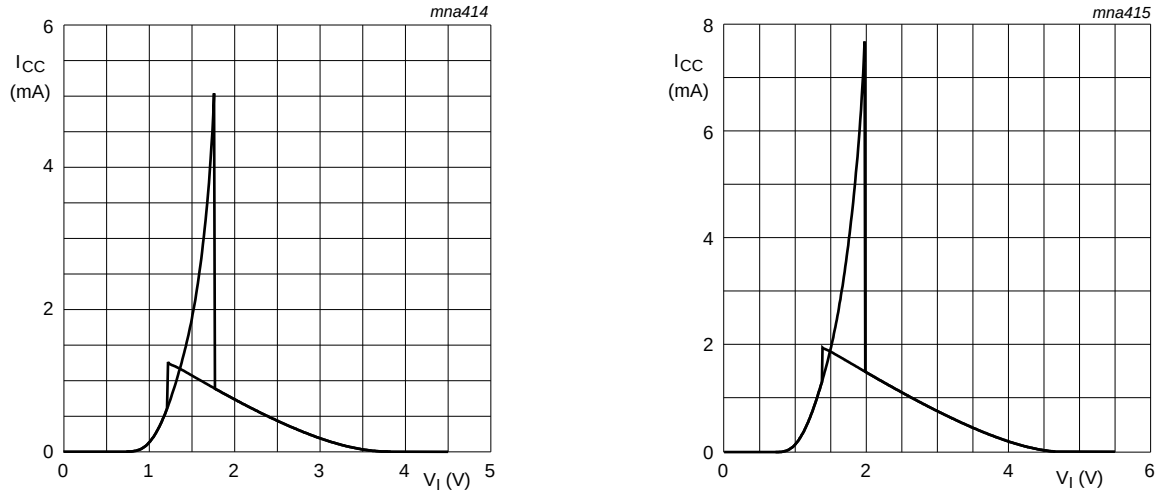


b. V_{CC} = 4.5 V



c. V_{CC} = 5.5 V

Fig 10. Typical 74AHC132-Q100 transfer characteristics

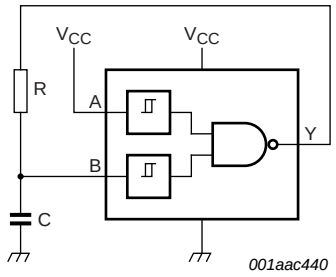


a. V_{CC} = 4.5 V.

b. V_{CC} = 5.5 V.

Fig 11. Typical 74AHCT132-Q100 transfer characteristics

14. Application information



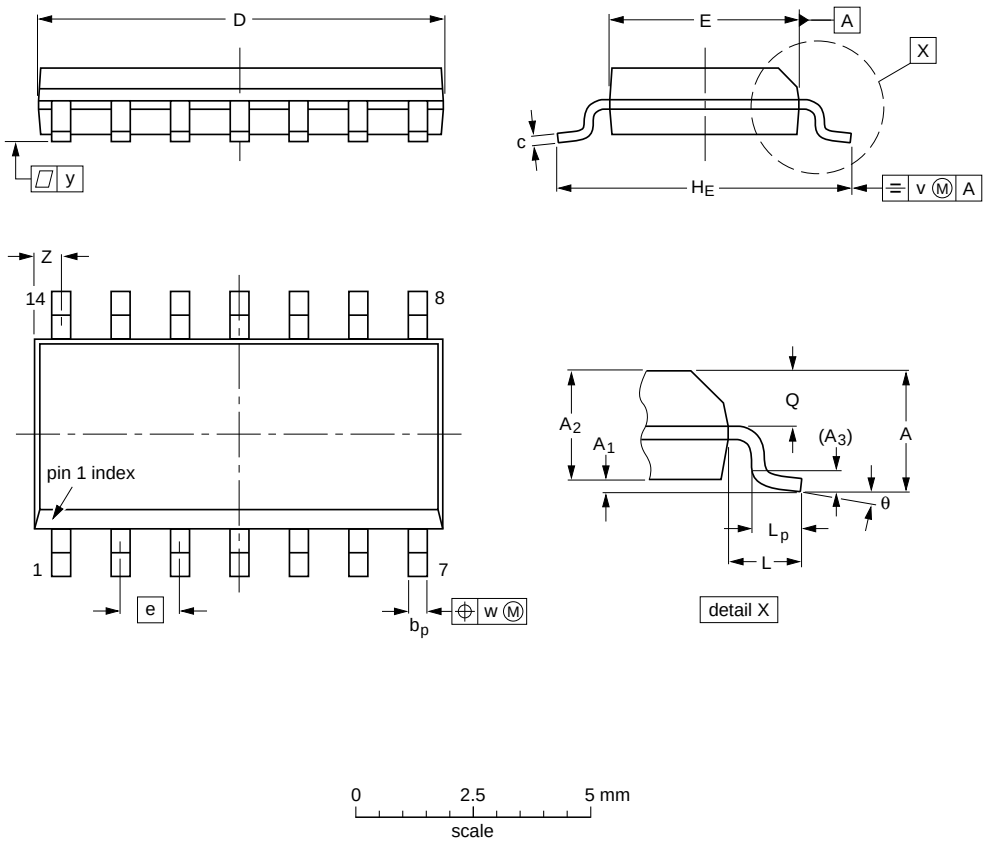
For 74AHC132-Q100: $f = \frac{1}{T} \approx \frac{1}{0.55 \times RC}$

For 74AHCT132-Q100: $f = \frac{1}{T} \approx \frac{1}{0.60 \times RC}$

Fig 12. Relaxation oscillator

15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

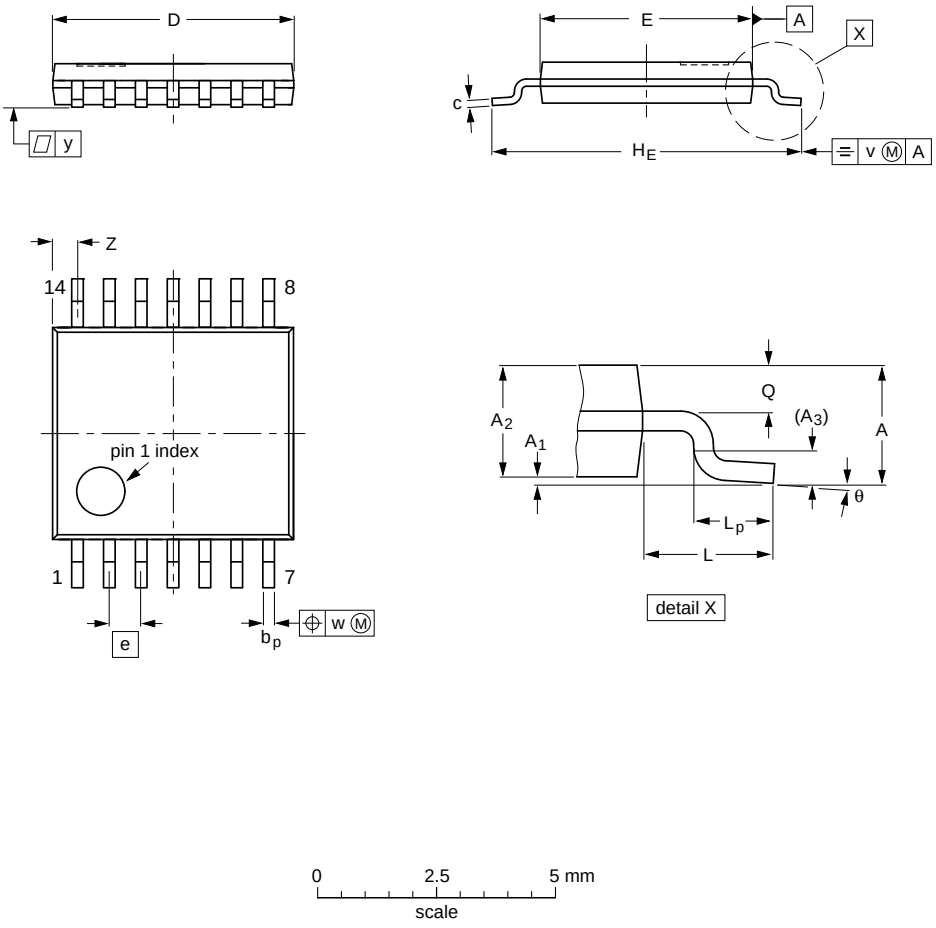
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

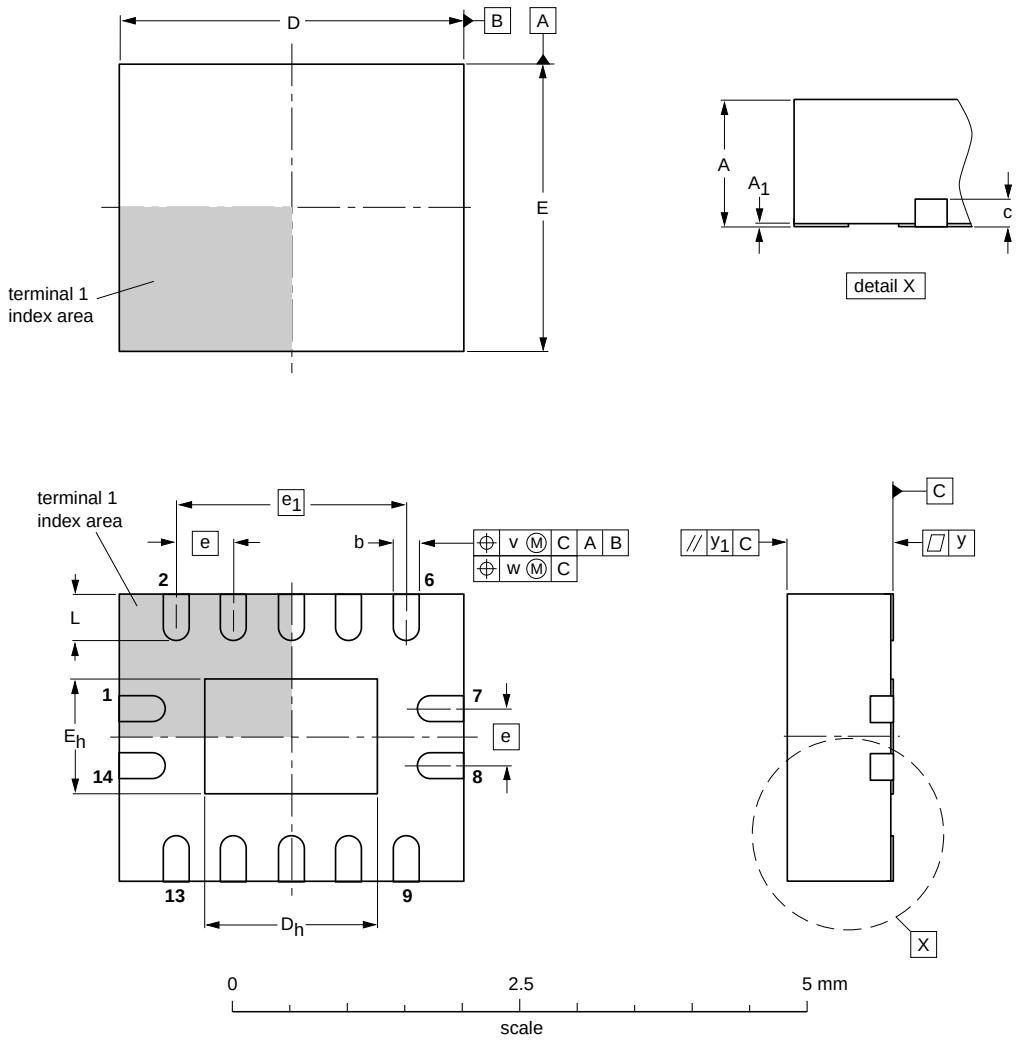
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 15. Package outline SOT762-1 (DHVQFN14)

16. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT132_Q100 v.1	20131108	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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20. Contents

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