500mA Current Limited Power Switch

Check for Samples: LM34904

FEATURES

- **Input Voltage of 2.8V to 5.3V**
- **0.5A Maximum Switch Current**
- **0.4Ω Typical Total On-Resistance**
- **Load Detection**
- **Enable/Disable**
- **Switch On Indicator**
- **Peak Current Limit**
- **Thermal Shutdown**
- **6-bump Thin DSBGA Package**

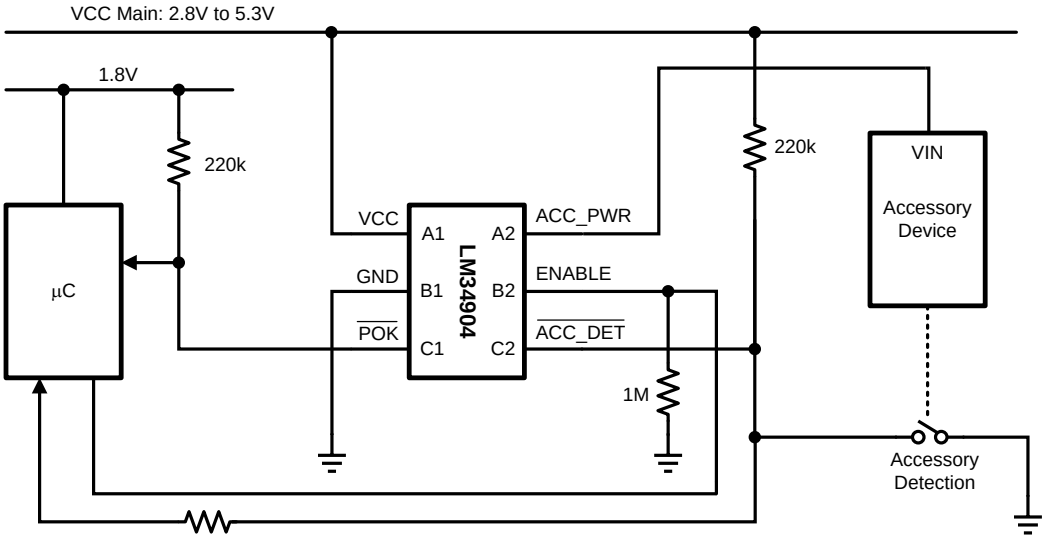
APPLICATIONS

- **Handsets, Tablets, Notebooks**
- **Portable Devices**

DESCRIPTION

The LM34904 is a 0.5A PFET switch used to control the input voltage of electronic devices. It is easily integrated into system designs that have a 2.8V to 5.3V voltage rail. Besides the 0.4Ω PFET switch, the LM34904 can be enabled or disabled by a logic signal. The IC monitors the presence of a downstream electronic device via a dedicated pin to decide whether to turn on the PFET switch. A power good signal generated by the IC can be used by system control to determine the status of the switch. The LM34904 also provides over-current and over-temperature protection. The IC comes in a tiny 6-bump thin DSBGA package.

Typical Application Circuit



Connection Diagram

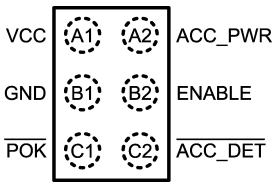


Figure 1. Top View - 6-Bump Thin DSBGA Package
See Package Number YFQ

PIN DESCRIPTIONS

Name	Pin Number	Function
VCC	A1	Power input of the PFET switch. It also provides power to the entire IC. Connect to the voltage rail that the accessory device is expected to work off.
GND	B1	Common Ground (device substrate).
$\overline{\text{POK}}$	C1	Open-drain PFET status indicator. When the PFET is off, this pin floats. When PFET is on, it is grounded.
$\overline{\text{ACC\_DET}}$	C2	Pull this pin low to tell the IC that the downstream accessory device is plugged in.
ENABLE	B2	When this pin is low, the PFET will be turned off and $\overline{\text{POK}}$ will be open-drained. Current limit circuitry will also be disabled. The IC will be in a low-power state. This pin should be held low until VCC is established to ensure proper initial state of internal logic. When ENABLE is high, the PFET switch will be allowed to turn on.
ACC_PWR	A2	Power output terminal of the PFET switch. Connect to input rail of accessory device.

Truth Table(1)

Input					Output	
ENABLE	**$\overline{\text{ACC\_DET}}$**	**Current Limit Detected**	**T_J Limit Exceeded**	**2.8V < VCC < 5.3V**	**PFET Switch Status**	**$\overline{\text{POK}}$**
0	x	No	No	Yes	Open	Open Drain
x	1	No	No	Yes	Open	Open Drain
0 to 1	0	No	No	Yes	On	Grounded
0 to 1	0	Yes	No	Yes	Current Limited	Grounded
x	x	x	Yes	2.2V < VCC < 5.3V	Open	Open Drain
0	x	x	No	2.2V < VCC < 2.8V	Open	Open Drain

(1) Note: "x" stands for "don't care".

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VCC	-0.3V to 6V
ENABLE, $\overline{POK}$, $\overline{ACC\_DET}$, ACC_PWR[3]	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility, Human Body Model[4]	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The voltages on these pins should never exceed VCC+0.3V.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-A114.

Operating Ratings

VCC Voltage[1]	2.8V to 5.3V
Junction Temperature (T_J), LM34904	-40°C to +85°C

(1) For VCC between 2.2V and 2.8V, if ENABLE is a logic low, the LM34904 will not turn on the PFET switch.

Electrical Characteristics

Unless otherwise stated, the following conditions apply: VCC = 3V. Limits in standard type are for T_J = 25°C only; limits in **boldfacetype** apply over the operating junction temperature (T_J) range. Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage, $\overline{ACC\_DET}$, ENABLE				**0.45**	V
V_{IH}	Input High Voltage, $\overline{ACC\_DET}$, ENABLE		**1.35**			V
V_{IHS}	Input Hysteresis, $\overline{ACC\_DET}$, ENABLE			55		mV
I_{LK}	Input Current, $\overline{ACC\_DET}$, ENABLE	$\overline{ACC\_DET}$, ENABLE between 0V and VCC			1	µA
I_{SD}	VCC Current in Shutdown Mode	V_{ENABLE} = 0V V_{VCC} = 5.3V		0.005	**1**	µA
I_Q	VCC Quiescent Current	V_{ENABLE} = 1.8V V_{VCC} = 5.3V, I_{ACC_PWR} = 0A		47	**100**	µA
R_{ON}	Total On Resistance Between VCC and ACC_PWR Pins	V_{VCC} = 2.8V to 5.3V I_{ACC_PWR} = 0.5A		0.4	**0.6**	Ω
I_{LK_ACC}	ACC_PWR Leakage Current When PFET is Off	V_{ACC_PWR} = 0V to VCC V_{VCC} = 5.3V V_{ENABLE} = 0V			1	µA
I_{LIMIT}	PFET Switch Current Limit	V_{VCC} = 2.8V to 5.3V V_{ACC_PWR} = 0V	**0.50**	0.59	**0.76**	A
V_{POK}	$\overline{POK}$ Current Sink Capability	$\overline{POK}$ asserted. 1mA sink current			0.4	V
I_{POK}	$\overline{POK}$ Leakage Current	$\overline{POK}$ de-asserted $V_{\overline{POK}}$ = 3.3V			1	µA
T_1	$\overline{ACC\_DET}$ Response Time	$\overline{ACC\_DET}$ rising to either PFET or $\overline{POK}$ FET turn-off		107		ns
T_2	ENABLE Response Time	ENABLE rising to either PFET or $\overline{POK}$ FET turn-on		10		µs
T_3	Minimum ENABLE Cycle Time[1]	$\overline{ACC\_DET}$ tied to ground. ENABLE logic high = 1.8V. VCC = 2.8V to 5.3V.		300		ns

(1) If ENABLE toggles low from a high state, it needs to stay low for at least T_3 long before toggling back to high. Otherwise the internal flip-flop may not be set and the PFET switch may not turn on.

Thermal Characteristics

Symbol	Description	Conditions	Typical Value	Unit
θ_{JA1}	Junction-to-Ambient Thermal Resistance	Mount device on a standard 4-layer 4" x 3" JEDEC board. Apply known amount of power to the package. Measure junction temperature and surrounding air temperature. No air flow. Refer to JESD51-7 for more information.	104	°C/W
θ_{JA2}	Junction-to-Ambient Thermal Resistance	Mount device on a 2-layer 2.19" x 2.9" board. Copper thickness is 1 oz per layer. No air flow. Power dissipation is 0.5W.	136	°C/W
T_{SD}	Thermal Shutdown Threshold	Raise T_J from below 120°C until $\overline{POK}$ is de-asserted. No load is connected at ACC_PWR.	135	°C

Typical Performance Characteristics

Unless indicated otherwise, VCC = 3.0V and T_J = 25°C.

Total ON Resistance vs Temperature

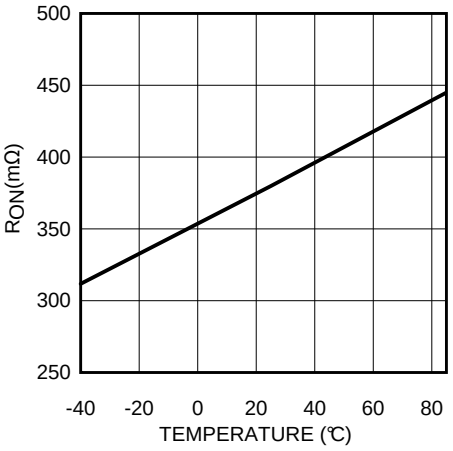


Figure 2.

Total ON Resistance vs Switch Current

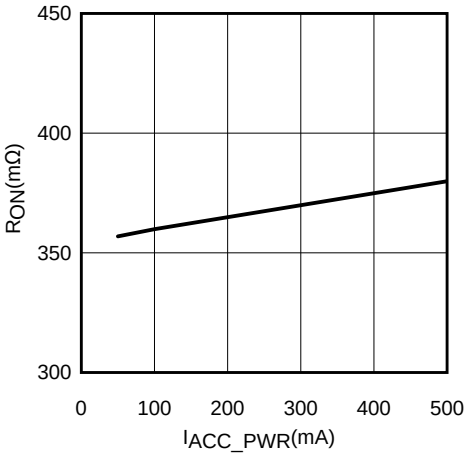


Figure 3.

Total ON Resistance vs VCC

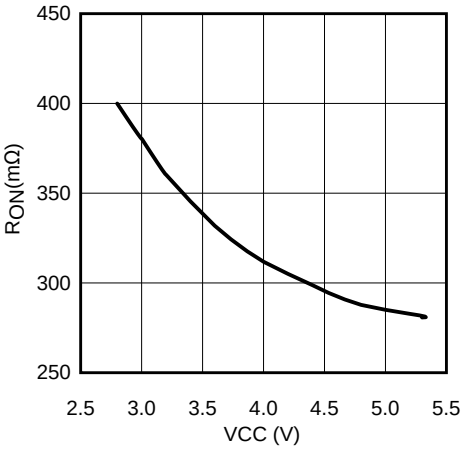


Figure 4.

Current Limit vs Temperature

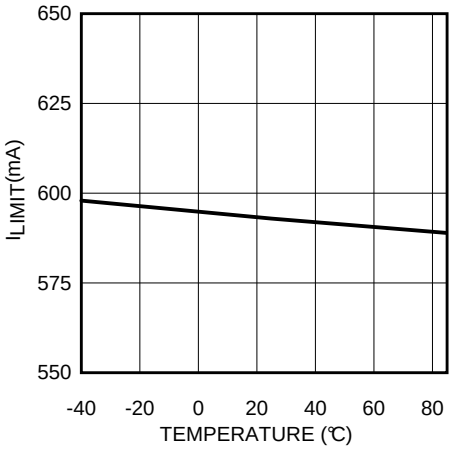


Figure 5.

Input Logic High Threshold vs Temperature

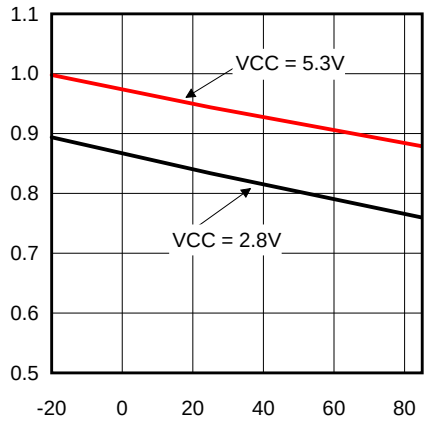


Figure 6.

Input Logic Low Threshold vs Temperature

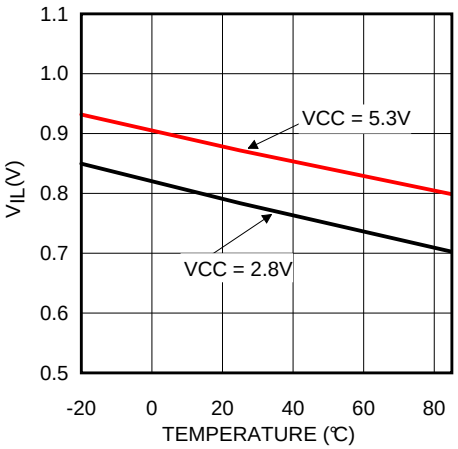
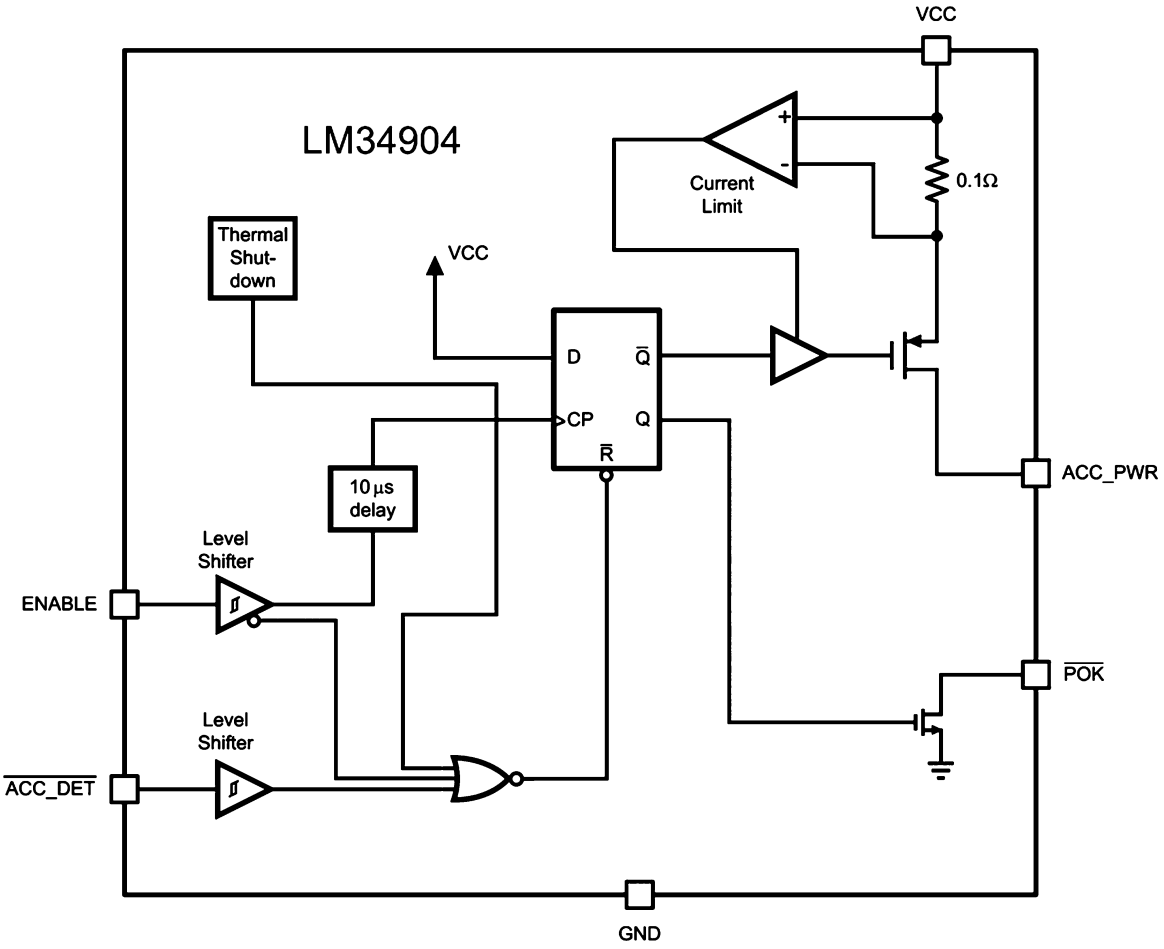


Figure 7.

BLOCK DIAGRAM



APPLICATION HINTS

To turn on the PFET switch, both the ENABLE and the $\overline{\text{ACC\_DET}}$ pins need to be asserted. In addition, $\overline{\text{ACC\_DET}}$ needs to be asserted no later than the rising edge of the ENABLE signal. De-assertion of either the ENABLE or the $\overline{\text{ACC\_DET}}$ will result in turned-off PFET switch and de-asserted $\overline{\text{POK}}$ signal.

To prevent a glitch in the otherwise asserted $\overline{\text{ACC\_DET}}$ from keeping the FETs turned off, it is a good practice to cycle the ENABLE following every falling edge in the $\overline{\text{ACC\_DET}}$ signal. When cycling the ENABLE, make sure it stays low for at least T_3 long before toggling back high. If ENABLE logic high level is not 1.8V, make sure ENABLE stays low for at least 1µs.

When laying out the PCB, try to keep the ENABLE and $\overline{\text{ACC\_DET}}$ traces as short as possible and away from noisy traces.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM34904ITM/NOPB	ACTIVE	DSBGA	YFQ	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L	Samples
LM34904ITMX/NOPB	ACTIVE	DSBGA	YFQ	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

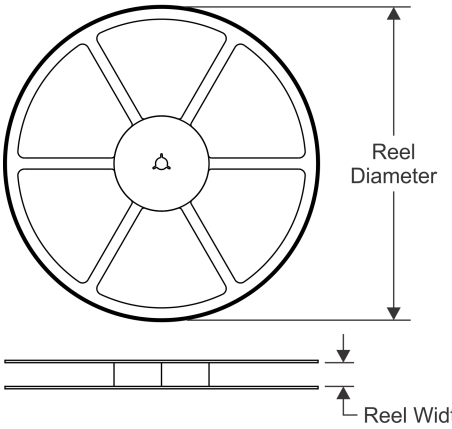
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

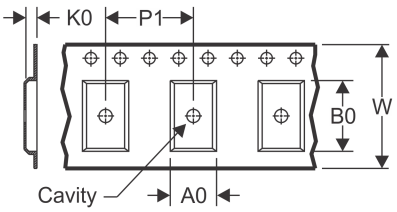
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

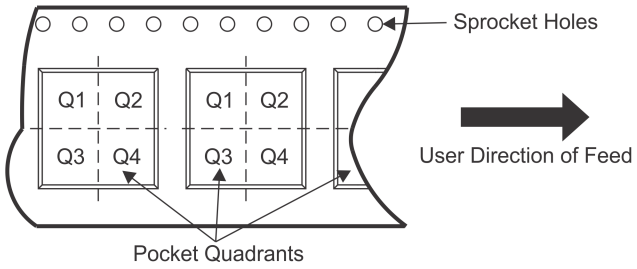


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

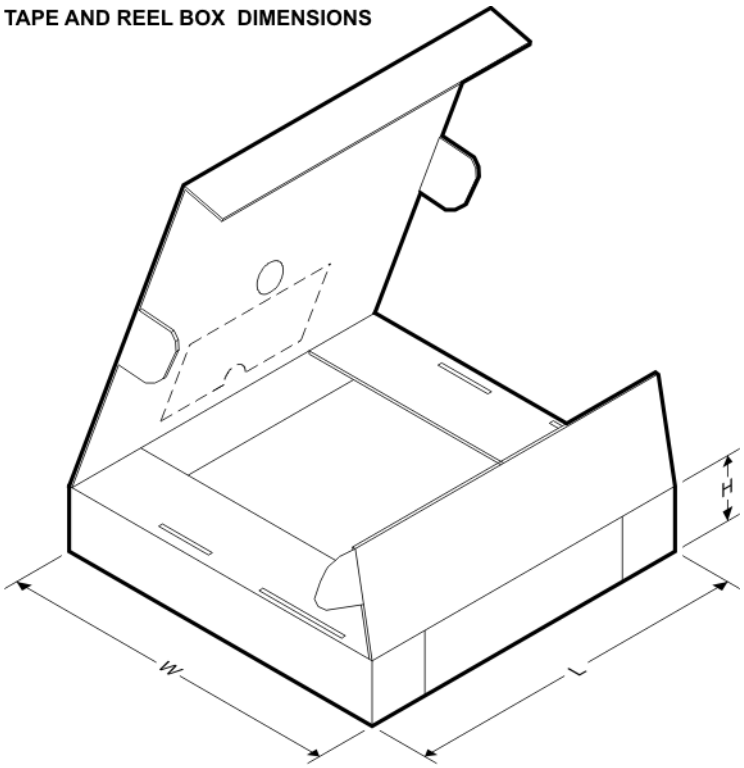
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM34904ITM/NOPB	DSBGA	YFQ	6	250	178.0	8.4	0.89	1.3	0.7	4.0	8.0	Q1
LM34904ITMX/NOPB	DSBGA	YFQ	6	3000	178.0	8.4	0.89	1.3	0.7	4.0	8.0	Q1

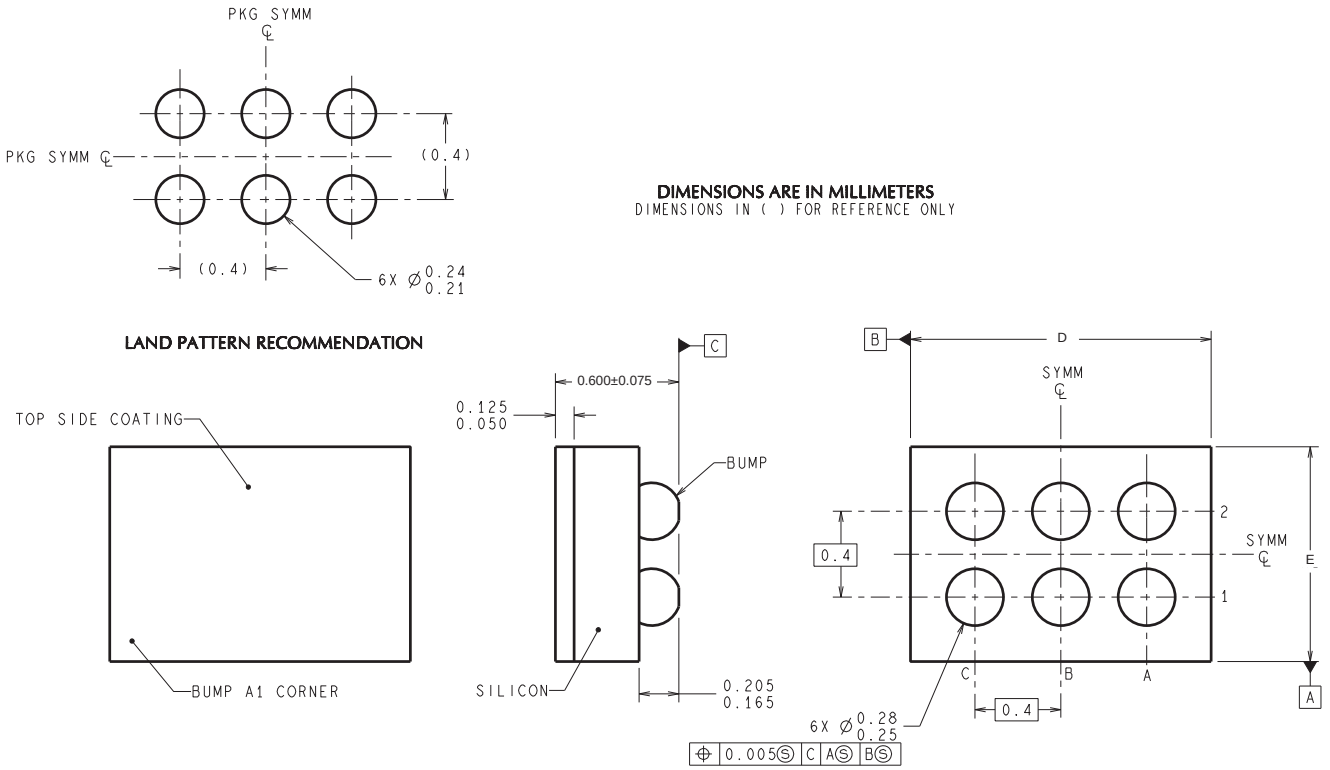
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM34904ITM/NOPB	DSBGA	YFQ	6	250	210.0	185.0	35.0
LM34904ITMX/NOPB	DSBGA	YFQ	6	3000	210.0	185.0	35.0

YFQ0006



TMD06XXX (Rev B)

D: Max = 1.24 mm, Min = 1.18 mm

E: Max = 0.84 mm, Min = 0.78 mm

4215075/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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