Complementary Switch FET Drivers

Check for Samples: UC1714, UC1715, UC2714, UC2715, UC3714, UC3715

FEATURES

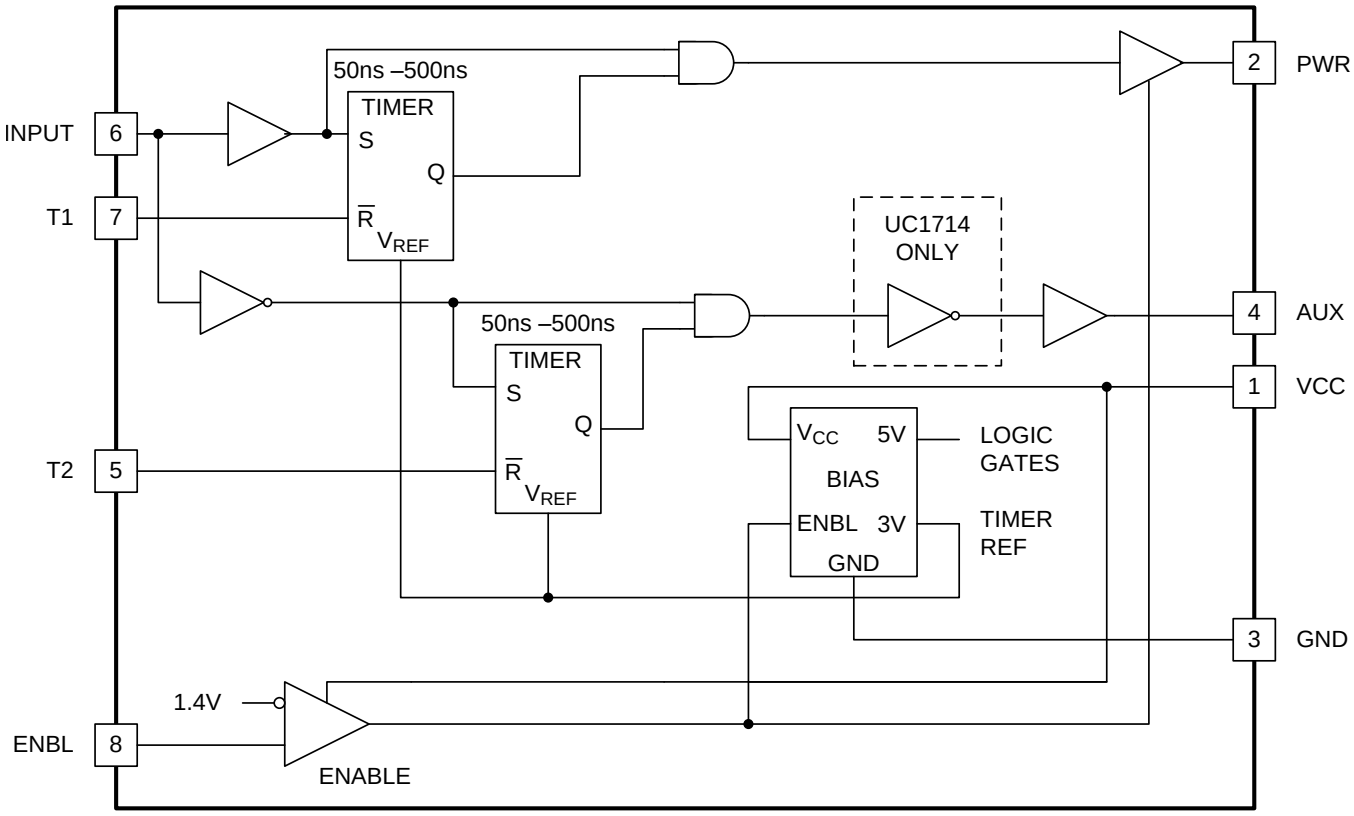
- **Single Input (PWM and TTL Compatible)**
- **High-Current Power FET Driver, 1-A Source and 2-A Sink**
- **Auxiliary Output FET Driver, 0.5-A Source and 1-A Sink**
- **Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50 to 500-ns**
- **Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output**
- **Switching Frequency to 1 MHz**
- **Typical 50-ns Propagation Delays**
- **ENBL Pin Activates 220-µA Sleep Mode**
- **Power Output is Active-Low in Sleep Mode**
- **Synchronous Rectifier Driver**

DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true-zero voltage-sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and interface with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

BLOCK DIAGRAM



Pin numbers refer to J, N and D packages.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)(2)

			MIN	MAX	UNIT
	Auxiliary Driver IOH	continuous		–100	mA
		peak		–500	mA
	Auxiliary Driver IOL	continuous		200	mA
		peak		1	A
	Input Voltage Range (INPUT, ENBL)		–0.3	20	V
	Power Driver IOH	continuous		–200	mA
		peak		–1	A
	Power Driver IOL	continuous		400	mA
		peak		2	A
V_{CC}	Supply voltage			20	V
	Lead Temperature (Soldering 10 seconds)			300	°C
	Operating Junction Temperature(3)			150	°C
	Storage Temperature Range		–65	150	°C

(1) Consult the Packaging Section at the end of this datasheet for thermal limitations and specifications of packages.
(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC} = 15 V, ENBL ≥ 2 V, R_T1 = 100 kΩ from T1 to GND, R_T2 = 100 kΩ from T2 to GND, and −55°C < T_A < 125°C for the UC1714 and UC1715, –40°C < T_A < 85°C for the UC2714 and UC2715, and 0°C < T_A < 70°C for the UC3714 and UC3715, T_A = T_J

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall						
V_{CC}			7		20	V
I_{CC}	Nominal	ENBL = 2 V		18	24	mA
	Sleep mode	ENBL = 0.8 V		200	300	µA
Power Driver (PWR)						
	Pre turn-on PWR output, low	V_{CC} = 0 V, I_{OUT} = 10 mA, ENBL at 0.8 V		0.3	1.6	V
V_{PWR}	PWR output low, sat.	INPUT = 0.8 V, I_{OUT} = 40 mA		0.3	0.8	V
		INPUT = 0.8 V, I_{OUT} = 400 mA		2.1	2.8	
V_{CC} − V_{PWR}	PWR output high, sat.	INPUT = 2 V, I_{OUT} = −20 mA		2.1	3	V
		INPUT = 2 V, I_{OUT} = −200 mA		2.3	3	
	Rise time	C_L = 2200 pF		30	60	ns
	Fall time	C_L = 2200 pF		25	60	ns
	T1 Delay, AUX to PWR	INPUT rising edge, R_T1 = 10 kΩ(1)	20	35	80	ns
		INPUT rising edge, R_T1 = 100 kΩ(1)	350	500	700	
	PWR Prop Delay	INPUT falling edge, 50%(2)		35	100	ns
Auxiliary Driver (AUX)						
V_{AUX}	AUX output low, sat.	V_{IN} = 2 V, I_{OUT} = 20 mA		0.3	0.8	V
		V_{IN} = 2 V, I_{OUT} = 200 mA		1.8	2.6	
V_{CC} – V_{AUX}	AUX output high, sat.	V_{IN} = 0.8 V, I_{OUT} = –10 mA		2.1	3	V
		V_{IN} = 0.8 V, I_{OUT} = –100 mA		2.3	3	
	Rise Time	C_L = 1000 pF		45	60	ns

(1) T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.
(2) Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

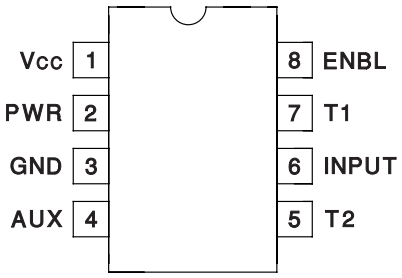
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, V_{CC} = 15 V, ENBL ≥ 2 V, R_T1 = 100 kΩ from T1 to GND, R_T2 = 100 kΩ from T2 to GND, and −55°C < T_A < 125°C for the UC1714 and UC1715, –40°C < T_A < 85°C for the UC2714 and UC2715, and 0°C < T_A < 70°C for the UC3714 and UC3715, $T_A = T_J$

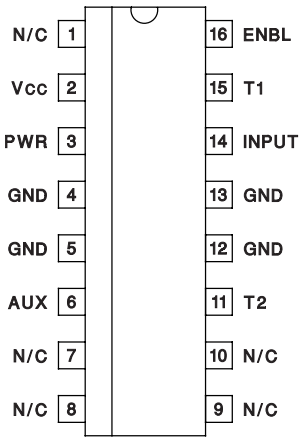
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Fall Time	C_L = 1000 pF		30	60	ns
	T2 Delay, PWR to AUX	INPUT falling edge, R_T2 = 10 kΩ (1)	20	50	80	ns
		INPUT falling edge, R_T2 = 100 kΩ (1)	250	350	550	
	AUX Prop Delay	INPUT rising edge, 50% (2)		35	80	ns
Enable (ENBL)						
	Input Threshold		0.8	1.2	2	V
I_{IH}	Input Current	ENBL = 15 V		1	10	µA
I_{IL}	Input Current	ENBL = 0 V		–1	–10	µA
T1						
	Current Limit	T1 = 0 V		–1.6	–2	mA
	Nominal Voltage at T1		2.7	3	3.3	V
	Minimum T1 Delay	T1 = 2.5 V (1)		40	70	ns
T2						
	Current Limit	T2 = 0 V		–1.2	–2	mA
	Nominal Voltage at T2		2.7	3	3.3	V
	Minumum T2 Delay	T2 = 2.5 V (1)		50	100	ns
Input (INPUT)						
	Input Threshold		0.8	1.4	2	V
I_{IH}	Input Current	INPUT = 15 V		1	10	µA
I_{IL}	Input Current	INPUT = 0 V		–5	–20	µA

DEVICE INFORMATION

DIL-8, SOIC-8; J or N, D Packages
(TOP VIEW)



SOIC-16; DP Package
(TOP VIEW)



PIN DESCRIPTIONS

AUX The AUX switches immediately at the rising edge of INPUT'but waits through the T2 delay after the falling edge of INPUT before switching. AUX is capable of sourcing 0.5 A and sinking 1 A of drive current. See the Time Relationships diagram below (Figure 1) for the differences between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.

ENBL The ENBL input switches at TTL logic levels (approximately 1.2 V), and the input range is from 0 to 20 V. The ENBL input places the device into sleep mode when it is a logical low. The current into VCC during the sleep mode is typically 220 µA.

GND This is the reference pin for all input voltages and the return point for all device currents. GND carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

INPUT The input switches at TTL logic levels (approximately 1.4 V) but the allowable range is from 0 to 20 V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.
Note that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR The PWR output waits for the T1 delay after the rising edge of INPUT before switching on, but switches off immediately at the falling edge of INPUT'(neglecting propagation delays). This output is capable of sourcing 1 A and sinking 2 A of peak gate-drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≤ 0.8V regardless of the voltage of VCC.

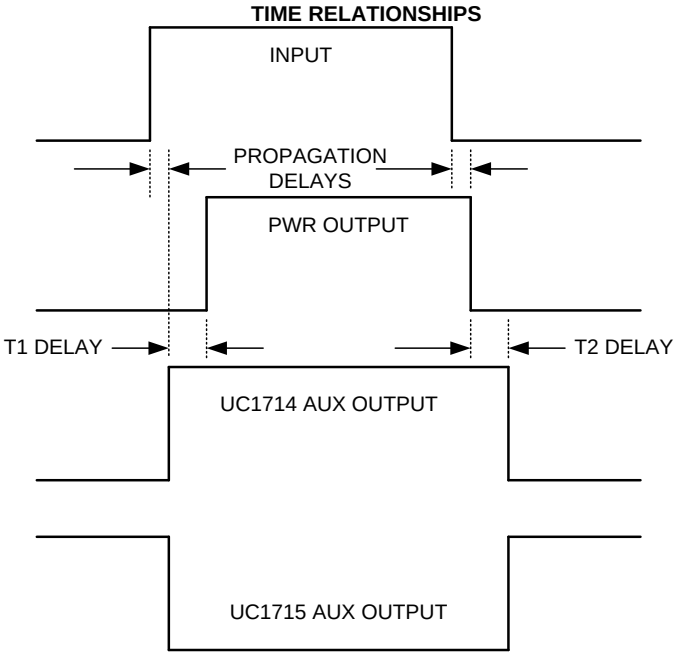
T1 A resistor to ground programs the time delay between the AUX switch turnoff and PWR turnon.

T2 This pin functions in the same way as T1 but controls the time delay between PWR turnoff and activation of the AUX switch.

T1, T2 The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3 V and the current is internally limited to 1 mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but because the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the TYPICAL CHARACTERISTICS curves (see Figure 2). Either or both pins are alternatively used for voltage sensing in lieu of delay programming, which is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

VCC The V_{CC} input range is from 7 to 20 V. This pin must be bypassed with a capacitor to GND consistent with peak load current demands.

TYPICAL CHARACTERISTICS



(2) T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.

Figure 1.

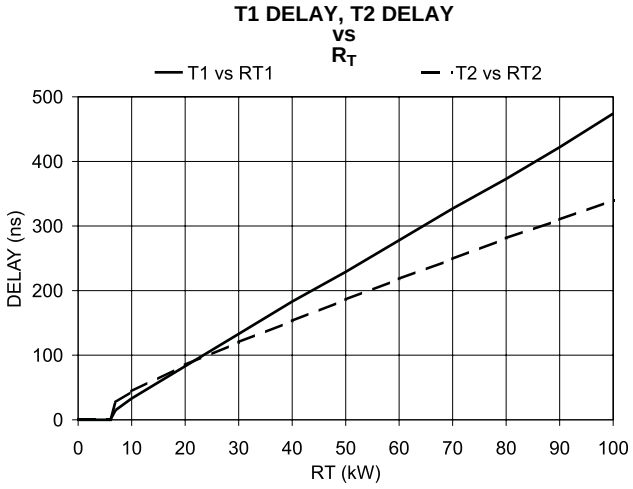


Figure 2.

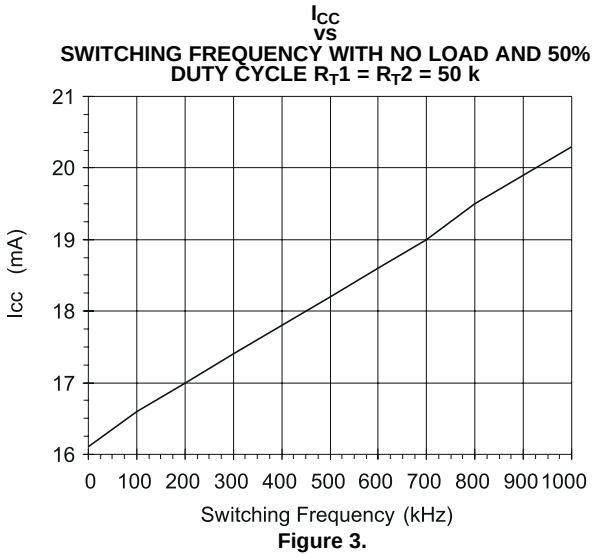


Figure 3.

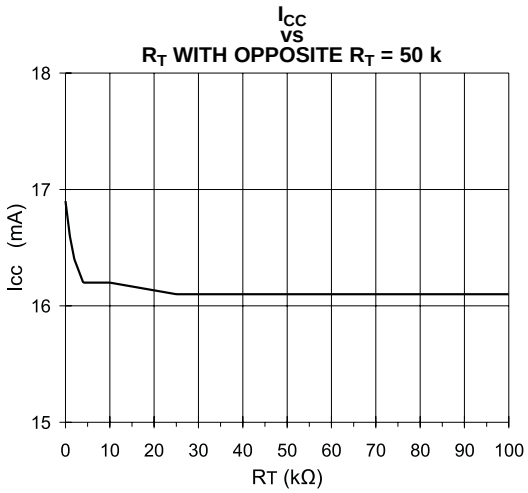


Figure 4.

TYPICAL CHARACTERISTICS (continued)

T1 DEADBAND vs TEMPERATURE AUX TO PWR

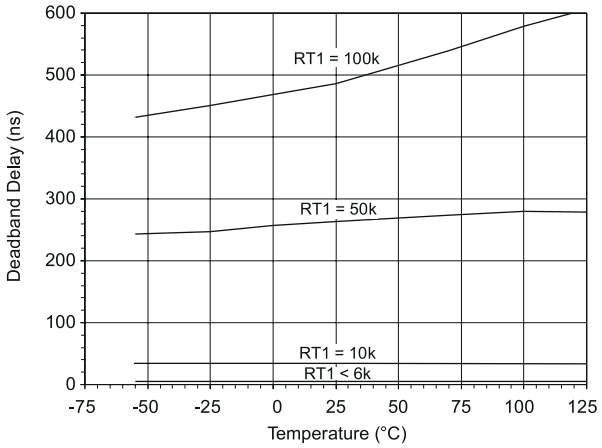


Figure 5.

T2 DEADBAND vs TEMPERATURE PWR TO AUX

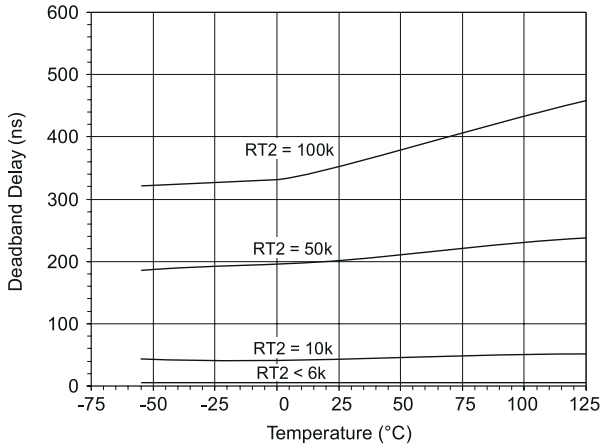


Figure 6.

TYPICAL APPLICATIONS

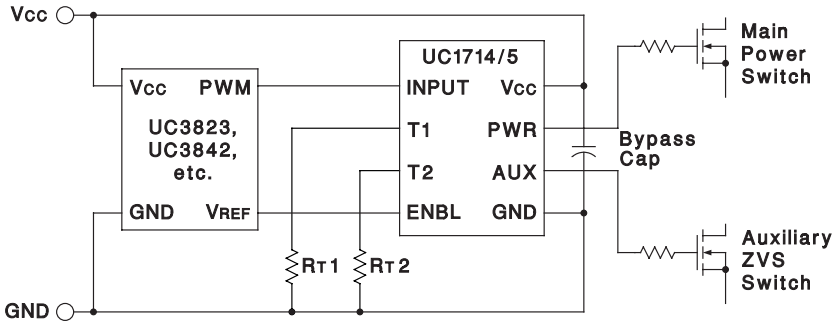


Figure 7. Typical Application With Timed Delays

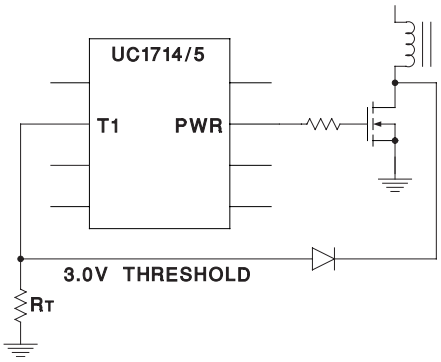
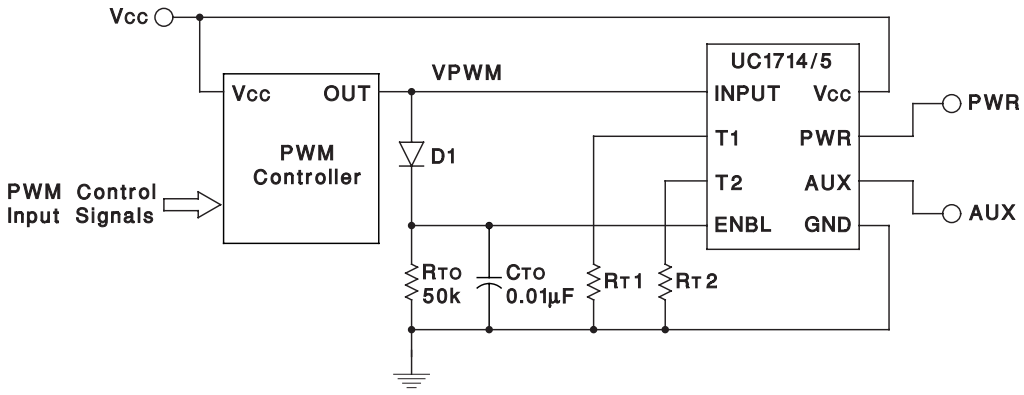


Figure 8. Using The Timer Input For Zero-Voltage Sensing



Wake-up occurs with the first pulse while turnoff is determined by the (RTO CTO) time constant.

Figure 9. Self-Actuated Sleep Mode With The Absence Of An Input PWM Signal

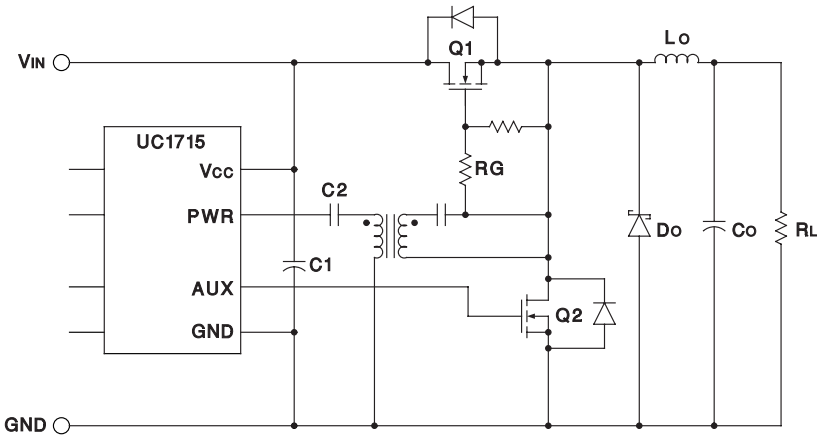
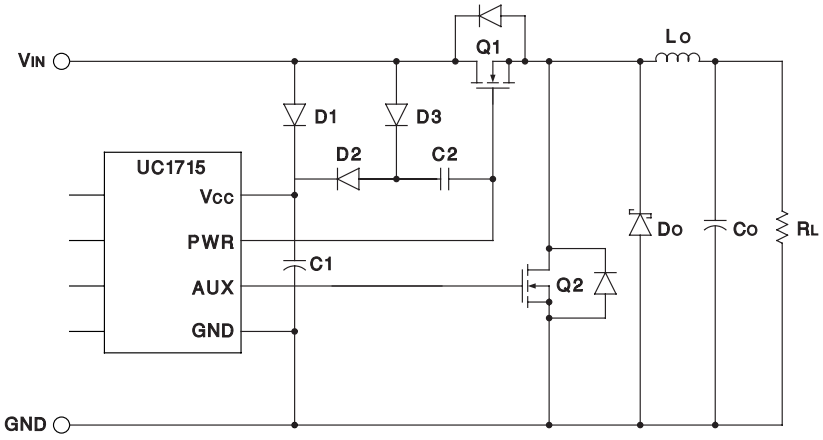
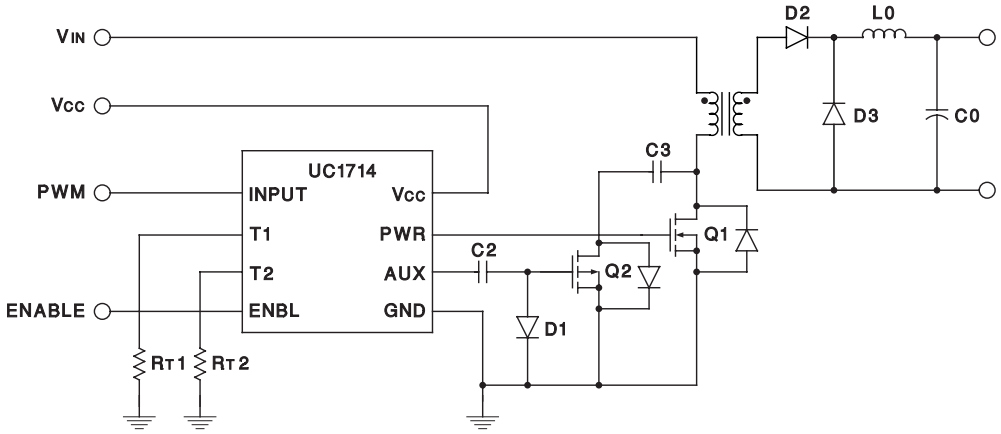


Figure 10. Using The UC1715 As A Complementary Synchronous Rectifier Switch Driver With N-Channel FETs



V_{IN} is limited to 10 V as V_{CC} rises to approximately $2V_{IN}$.

Figure 11. Synchronous Rectifier Application With A Charge Pump To Drive The High-Side N-Channel Buck Switch



With active reset provided by the UC1714 driving an N-channel switch (Q1) and a P-channel auxiliary switch (Q2).

Figure 12. Typical Forward Converter Topology

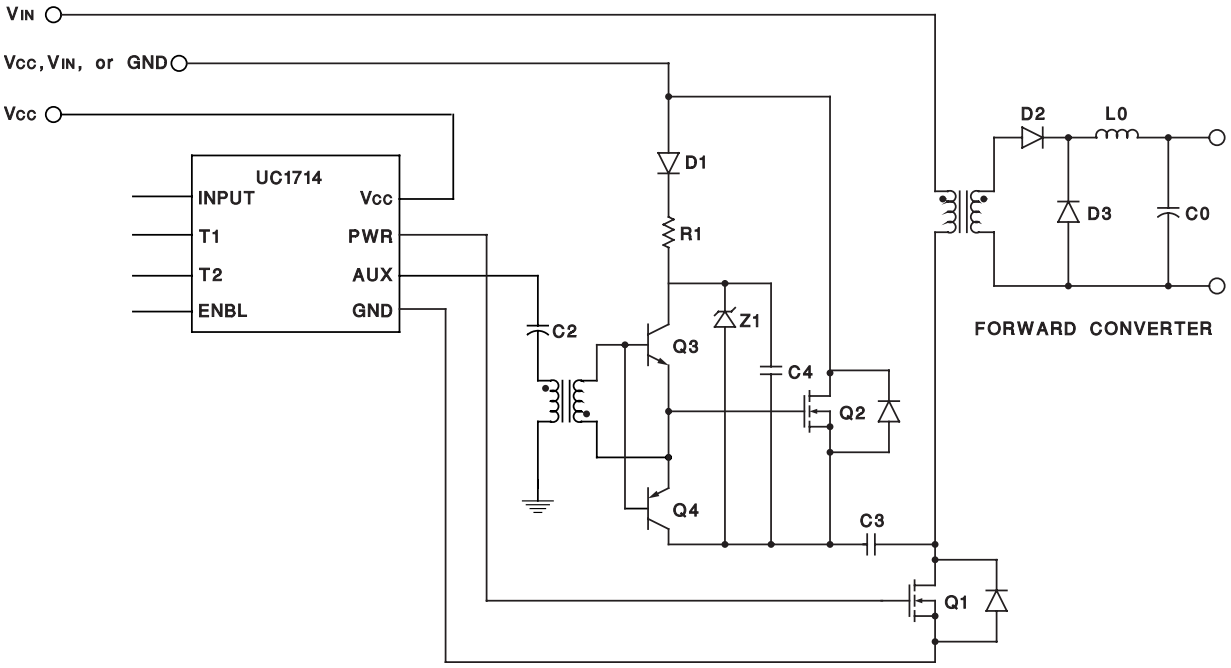


Figure 13. Using An N-Channel Active Reset Switch With A Floating Drive Command

REVISION HISTORY

Changes from Revision A (January 2002) to Revision B **Page**

- Added TI's general *Absolute Maximum Ratings* table note to end of Absolute Maximum table 2
- Changed ENBL ≥ 0.8V to ENBL ≤ 0.8V in PWR pin description 4
- Changed layout from Unitrode Products datasheet to TI datasheet 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2714DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2714DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2715D	Samples
UC2715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2715D	Samples
UC3714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3714D	Samples
UC3715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3715D	Samples
UC3715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3715D	Samples
UC3715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3715D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

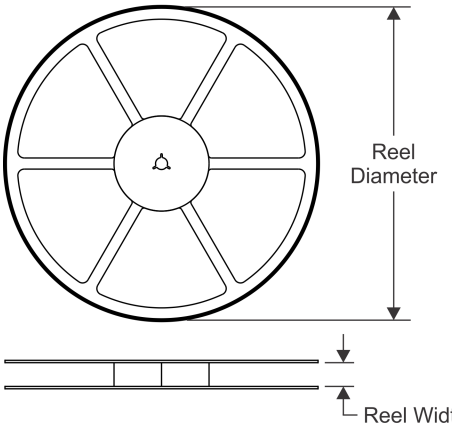
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

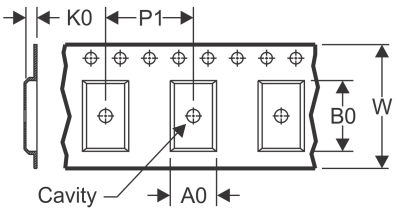
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

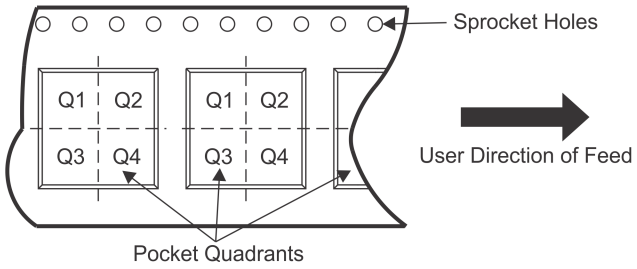


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

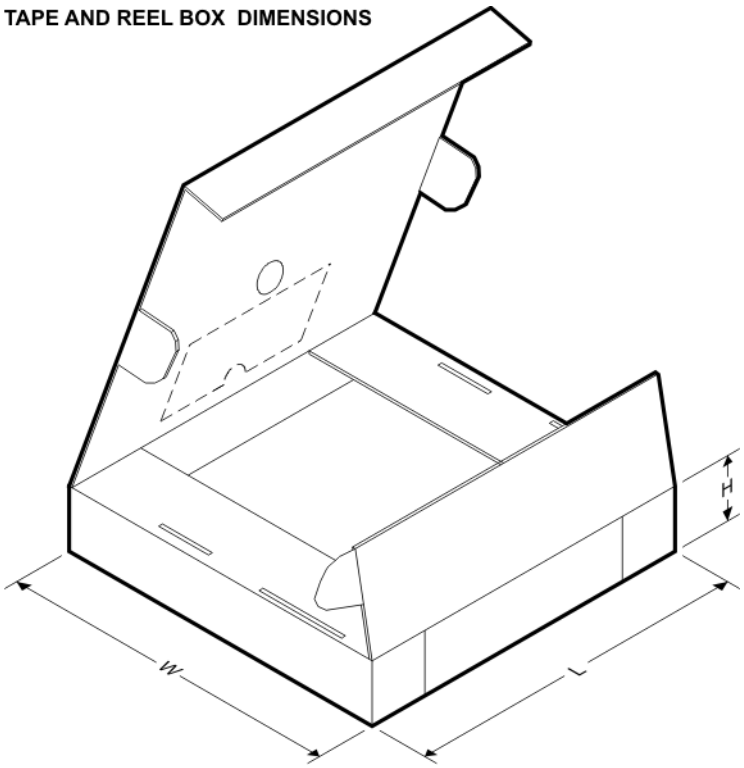
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2714DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2714DTR	SOIC	D	8	2500	367.0	367.0	35.0
UC2715DTR	SOIC	D	8	2500	367.0	367.0	35.0
UC3715DTR	SOIC	D	8	2500	367.0	367.0	35.0

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