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NCSD Applications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MC92460 Multichannel HDLC Controller.

The following topics are addressed:

Figure 1 shows a block diagram of the MC92460.
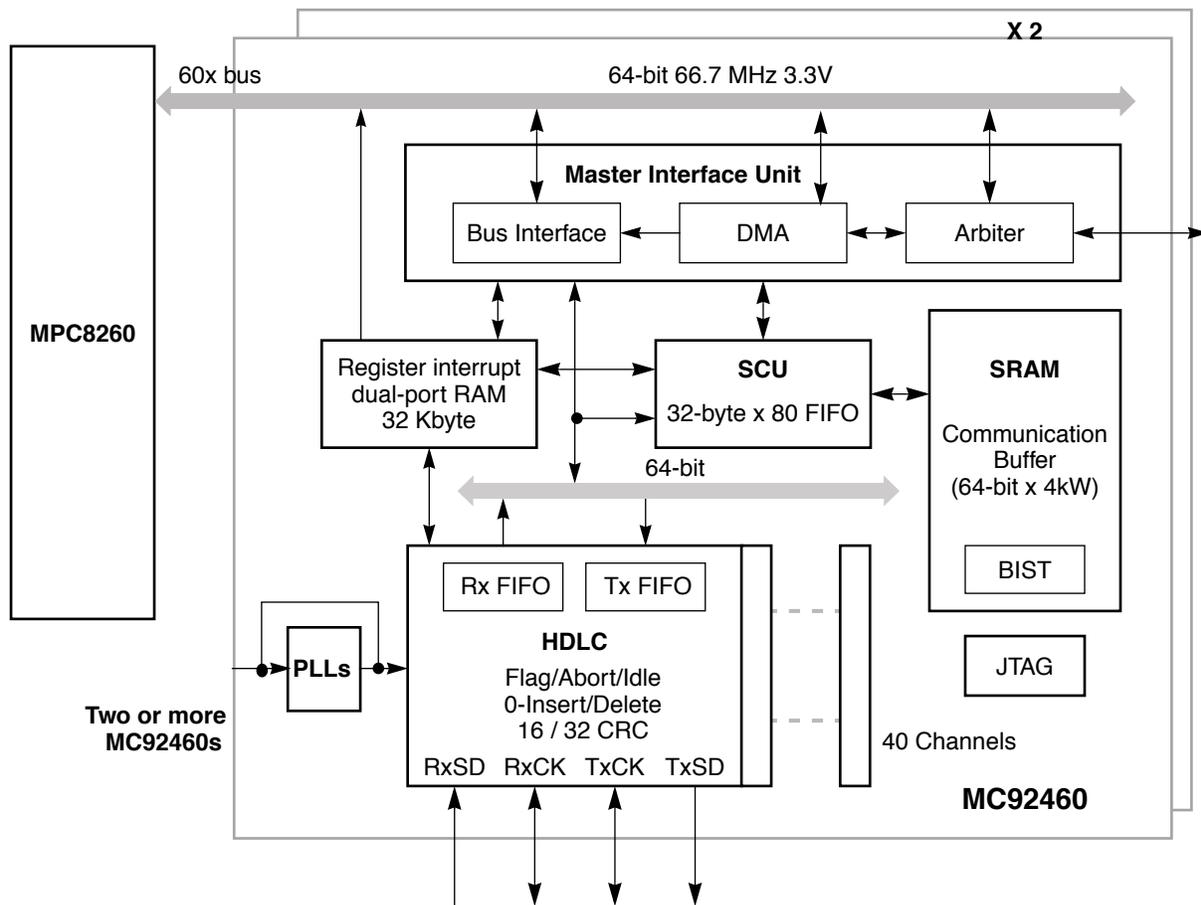

Figure 1. MC92460 Block Diagram

1.1   Features

The following is an overview of the MC92460 feature set:

- Channels
  - 40 full-duplex HDLC channels
  - Programmable channel assignment (any logical channel to any signal)
  - Each channel has a default of 64 buffer descriptors (Rx and Tx) but the number of buffer descriptors per channel is configurable
- Controllers
  - Maximum throughput of 1919 Mbps; individual controllers operate up to 66.7 Mbps
  - All communication controllers operate asynchronously
  - Programmable frame size (maximum 65,535 bytes)
  - Transparent memory access with internal memory controller
- 60x Bus
  - MC92460 directly connects with a 64-bit data and 32-bit address 60x bus
  - Supports 66.7 MHz 60x bus speed, with aggregate bandwidth of up to 1919 Mbps depending

on the type of main memory used

— Up to four MC92460's may be connected in parallel on the 60x bus

— Bus supports multiple master design

- Communication Buffers

  — Data Buffer

    – 256 Kbits on-chip memory for data buffers

    – 256 Kbit communication buffer can store up to 819 bytes per frame.

    – 80 channel virtual DMA functionality executes between off-chip memory and the communication buffer

  — BD Buffer

    – 32 Kbyte on-chip dual-port RAM for buffer descriptors

    – A total of 4096 buffer descriptors (2048 TxBD and 2048 RxBD)

- JTAG Support

  — Supports the IEEE1149.1 JTAG controller standard

- Power and Clocks

  — Supports single-beat and burst accesses

  — On-chip PLL for baud rate generator (maximum of 66.7 MHz)

  — Separate power supplies for core internal logic (1.8V) and for I/O (3.3V)

- Package

  — 480 pin TPGA, 1.27 mm pitch

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electical specifications and thermal characteristics for the MC92460.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MC92460. Table 1 shows the maximum electrical ratings.

Table 1. Maximum Temperatures and Voltages

Rating	Symbol	Value Name	Unit
Core supply voltage	VDD	-0.3 – 2.5	V
I/O supply voltage	VDDH	-0.3 – 3.6	V
Input voltage	VIN	GND-0.3 – 3.6	V
Junction temperature	Tj	120	^{o}C
Storage temperature range	T_{STG}	-55 – 150	^{o}C
Ambient temperature	T_A	-40 – 85	^{o}C

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.65 – 1.95	V
I/O supply voltage	VDDH	3.15 – 3.465	V
Input voltage	VIN	GND -0.3 – 3.6	V
Junction temperature	Tj	105	^{o}C

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Characteristics	Conditions	Symbol	Min	Max	Unit
Input high voltage		V_{IH}	2.0	3.465	V
Input low voltage		V_{IL}	GND	0.8	V
Input leakage current	V_{IN}=VDDH	I_{IN}	–	10	uA
HI-Z leakage current	V_{IN}=VDDH, GND	I_{OZ}	–10	+10	uA
Signal low input current	V_{IL}=0.8V	I_{IL}	–	60	uA
Signal high input current	V_{IH}=2.0V	I_{IH}	–	60	uA
Output high voltage	I_{OH}=-7.0mA	V_{OH}	2.4	-	V

Table 3. DC Electrical Characteristics (continued)

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Output low voltage • BR • BG • ABB • TS • A[0-31] • AP[0-3] • APE • TT[0-4] • TBST • TSIZ[0-2] • GBL • CI • WT • LBCLAIM • BTO • INT • TC[0-1] • AACK • ARTRY • DBG • DBWO • DBB • DH[0-31],DL[0-31] • DP[0-7] • DPE • DBDIS • TA • DRTRY • TEA	I_{OL}=7.0mA	V_{OL}		0.4	V
Output low voltage • Rx CLK[0-39] • Tx CLK[0-39] • Tx SD[0-39] • TDO • SBG • SDBG • SBR • SIRQ • CS0 • CS1 • CS2	I_{OL}=5.0mA	V_{OL}		0.4	V

1.2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Maximum Temperatures and Voltages

Characteristics	Symbol	Thermal Resistance Value	Unit	Air Flow
Thermal resistance for 480 TBGA	θ_{JA}	10.48	^{o}C/W	0 LFM
		8.61	^{o}C/W	100 LFM
		7.78	^{o}C/W	200 LFM
		6.89	^{o}C/W	400 LFM
		5.52	^{o}C/W	800 LFM

LFM = Linear Feet per Minute

1.2.3 Power Considerations

The average chip-junction temperature, Tj, can be obtained from the following:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where

θ_{JA} = package thermal resistance, junction to ambient, ^{o}C/W

T_A = ambient temperature, ^{o}C

Power equations are the following:

$$P_D = P_{VDD} + P_{VDDH} = \text{chip total power dissipation, W}$$
$$P_{VDD} = I_{VDD} \times VDD = \text{chip core power, W}$$

$$P_{VDDH} = I_{VDDH} \times VDDH$$

= user-determined power dissipation on input/output pins, W

1.2.4 Power Dissipation

Table 5 describes maximum chip core power dissipation.

Table 5. Maximum Core Power Dissipation (PVDD)

VDD(V)	SYSCLK Frequency (MHz)	I_{VDD} (mA)	P_{VDD} (mW)	P_{VDDH}(mW)
1.95	66.7	650	980	920

1.2.5 AC Specifications

These AC specifications are target specifications.

1.2.5.1 SYSCLK Timing

Table 6 shows the system clock timing.

Table 6. Clock Timing

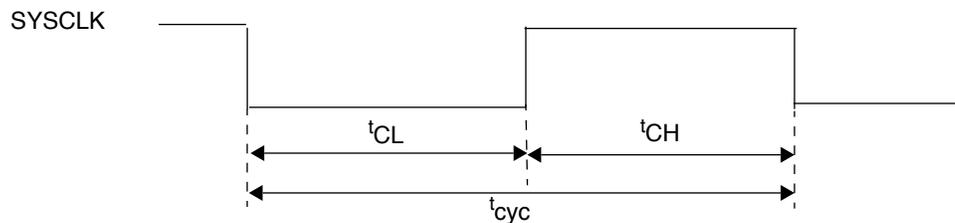| Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	60.0	66.7	MHz
Clock period		15.0	16.7	nS
Clock pulse width	t_{CL}, t_{CH}	7	8	nS
SYSCLK input high voltage	V_{IHC}	2.4	3.465	V
SYSCLK input low voltage	V_{ILC}	GND	0.4	V
SYSCLK Jitter			±200	pS

Figure 2 shows the SYSCLK.

Figure 2. SYSCLK

1.2.5.2 EXCLK Timing

Table 7 shows the external clock timing.

Table 7. Clock Timing

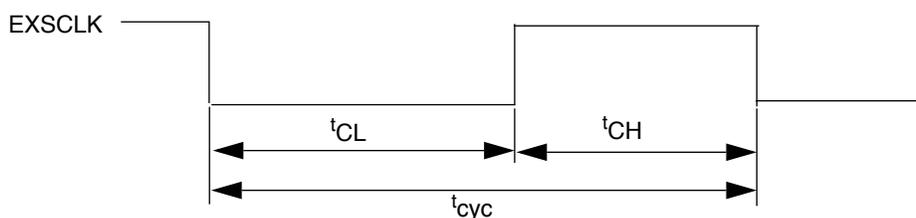| Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	14.0	16.0	MHz
Clock duty		40	60	%
Clock Pulse width	t_{CL}, t_{CH}	25	42.8	nS
EXCLK input high voltage	V_{IHC}	2.4	3.465	V
EXCLK input low voltage	V_{ILC}	GND	0.4	V
EXCLK Jitter			±200	pS

Figure 3 shows the EXCLK.

Figure 3. EXCLK

1.2.5.3 AC Timing

Figure 4 shows the HDLC external clock with polarity not inverted. All time specifications were measured at expected load capacitance C_L=8pF.
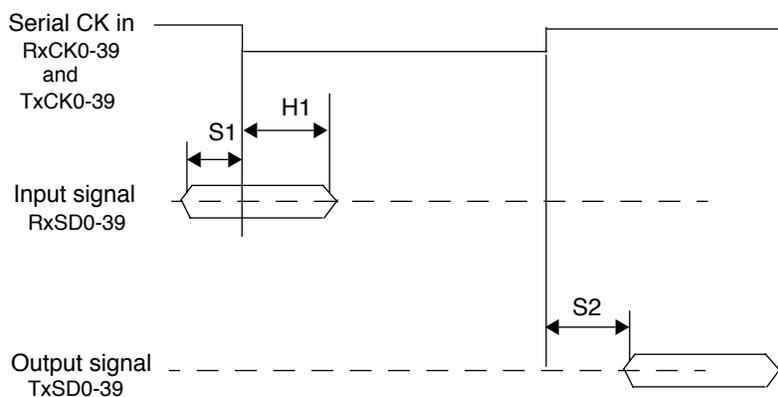

Figure 4. HDLC External Clock

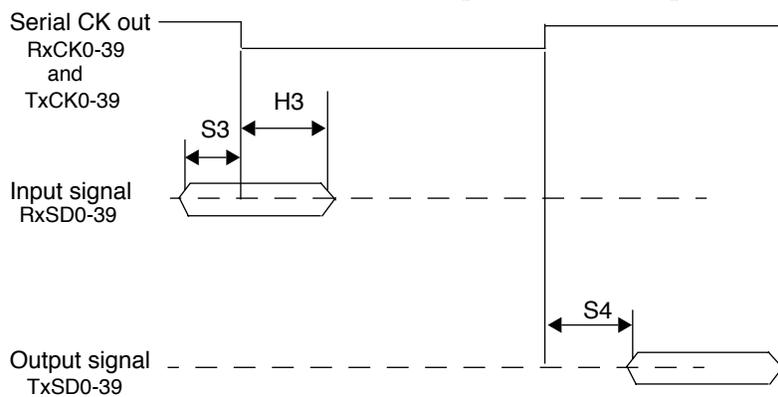Figure 5 shows an HDLC internal clock (TxCK/RxCK output mode) whose polarity is not inverted.

Figure 5. HDLC Internal Clock

Table 8 shows the AC electrical characteristics. The frequency is 20 MHz.

Table 8. AC Electrical Characteristics

Spec Num	Characteristic	Min	Max	Unit
S1	HDLC input- external clock setup time	2		nS
H1	HDLC input -external clock hold time	1		nS
S2	HDLC output- external clock setup time		14	nS
S3	HDLC input- internal clock setup time	12		nS
H3	HDLC input- internal clock hold time	0		nS
S4	HDLC output- internal clock setup time		4	nS

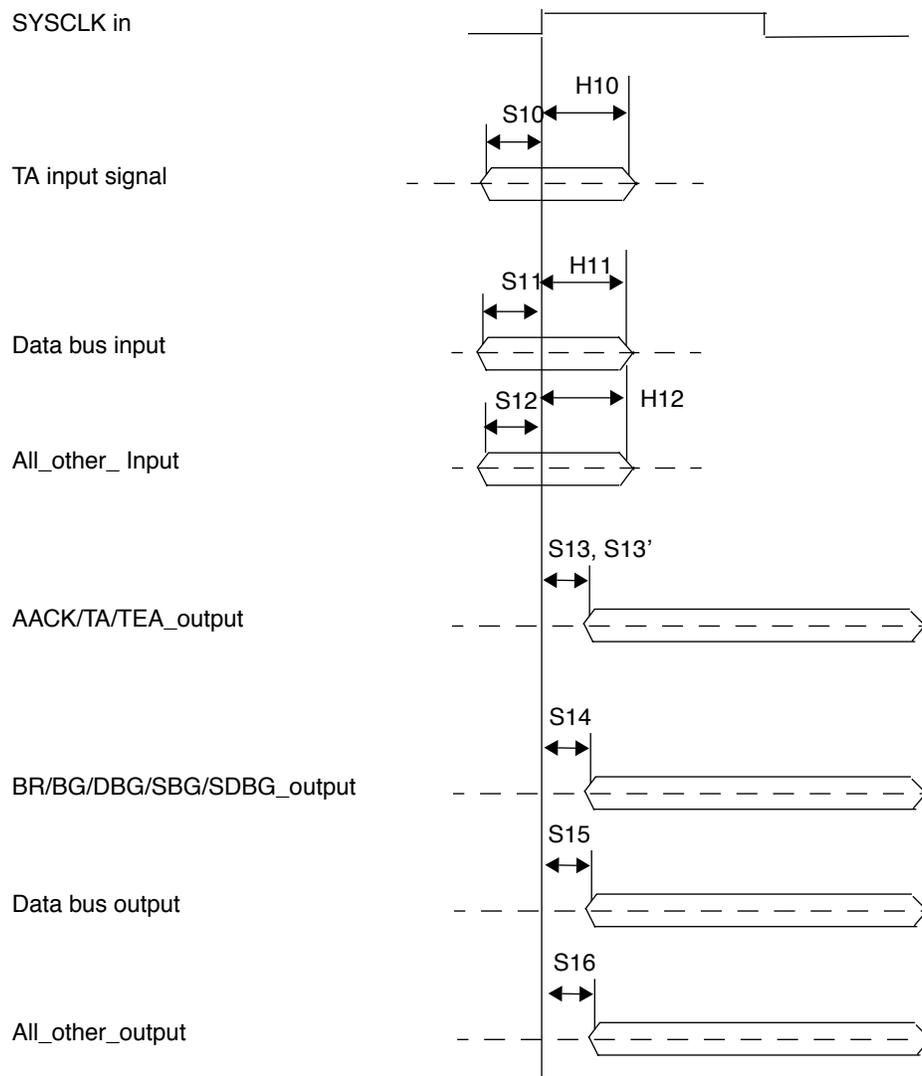Figure 6 shows the interaction of several bus signals.

Figure 6. Bus Signals

Table 9 shows the bus signal I/O characteristics. The frequency is 20 MHz.

Table 9. Bus Input/Output Characteristics

Spec Num	Characteristic	Min	Max	Unit
S10	TA/TEA input	6		nS
H10	TA/TEA input		1	nS
S11	Data bus input signals	7		nS
H11	Data bus input signals		1	nS
S12	All other input signals	7		nS
H12	All other input signals		1	nS
S13	AACK/TEA output	1	7	nS
S13'	TA output	1	8.5	nS
S14	BR/BG/DBG/SBG/SDBG output	1	7	nS
S15	Data bus output signals	1	8.5	nS
S16	All other output signals	1	7	nS

1.3 Pinout

Table 10. Pin Assignments

Ball	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ
1	PowVdd5	PowVdd6	PowVdd30	DP3	CoreGnd0	CoreVdd0	ARTRY	TT2	PowGnd2	SRG	PowGnd3	A8	SBR	A15	CoreVdd2	A18	A22	A25	A29	INT	BTO	API	CSA4	CSA7	CoreVdd4	TxSD0	PowVdd31	PowVdd13	PowVdd12
2	PowVdd7	PowVdd4	PowVdd3	DP1	DP2	PowGnd0	TS	AACK	DPE	SDRG	A1	A4	A7	A11	A12	CoreGnd2	A21	CoreVdd20	A26	A30	CoreVdd3	CSA6	AP2	PowGnd10	TC1	SYSCLK	ACoreGnd1	TxSD1	PowVdd14
3	PowVdd29	DP5	PowVdd3	DP0	TSIZ0	CoreVdd0	DBG	ABB	TT0	TT4	CoreGnd1	CoreVdd1	BR	A10	PowGnd5	A17	A19	A23	A27	PowGnd8	SRG	AP0	APE	MMODE	CoreGnd4	ACoreVdd1	RxCK0	PowVdd10	PowVdd32
4	DP4	D55	D8	PowVdd2	TX	TSIZ1	GT_DBG	PowGnd1	TT3	A0	A3	A6	PowGnd4	A14	A16	PowGnd6	A24	A28	A31	LBCLAIM	PowGnd9	WT	GBL	TxCK0	RxSD0	PowVdd9	RxSD1	TxCK2	TxSD2
5	D31	D39	D47	D0	PowVdd1	TEST	TSIZ2	BG	TT1	DBB	A2	A5	A9	A13	CoreGnd20	A20	PowGnd7	TEA	CoreGnd8	DRTRY	AP3	CI	TC0	PLL1O	PowVdd8	RxCK1	CoreVdd5	RxCK2	TxSD3
6	CoreGnd19	D23	CoreVdd25	PowGnd35	D63															PowGnd11	CoreGnd5	RxSD2	RxSD3	CoreVdd6	PowGnd11	RxCK3	RxSD2	RxCK3	RxCK3
7	D54	D62	PowGnd34	CoreVdd25	CoreVdd19															CoreGnd5	RxSD5	RxSD3	TxCK4	RxSD4	CoreGnd5	RxSD3	TxCK4	RxSD4	RxCK4
8	PowGnd33	D30	CoreGnd25	D46	D7															TxSD4	TxSD5	TxCK5	RxCK5	PowGnd12	TxSD4	TxSD5	TxCK5	RxCK5	PowGnd12
9	D61	D6	D14	D22	D38															RxSD5	TxSD6	TxCK6	CoreGnd21	RxCK6	RxSD5	TxSD6	TxCK6	RxCK6	RxCK6
10	D45	PowGnd32	D53	CoreVdd18	DP6															RxSD6	TxSD7	TxCK7	CoreGnd6	RxSD7	RxSD6	TxSD7	TxCK7	RxSD7	RxSD7
11	D21	DP7	D29	CoreGnd18	D37															RxCK7	CoreVdd6	TxSD8	TxCK8	RxSD8	RxCK7	CoreVdd6	TxSD8	RxSD8	RxSD8
12	D52	D60	D5	PowGnd31	D13															RxCK8	TxSD9	TxCK9	RxSD9	RxCK9	RxCK8	TxSD9	TxCK9	RxSD9	RxCK9
13	D28	PowGnd30	D36	D44	scan_out_i															PowGnd13	TxSD10	TxCK10	CoreVdd21	RxSD10	PowGnd13	TxSD10	TxCK10	RxSD10	RxSD10
14	CoreVdd17	D20	D4	D40	D12															TxSD11	TxCK11	RxSD11	RxCK10	RxCK11	TxSD11	TxCK11	RxSD11	RxCK11	RxCK11
15	D59	CoreGnd17	D43	D51	D51															TxSD12	CoreGnd7	RxSD12	TxSD12	CoreVdd7	TxSD12	CoreGnd7	RxSD12	CoreVdd7	CoreVdd7
16	D35	PowGnd28	D27	D19	D19															RxSD13	TxCK13	TxSD13	RxCK13	RxCK12	RxSD13	TxCK13	TxSD13	RxCK12	RxCK12
17	D11	D3	D58	CoreGnd24	D50															RxSD14	CoreGnd22	TxCK14	TxSD14	PowGnd14	RxSD14	CoreGnd22	TxCK14	PowGnd14	RxCK14
18	D42	PowGnd27	D34	D26	D18															RxCK15	RxSD15	TxCK15	TxSD15	RxCK14	RxCK15	RxSD15	TxCK15	RxCK14	RxCK14
19	D32	D10	CoreVdd16	D2	PowGnd26															RxCK16	CoreGnd8	RxSD16	TxCK16	TxSD16	RxCK16	CoreGnd8	RxSD16	TxSD16	TxSD16
20	D57	CoreGnd16	D49	D41	D33															PowGnd15	RxSD17	TxCK17	CoreVdd8	TxSD17	PowGnd15	RxSD17	TxCK17	TxSD17	TxSD17
21	CoreVdd23	D25	PowGnd25	D17	D16															TxSD19	CoreVdd22	TxCK18	TxSD18	RxCK17	TxSD19	CoreVdd22	TxCK18	TxSD18	RxCK17
22	D9	D1	D56	D48	D24															RxSD20	CoreVdd19	TxCK19	RxCK18	RxSD18	RxSD20	CoreVdd19	TxCK19	RxSD18	RxCK18
23	PowGnd24	scan_out_h	scan_out_g	scan_out_f	C50															CoreVdd9	TxSD21	TxCK20	TxSD20	RxCK19	CoreVdd9	TxSD21	TxCK20	RxCK19	RxCK19
24	CoreGnd23	CS1	CoreVdd15	CSA2	CS2		CoreVdd14													RxSD22	PowGnd16	CoreGnd9	TxCK21	RxCK20	RxSD22	PowGnd16	CoreGnd9	RxCK20	TxCK20
25	PowGnd23	CoreGnd15	scan_out_j	scan_out_e	PowVdd22	AMODE	CoreVdd14	CSA0	TMS	ACoreGnd2	TxCK39	TxCK38	TxCK37	RxCK35	RxCK34	RxCK33	TxSD31	TxSD31	TxCK29	PowVdd15	RxCK22	TxSD22	RxCK21	RxSD21	PowVdd15	RxCK22	TxSD22	TxCK23	TxSD21
26	scan_out_k	scan_out_k	PowGnd22	PowVdd23	SMODE1	scan_out_d	CoreGnd14	HRESET	TDO	RxCK39	CoreVdd13	PowGnd20	TxSD37	RxSD35	RxSD34	PowGnd19	RxSD32	TxCK31	CoreVdd11	TxSD24	TxCK27	TxSD23	TxCK22	PowVdd16	TxSD24	PowVdd16	TxSD23	TxCK22	scan_in_j
27	PowVdd36	TEST0	PowVdd24	SMODE0	TEST3	DBWO	DBRS	TDI	EXCLK	CoreVdd13	TxSD39	TxSD38	RxCK36	RxCK35	RxCK35	TxSD34	RxCK32	RxSD31	RxSD30	TxSD25	RxSD27	PowVdd17	TxCK23	PowVdd33	TxSD25	RxCK23	PowVdd17	TxCK23	PowVdd33
28	PowVdd28	PowVdd25	TEST2	PDR	CSA3	PowGnd21	TEST1	TRST	ACoreVdd2	RxSD39	RxCK38	RxCK37	RxSD36	TxSD36	RxSD36	RxSD33	TxSD33	RxCK31	scan_out_a	PowGnd17	TxSD28	RxSD26	RxCK24	PowVdd18	TxSD25	RxCK24	TxSD23	PowVdd18	PowVdd20
29	PowVdd26	PowVdd27	PowVdd35	SEN	CSA5	CSA1	PQMD	TCK	PLL2O	scan_out_c	RxSD38	RxSD37	TxCK36	CoreVdd12	TxSD35	TxCK34	TxCK33	TxSD32	RxCK30	CoreGnd1	RxSD29	TxCK28	PowVdd34	PowVdd21	RxCK28	RxCK23	PowVdd34	PowVdd21	PowVdd19
Ball	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ

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