

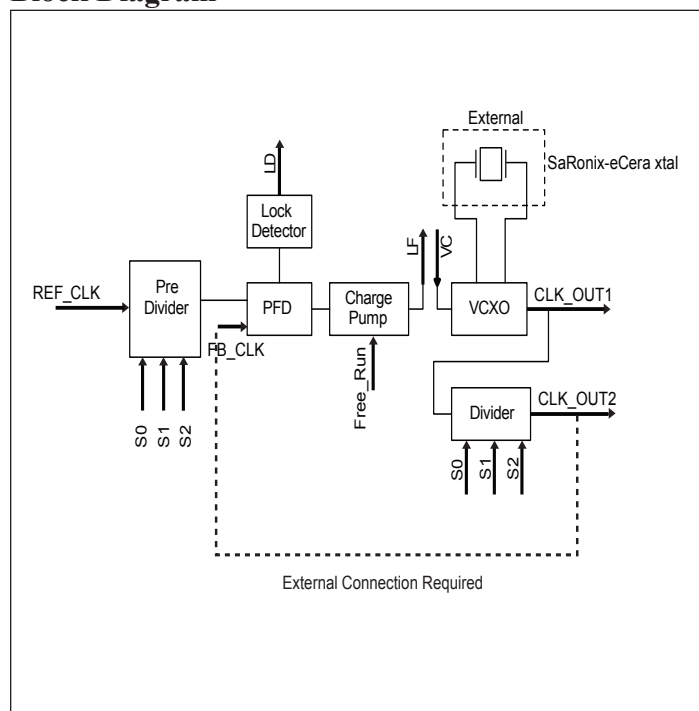
## Features

- PLL with quartz stabilized VCXO
- Optimized for 25MHz input/output frequency
- Other frequencies available
- Low phase jitter less than 350fs typical
- Free run mode  $\pm 100\text{ppm}$
- Single ended input and outputs
- 3.3V single supply
- Lock detection
- Industrial Temperature:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- 20-pin TSSOP package

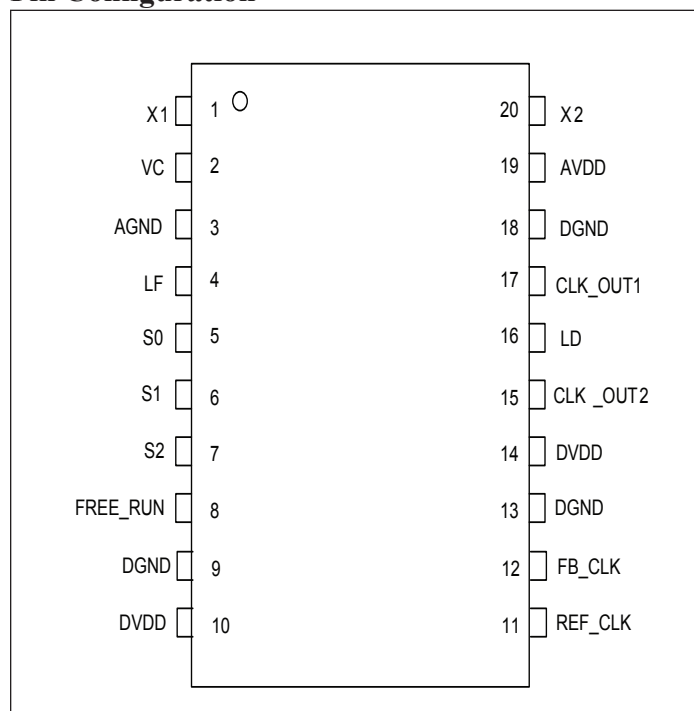
## Description

The PI6CX201A is composed of a phase-locked loop with integrated VCXO oscillator for use in the clock jitter attenuation applications. It is optimized for use with a SaRonix-eCera™ crystal of 25MHz, and has typical output phase jitter less than 350fs (RMS).

## Block Diagram



## Pin Configuration



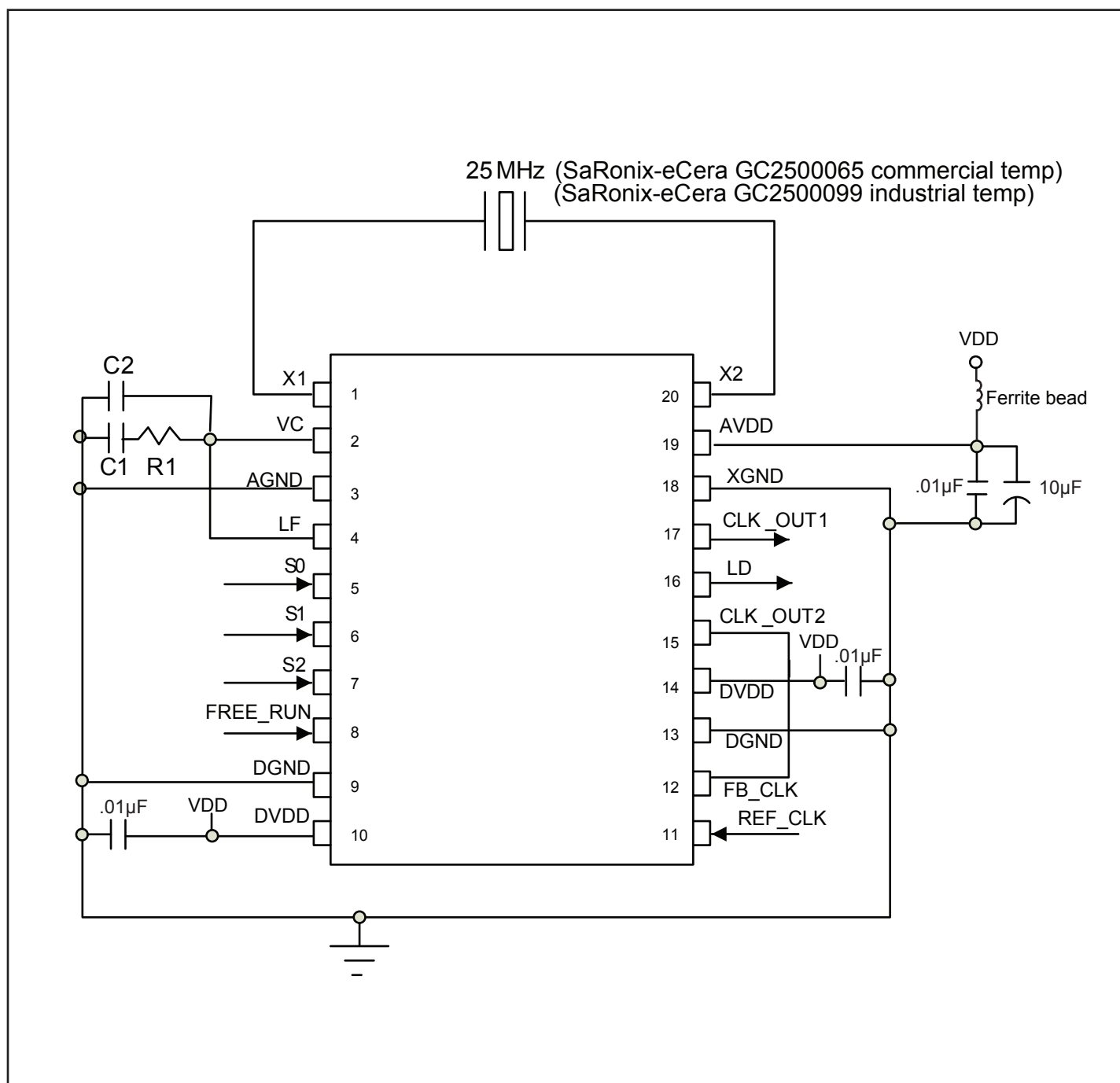
**Pin Descriptions for 20-pin TSSOP Package**

| Pin Name   | Type | Pin No    | Description                                                                                                                                                                                                                                           |
|------------|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| XI         | I    | 1         | Crystal input pin                                                                                                                                                                                                                                     |
| VC         | I    | 2         | VCXO control voltage input                                                                                                                                                                                                                            |
| LF         | I    | 4         | Loop filter pin for external loop filter connection                                                                                                                                                                                                   |
| AGND       | PWR  | 3         | Analog ground                                                                                                                                                                                                                                         |
| S0, S1, S2 | I    | 5, 6, 7   | LVC MOS selection pins for internal CLK_OUT2 divider, Pins have internal pull up resistor                                                                                                                                                             |
| REF_CLK    | I    | 11        | LVC MOS input clock signal to phase detector                                                                                                                                                                                                          |
| FB_CLK     | I    | 12        | LVC MOS feedback clock signal to phase detector                                                                                                                                                                                                       |
| DGND       | PWR  | 9, 13, 18 | Digital ground                                                                                                                                                                                                                                        |
| DVDD       | PWR  | 10, 14    | Digital power                                                                                                                                                                                                                                         |
| CLK_OUT2   | O    | 15        | LVC MOS output clock of the internal VCXO with divider controlled by S0 and S1                                                                                                                                                                        |
| LD         | O    | 16        | LVC MOS lock detect output, LD output is logic '0' when REF_CLKx is greater than 1MHz, and phase difference between REF_CLKx and FB_CLK is more than 2ns for 8 consecutive clock pulses. The clock pulse frequency is equal to the crystal frequency. |
| CLK_OUT1   | O    | 17        | LVC MOS output clock of the internal VCXO                                                                                                                                                                                                             |
| AVDD       | PWR  | 19        | Analog power                                                                                                                                                                                                                                          |
| X2         | O    | 20        | Crystal output pin                                                                                                                                                                                                                                    |
| FREE_RUN   | I    | 8         | When FREE_RUN is logic low, chip is in "free run" mode. The output will remain fixed at a fixed frequency with up to a $\pm 100$ ppm offset from the nominal 25MHz. Logic HIGH is normal mode, with output locked to the input. Internal pull-up.     |

**Frequency Selection Table**

| Input Frequency | S0 | S1 | S2 | Output Frequency |
|-----------------|----|----|----|------------------|
| 25MHz           | 1  | 0  | 1  | 25MHz            |
| 12.5MHz         | 0  | 0  | 1  | 25MHz            |
| 33.33MHz        | 0  | 1  | 1  | 25MHz            |
| 66.67MHz        | 1  | 1  | 1  | 25MHz            |

## Application Diagram



### Notes:

1. A feedback clock is required for lock. Pin 15 can be connected to pin 12 as shown above.
2. The network R1, C1:C2 comprises the external loop filter. The loop bandwidth and jitter peaking profiles are set by changing these values. Please consult factory to meet your requirement.
3. The crystal and loop filter components should be placed on the same side of the board as the IC. Components should be placed as close as possible to IC (within 300 mils).
4. A ground ring should enclose the loop filter components along with pins 2 and 4.

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

|                                                       |                       |
|-------------------------------------------------------|-----------------------|
| Storage temperature .....                             | -65 to +150°C         |
| Supply Voltage to Ground Potential ( $V_{DD}$ ) ..... | -0.5 to +4.6V         |
| Inputs (Referenced to GND) .....                      | -0.5 to $V_{DD}+0.5V$ |
| Clock Output (Referenced to GND) .....                | -0.5 to $V_{DD}+0.5V$ |
| Soldering Temperature (Max of 10 seconds) .....       | 260°C                 |
| Latch up .....                                        | 200mA                 |
| ESD Protection (HBM) .....                            | 2000V                 |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### 3.3V DC Electrical Characteristics

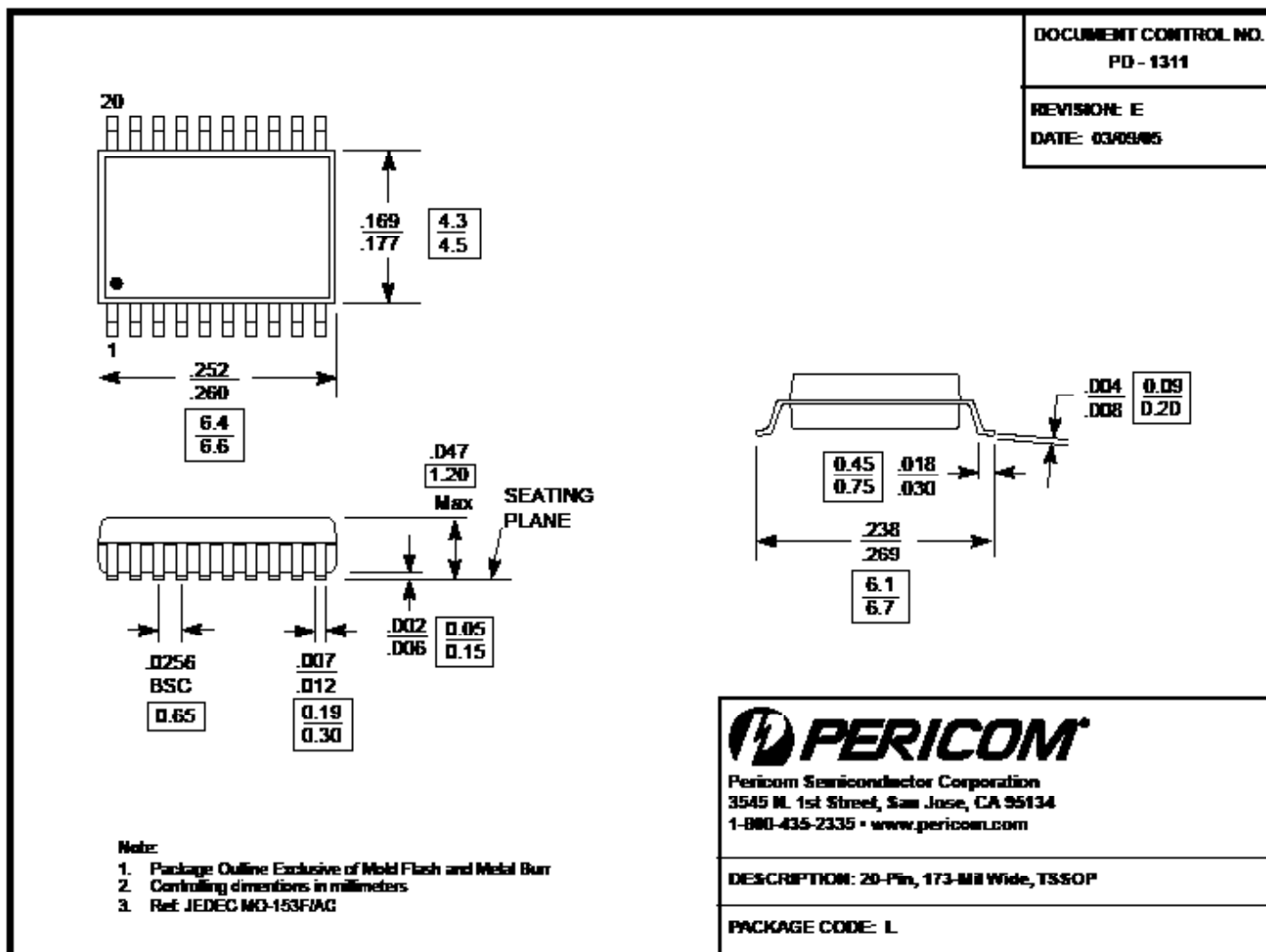
| Parameter | Description                  | Test Conditions   | Min.  | Max            | Units   |
|-----------|------------------------------|-------------------|-------|----------------|---------|
| $V_{DD}$  | 3.3V Supply Voltage          |                   | 3.135 | 3.465          | V       |
| $V_{IL}$  | Input LOW Voltage            |                   |       | 0.8            |         |
| $V_{IH}$  | Input HIGH Voltage           |                   | 2     | $V_{DD} + 0.3$ |         |
| $I_{IL}$  | Input LOW Current            | $V_{IN} = 0V$     | -50   |                | $\mu A$ |
| $I_{IH}$  | Input HIGH Current           | $V_{IN} = V_{DD}$ |       | 10             |         |
| $V_{OL}$  | Output LOW Voltage           | $I_{OL} = 8mA$    |       | 0.4            | V       |
| $V_{OH}$  | Output HIGH Voltage          | $I_{OL} = -8mA$   | 2.4   |                | V       |
| $T_A$     | Ambient Operatin Temperature |                   | -40   | 85             | °C      |

### 3.3V AC Electrical Characteristics

| Parameter        | Description                | Test Conditions                                         | Min. | Typ       | Max       | Units |
|------------------|----------------------------|---------------------------------------------------------|------|-----------|-----------|-------|
| $F_O$            | Output Frequency           | $CL = 15pF$                                             |      | 25        |           | MHz   |
| BW               | Control Voltage Band Width | -3 dB, $VC=1.65V$                                       |      | 25        |           | KHz   |
| $\Delta F_{CLK}$ | Control Pull Range         | $0V \leq VC \leq V_{DD}$                                |      | $\pm 140$ |           | ppm   |
| $t_{IDC}$        | Input Duty Cycle           | Measured at $V_{DD}/2$                                  | 40   | 50        | 60        | %     |
| $t_{DC}$         | Output Duty Cycle          | Measured at $V_{DD}/2$ ,<br>15pF load                   | 45   | 50        | 55        | %     |
| $t_R, t_F$       | Rise and Fall Time         | CLK_OUT1 Measured<br>from 0.5V to 2.5V, $C_L$<br>= 0pF  |      |           | 2         | ns    |
| $t_R, t_F$       | Rise and Fall Time         | CLK_OUT1 Measured<br>from 0.5V to 2.5V, $C_L$<br>= 15pF |      |           | 3         | ns    |
| $J_p$            | Phase Jitter (RMS)         | 12kHz to 5Mhz                                           |      | 0.35      | 0.5       | ps    |
| $F_{free}$       | Free Run Accuracy          |                                                         |      |           | $\pm 100$ | ppm   |

**Loop Filter Selection Table**

| Loop Band Width | Charge Pump Current | VCO Gain | Feedback Divider | R1       | C1  | C2    |
|-----------------|---------------------|----------|------------------|----------|-----|-------|
| 100Hz           | 32uA                | 2.5KHz/V | 1                | 5.1K Ohm | 1uF | 0.1uF |

**Packaging Mechanicals: 20-Pin TSSOP (L)**

**Recommended Crystal:**

SaRonix-eCERA Part Number: GC2500065

**Ordering Information<sup>(1-3)</sup>**

| Ordering Code | Package Code | Package Description                    |
|---------------|--------------|----------------------------------------|
| PI6CX201ALE   | L            | 20-pin TSSOP, Pb-free & Green          |
| GC2500065     | N/A          | Commercial temperature 49S SMD Crystal |
| GC2500099     | N/A          | Industrial temperature 49S SMD Crystal |

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Diodes Incorporated:](#)

[PI6CX201ALEX](#) [PI6CX201ALE](#)