CTVS –
Ceramic transient voltage suppressors

SMD multilayer varistors (MLVs),
surge protection series

Series/Type:

Date: May 2017

EPCOS AG is a TDK Group Company.

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EPCOS type designation system for surge protection series

CT	1206	K	30	E2	G	K2

Construction:
CT ≙ Single chip with nickel barrier termination (AgNiSn)
CN ≙ Single chip with silver-platin temination (AgPt)

Case sizes:
0805
1206
1210
1812
2220

Tolerance of the varistor voltage:
K ≙ ±10%, standard
S ≙ Special tolerance

Maximum RMS operating voltage (V_{RMS}):
30 ≙ 30 V

Features:
E2 ≙ Increased energy handling capability
TELE ≙ Specified for 10/700 µs pulses, acc. to telecom standards
A ≙ Special tolerance

Taping mode:
G ≙ 180-mm reel, 7"
G2 ≙ 330-mm reel, 13"

Termination:
K2 ≙ Code for AgPt termination (CN types only)

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Description

The surge protection series comprises a range of multilayer varistors for protection against severe transient overvoltage and high surge currents, such as 8/20 µs pulses with peak currents up to 6000 A and 10/700 µs pulses up to 45 A.

Features

- High energy absorption capability
- High surge load capability acc. to IEC 61000-4-5
- Reliable ESD protection up to 30 kV acc. to IEC 61000-4-2, level 4
- High surge voltage capability up to 2 kV for 10/700 µs acc. to IEC 61000-4-5 (types with $V_{RMS,max} \leq 60$ V)
- UL approval to UL 1449 (file number E481997)
- Bidirectional protection
- Low leakage current
- Long-term ESD stability
- RoHS-compatible, lead-free
- PSpice simulation modesl available

Applications

- Industrial applications
- Building safety and security applications
- Power supplies
- Control and measurement equipment
- Hard disk drives

Design

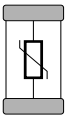
- Multilayer technology
- Flammability rating better than UL 94 V-0
- Termination (see “Soldering directions”):
  - CT types with nickel barrier terminations (AgNiSn), recommended for lead-free soldering, and compatible with tin/lead solder
  - CN types with silver-platin termination (AgPt) for reflow and wave soldering with solder on tin/lead basis or lead-free with a silver containing solder

V/I characteristics and derating curves

V/I and derating curves are attached to the data sheet. The curves are sorted by V_{RMS} and then by case size, which is included in the type designation.

Single chip

Internal circuit



MLV0006-H

Available case sizes:

EIA	Metric
0805	2012
1206	3216
1210	3225
1812	4532
2220	5750

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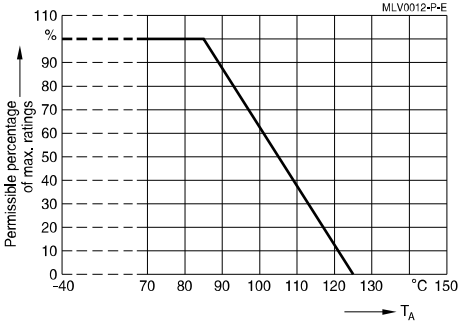
General technical data

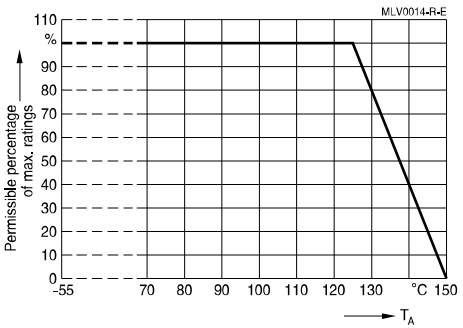
Maximum RMS operating voltage		$V_{RMS,max}$	30 ... 115	V
Maximum DC operating voltage		$V_{DC,max}$	38 ... 150	V
Maximum surge current	(8/20 µs)	$I_{surge,max}$	40 ... 6000	A
Maximum surge current	(10/700 µs)	$I_{surge,max}$	45	A
Maximum clamping voltage		$V_{clamp,max}$	77 ... 360	V
Operating temperature	(8/20 µs surge ratings)	T_{op}	−55/+125	°C
Operating temperature	(10/700 µs surge ratings)	T_{op}	−40/+85	°C
Storage temperature	(8/20 µs surge ratings)	LCT/UCT	−55/+150	°C
Storage temperature	(10/700 µs surge ratings)	LCT/UCT	−40/+125	°C
Response time		t_{resp}	< 0.5	ns

Temperature derating

Climatic category:
−40/+85 °C for chip size 1812 (dedicated telecom types: CT1812S60AG2, CT1812K75TELEG2, CT1812S95 AG2, CT1812K115TELEG2)



Climatic category:
−55/+125 °C for chip sizes 0805, 1206, 1210, 1812, and 2220



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Electrical specifications and ordering codes

Maximum ratings ($T_{op,max}$)

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 µs) A	$I_{surge,max}$ (10/700 µs) A	W_{max} (2 ms) mJ	$P_{diss,max}$ (2 ms) mW
High surge protection types, 8/20 µs surge rating, $T_{op,max}$ = +125 °C							
CT2220K30E2G	B72540T6300K062	30	38	5000	-	15000	20
CN2220K30E2GK2	B72542V6300K062	30	38	6000	-	15000	20
CN2220K50E2GK2	B72542V6500K062	50	65	4500	-	15000	20
CN2220S50E2GK2	B72542V6500S162	50	63	4500	-	15000	20
CT2220K50E2G	B72540T6500K062	50	65	4500	-	15000	20
CT2220S50E3G	B72540T6500S162	50	63	4500	-	15000	20
CN2220K60E2GK2	B72542V6600K062	60	85	4500	-	15000	20
Surge protection types, 8/20 µs surge rating, $T_{op,max}$ = +125 °C							
CT0805K30G	B72510T0300K062	30	38	80	-	300	5
CT1206K30G	B72520T0300K062	30	38	200	-	1100	8
CT1210K30G	B72530T0300K062	30	38	300	-	2000	10
CT1812K30G	B72580T0300K062	30	38	800	-	4200	15
CT2220K30G	B72540T0300K062	30	38	1200	-	12000	20
CT0805K35G	B72510T0350K062	35	45	80	-	300	5
CT1206K35G	B72520T0350K062	35	45	100	-	400	8
CT1210K35G	B72530T0350K062	35	45	250	-	2000	10
CT1812K35G	B72580T0350K062	35	45	500	-	4000	15
CT1206K40G	B72520T0400K062	40	56	100	-	500	8
CT1210K40G	B72530T0400K062	40	56	250	-	2300	10
CT1812K40G	B72580T0400K062	40	56	500	-	4800	15
CT2220K40G	B72540T0400K062	40	56	1000	-	9000	20
CT1206K50G	B72520T0500K062	50	65	100	-	600	8
CT1210K50G	B72530T0500K062	50	65	200	-	1600	10
CT1812K50G	B72580T0500K062	50	65	400	-	4500	15
CT2220K50G	B72540T0500K062	50	65	800	-	5600	20
CT1210K50E2G	B72530T6500K062	50	65	1200	-	3000	10
CT1206K60G	B72520T0600K062	60	85	100	-	700	8
CT1210K60G	B72530T0600K062	60	85	200	-	2000	10
CT1812K60G	B72580T0600K062	60	85	400	-	5800	15
CT2220K60G	B72540T0600K062	60	85	800	-	6800	20
CT1812K130G2	B72580T0131K072	130	170	250	-	3500	15
Telecom types, 10/700 µs surge rating, $T_{op,max}$ = +85 °C							
CT1812S60AG2	B72580T0600S172	60	85	400	45	2200	15
CT1812K75TELEG2	B72580T6750K072	75	100	400	45	2500	15
CT1812S95AG2	B72580T0950S172	95	125	250	45	2800	15
CT1812K115TELEG2	B72580T6111K072	115	150	250	45	3200	15

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Characteristics (T_A = 25 °C)

Type	V_V (1 mA) V	ΔV_V %	$V_{clamp,max}$ V	I_{clamp} (8/20 µs) A	C_{typ} [1] (1 MHz, 1 V) pF
High surge protection types, 8/20 µs surge rating, $T_{op,max}$ = +125 °C					
CT2220K30E2G	47	±10	77	10	10000
CN2220K30E2GK2	47	±10	77	10	10000
CN2220K50E2GK2	82	±10	135	10	3000
CN2220S50E2GK2	77	±10	130	10	5000
CT2220K50E2G	82	±10	135	10	3000
CT2220S50E3G	77.5	±8.4	115	10	8800
CN2220K60E2GK2	100	±10	165	10	3000
Surge protection types, 8/20 µs surge rating, $T_{op,max}$ = +125 °C					
CT0805K30G	47	±10	77	1	200
CT1206K30G	47	±10	77	1	500
CT1210K30G	47	±10	77	2.5	1000
CT1812K30G	47	±10	77	5	2000
CT2220K30G	47	±10	77	10	4000
CT0805K35G	56	±10	95	1	150
CT1206K35G	56	±10	90	1	200
CT1210K35G	56	±10	90	2.5	600
CT1812K35G	56	±10	90	5	1200
CT1206K40G	68	±10	110	1	250
CT1210K40G	68	±10	110	2.5	500
CT1812K40G	68	±10	110	5	1000
CT2220K40G	68	±10	110	10	2000
CT1206K50G	82	±10	135	1	120
CT1210K50G	82	±10	135	2.5	250
CT1812K50G	82	±10	135	5	500
CT2220K50G	82	±10	135	10	1000
CT1210K50E2G	82	±10	135	2.5	1200
CT1206K60G	100	±10	165	1	100
CT1210K60G	100	±10	165	2.5	200
CT1812K60G	100	±10	165	5	400
CT2220K60G	100	±10	165	10	800
CT1812K130G2	205	±10	340	5	200
Telecom types, 10/700 µs surge rating, $T_{op,max}$ = +85 °C					
CT1812S60AG2	100	+19/−1	200	45	400
CT1812K75TELEG2	120	±10	250	45	320
CT1812S95AG2	165	±10	270	45	250
CT1812K115TELEG2	180	±10	360	45	200

1) Measurement frequency: f = 1 MHz for C < 100 pF, f = 1 kHz for C ≥ 100 pF

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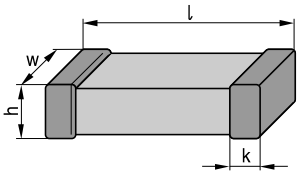
Dimensional drawing



MLV0031-M

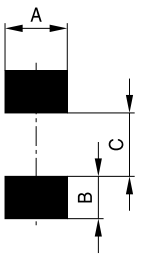
Dimensions in mm

Case size EIA / mm	l	w	h	k
0201 / 0603	0.6 ±0.03	0.30 ±0.03	0.33 max.	0.15 ±0.05
0402 / 1005	1.0 ±0.15	0.50 ±0.10	0.6 max.	0.10 ... 0.30
0603 / 1608	1.6 ±0.15	0.80 ±0.10	0.9 max.	0.10 ... 0.40
0805 / 2012	2.0 ±0.20	1.25 ±0.15	1.4 max.	0.13 ... 0.75
1206 / 3216	3.2 ±0.30	1.60 ±0.20	1.7 max.	0.25 ... 0.75
1210 / 3225	3.2 ±0.30	2.50 ±0.25	1.7 max.	0.25 ... 0.75
1812 / 4532	4.5 ±0.40	3.20 ±0.30	2.5 max.	0.25 ... 1.00
2220 / 5750	5.7 ±0.40	5.00 ±0.40	2.5 max.[1) 2)]	0.25 ... 1.00

1) h_{max} = 3.0 mm for type CN2220K30E2GK2, CN2220K50E2GK2, CT2220K30E2G, CT2220K50E2G and CN2220S50E2GK2

2) h_{max} = 3.3 mm for type CT2220S50E3G and CN2220K60E2GK2

Recommended solder pad layout



MLV0034-P

Dimensions in mm

Case size EIA / mm	A	B	C
0201 / 0603	0.30	0.25	0.30
0402 / 1005	0.60	0.60	0.50
0603 / 1608	1.00	1.00	1.00
0805 / 2012	1.40	1.20	1.00
1206 / 3216	1.80	1.20	2.10
1210 / 3225	2.80	1.20	2.10
1812 / 4532	3.60	1.50	3.00
2220 / 5750	5.50	1.50	4.20

Multilayer varistors (MLVs)

Surge protection series

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Delivery mode

EIA case size	Taping	Reel size mm	Packing unit pcs.	Type	Ordering code
Single chip					
0805	Blister	180	3000	CT0805K30G	B72510T0300K062
0805	Blister	180	3000	CT0805K35G	B72510T0350K062
1206	Blister	180	2000	CT1206K30G	B72520T0300K062
1206	Blister	180	2000	CT1206K35G	B72520T0350K062
1206	Blister	180	2000	CT1206K40G	B72520T0400K062
1206	Blister	180	2000	CT1206K50G	B72520T0500K062
1206	Blister	180	2000	CT1206K60G	B72520T0600K062
1210	Blister	180	2000	CT1210K30G	B72530T0300K062
1210	Blister	180	2000	CT1210K35G	B72530T0350K062
1210	Blister	180	2000	CT1210K40G	B72530T0400K062
1210	Blister	180	2000	CT1210K50E2G	B72530T6500K062
1210	Blister	180	2000	CT1210K50G	B72530T0500K062
1210	Blister	180	2000	CT1210K60G	B72530T0600K062
1812	Blister	180	1000	CT1812K30G	B72580T0300K062
1812	Blister	180	1000	CT1812K35G	B72580T0350K062
1812	Blister	180	1000	CT1812K40G	B72580T0400K062
1812	Blister	180	1000	CT1812K50G	B72580T0500K062
1812	Blister	180	1000	CT1812K60G	B72580T0600K062
1812	Blister	180	3000	CT1812K130G2	B72580T0131K072
1812	Blister	330	3000	CT1812K115TELEG2	B72580T6111K072
1812	Blister	330	3000	CT1812S95AG2	B72580T0950S172
1812	Blister	330	4000	CT1812K75TELEG2	B72580T6750K072
1812	Blister	330	4000	CT1812S60AG2	B72580T0600S172
2220	Blister	180	500	CT2220S50E3G	B72540T6500S162
2220	Blister	180	600	CN2220K30E2GK2	B72542V6300K062
2220	Blister	180	600	CN2220K50E2GK2	B72542V6500K062
2220	Blister	180	600	CN2220K60E2GK2	B72542V6600K062
2220	Blister	180	600	CN2220S50E2GK2	B72542V6500S162
2220	Blister	180	600	CT2220K30E2G	B72540T6300K062
2220	Blister	180	600	CT2220K50E2G	B72540T6500K062
2220	Blister	180	1000	CT2220K30G	B72540T0300K062
2220	Blister	180	1000	CT2220K40G	B72540T0400K062
2220	Blister	180	1000	CT2220K50G	B72540T0500K062
2220	Blister	180	1000	CT2220K60G	B72540T0600K062

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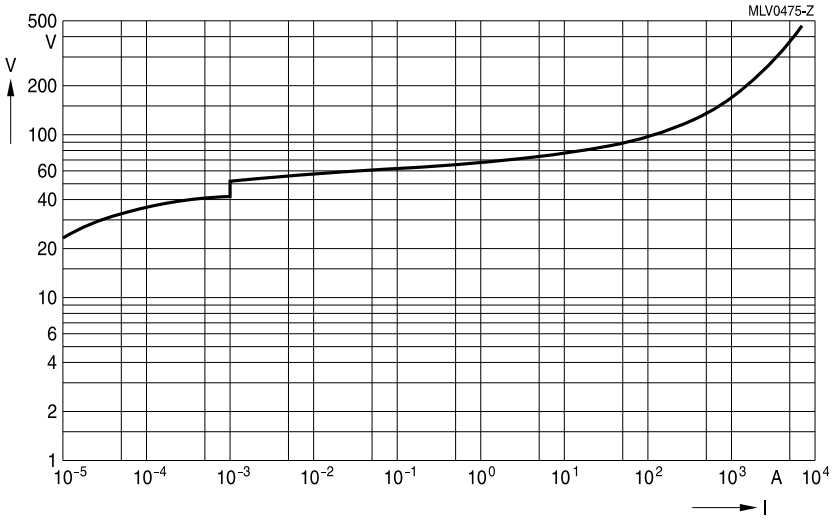
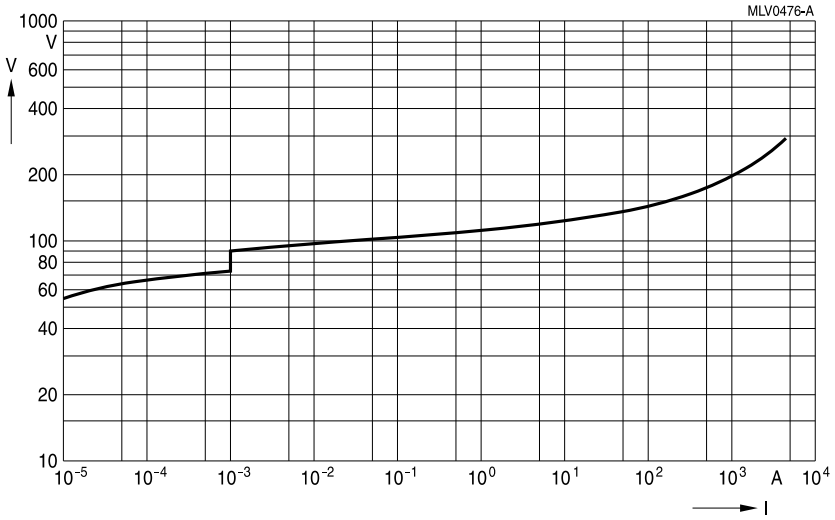
V/I characteristics for high surge protection types



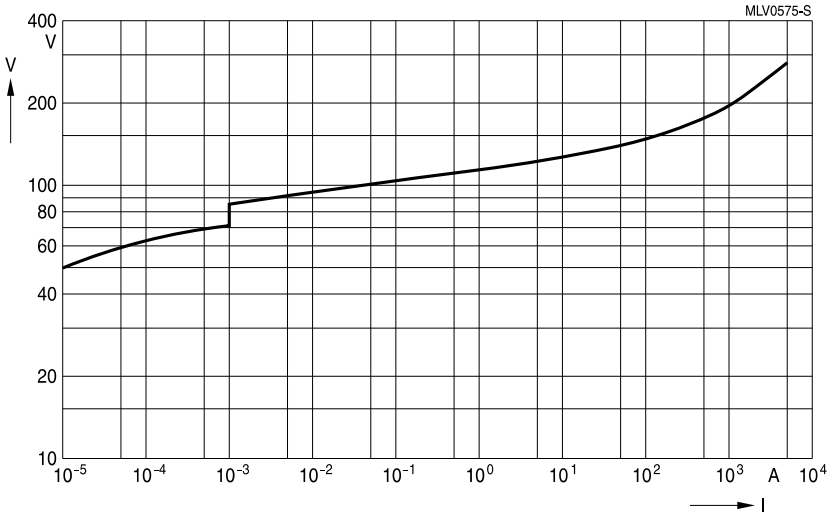
CN2220K30E2GK2



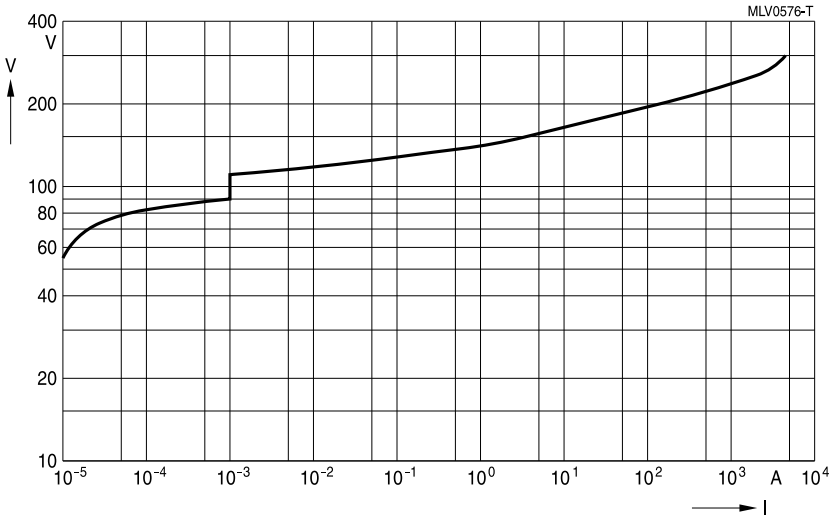
CN2220K50E2GK2

SMD

V/I characteristics for high surge protection types



CN2220S50E2GK2



CN2220K60E2GK2

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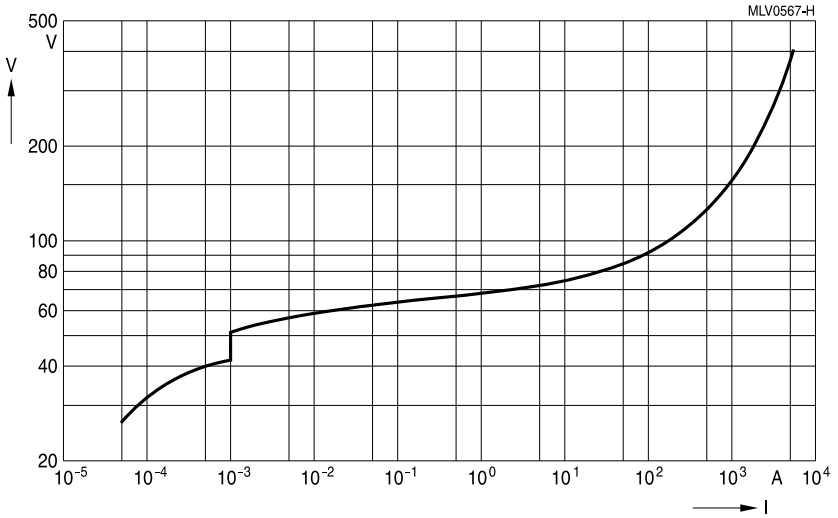
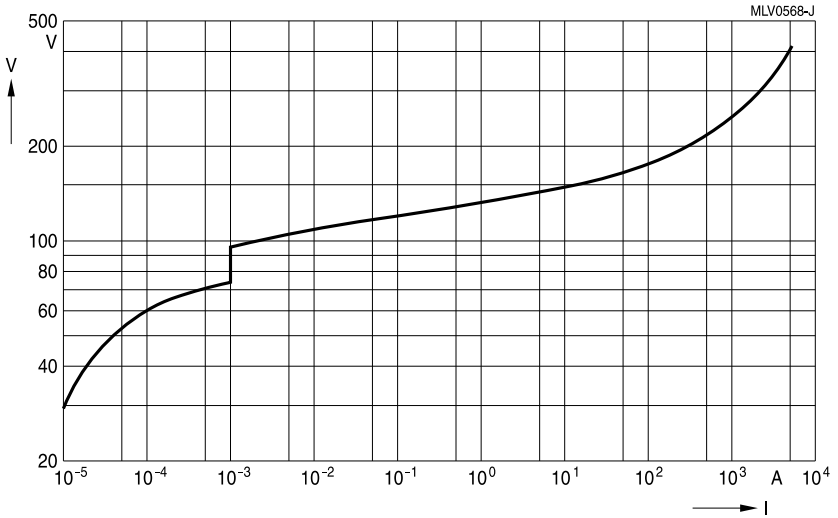
V/I characteristics for high surge protection types



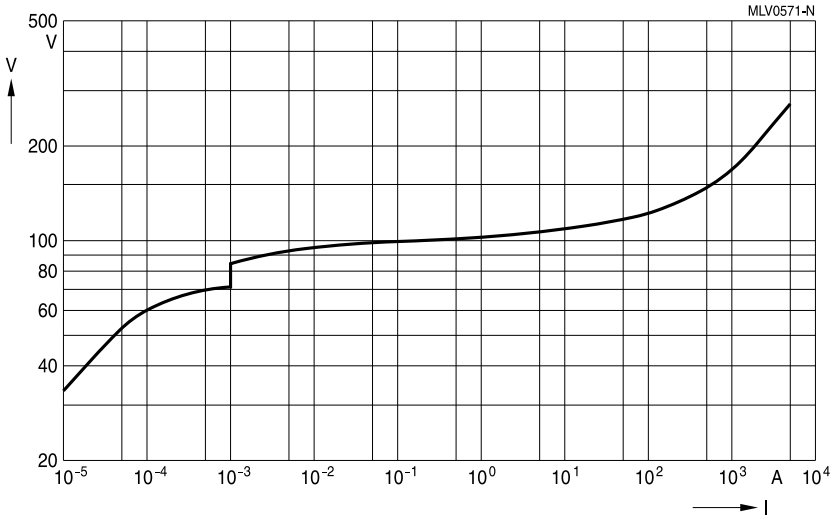
CT2220K30E2G



CT2220K50E2G

SMD

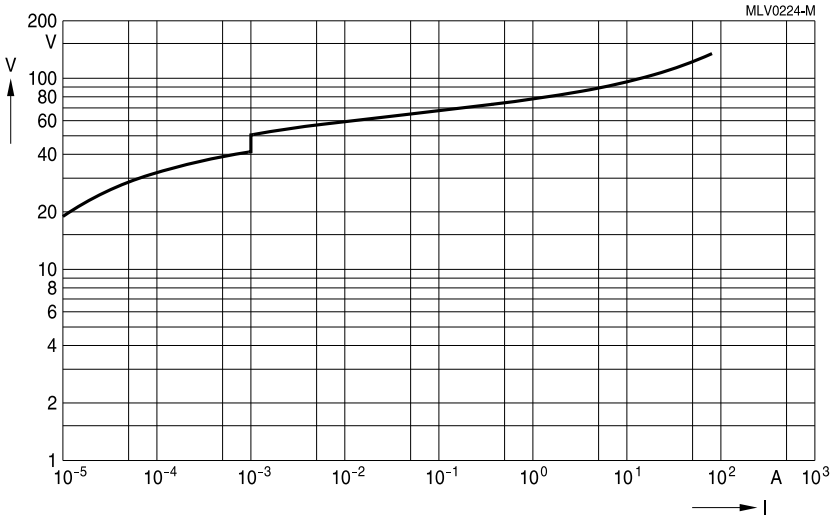
V/I characteristics for high surge protection types



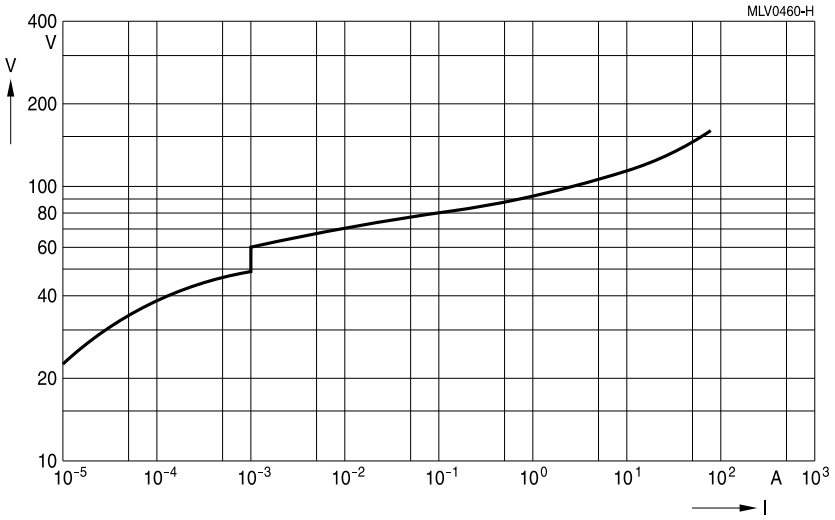
CT2220S50E3G

SMD

V/I characteristics for surge protection types



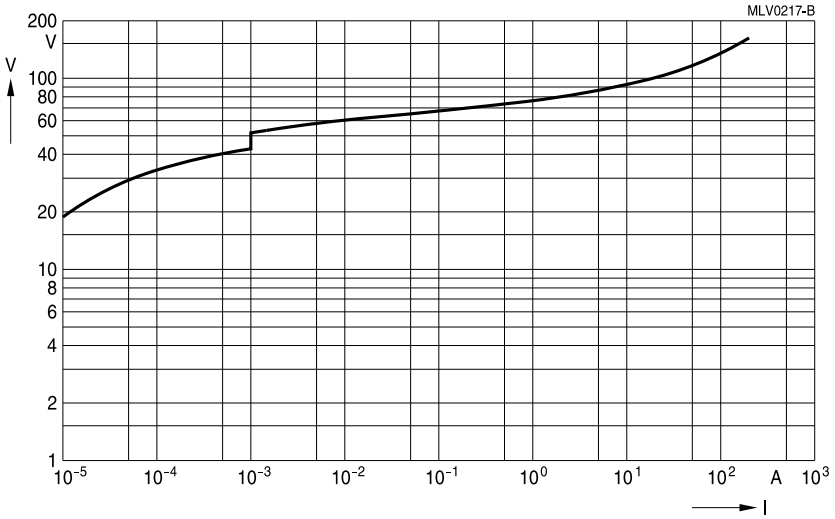
CT0805K30G



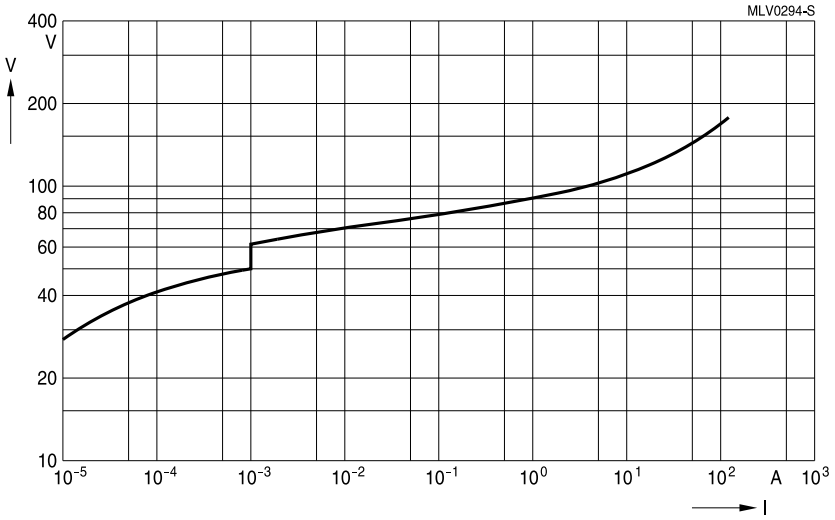
CT0805K35G

SMD

V/I characteristics for surge protection types



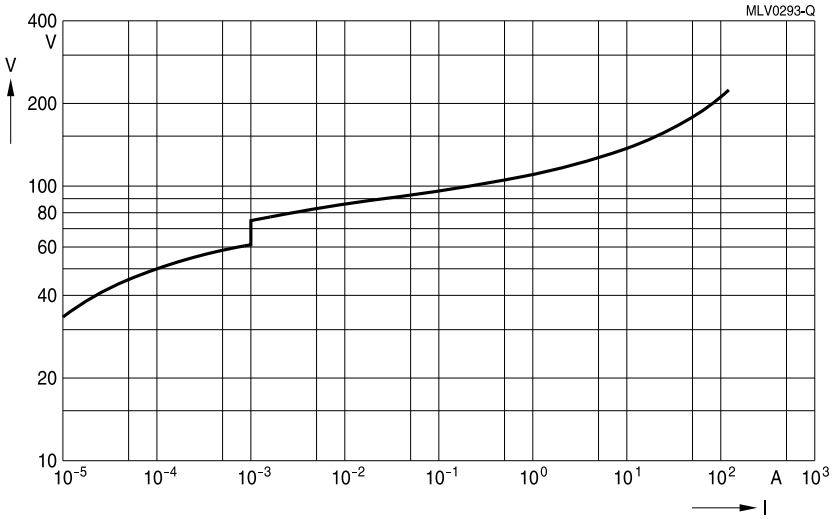
CT1206K30G



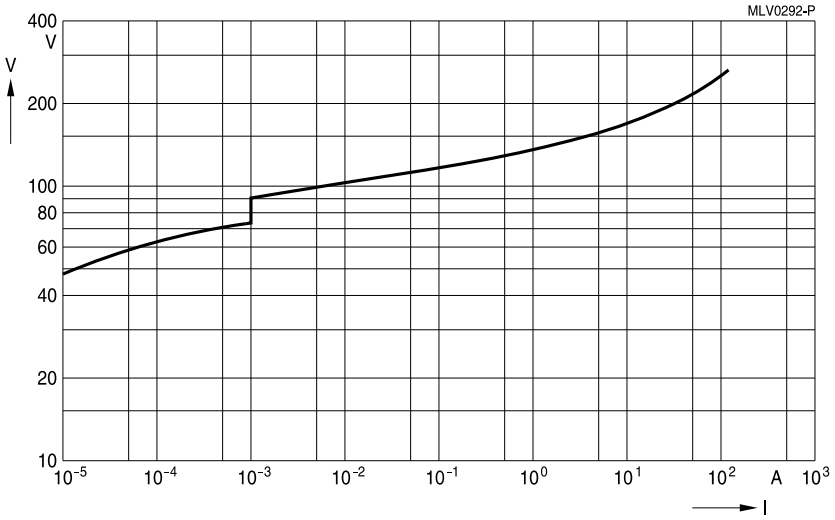
CT1206K35G

SMD

V/I characteristics for surge protection types



CT1206K40G



CT1206K50G

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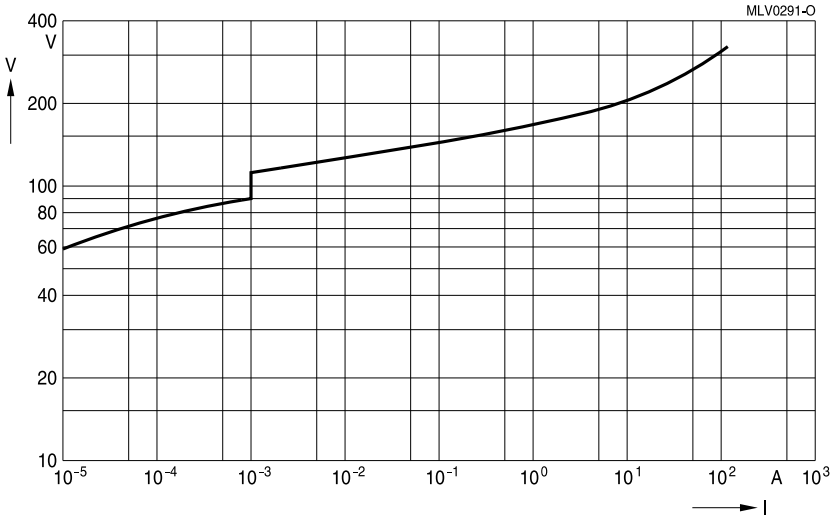
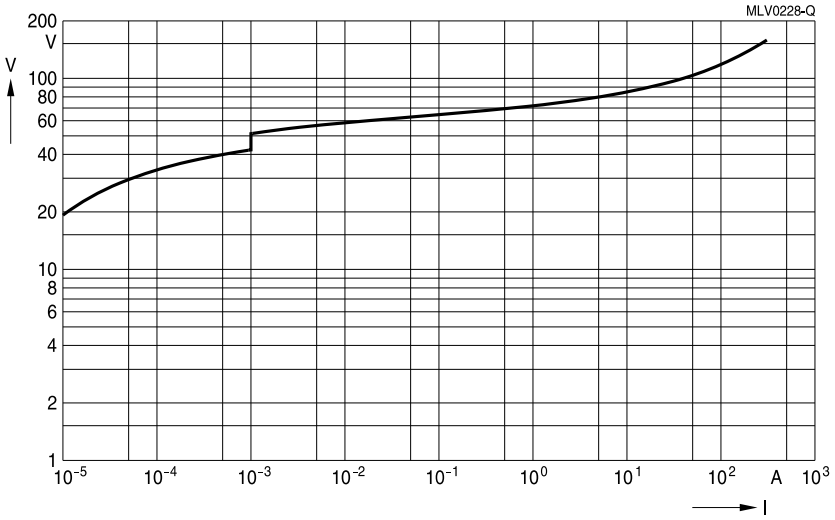
V/I characteristics for surge protection types



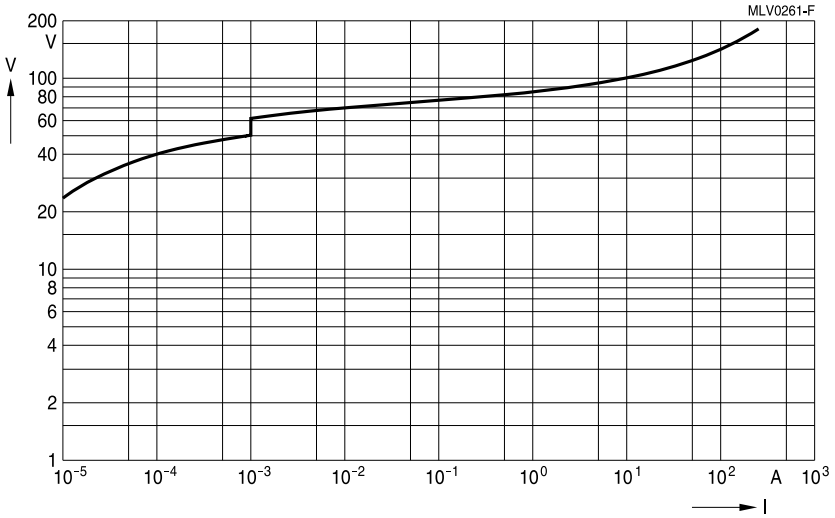
CT1206K60G



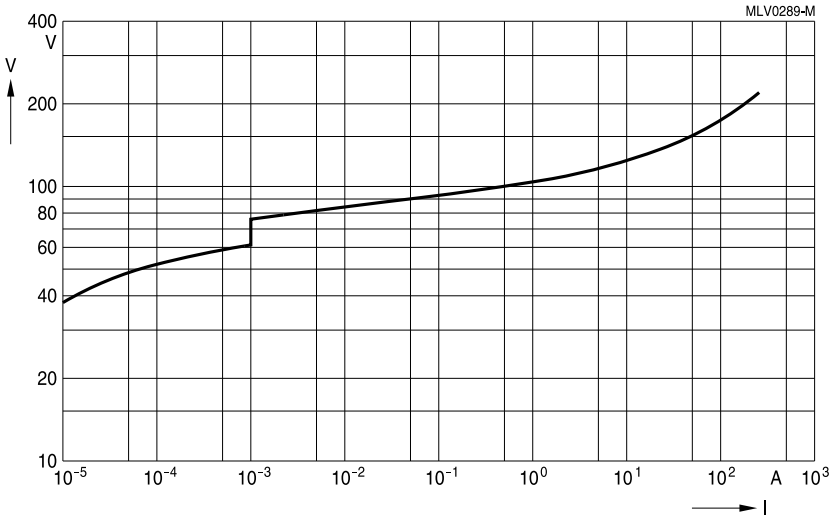
CT1210K30G

SMD

V/I characteristics for surge protection types



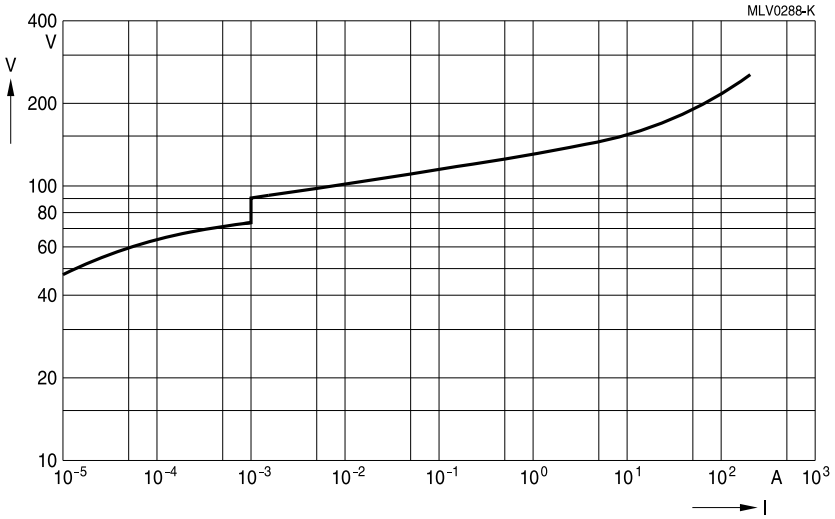
CT1210K35G



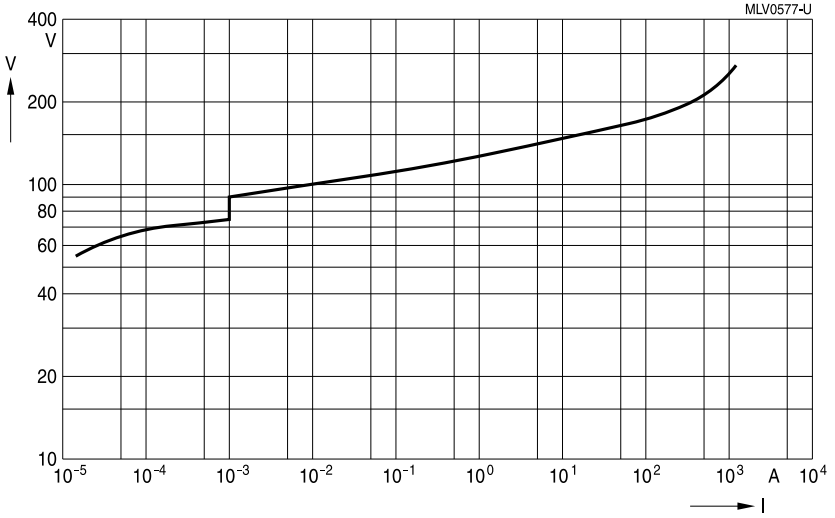
CT1210K40G

SMD

V/I characteristics for surge protection types



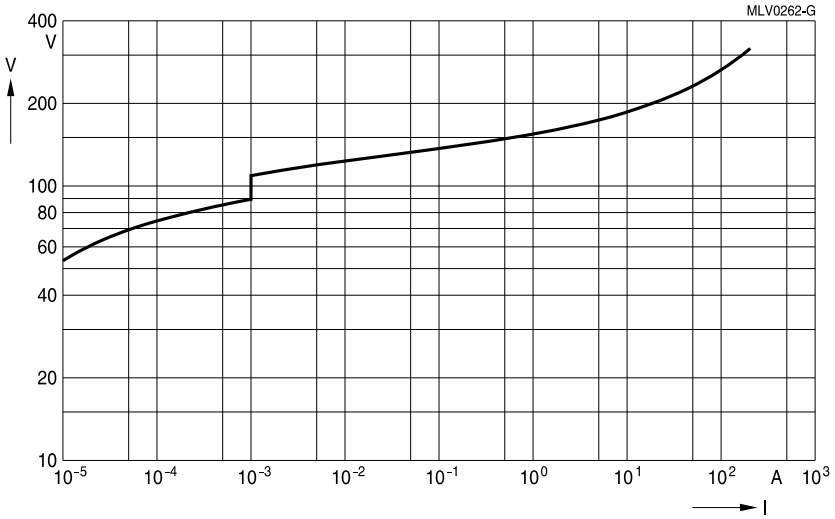
CT1210K50G



CT1210K50E2G

SMD

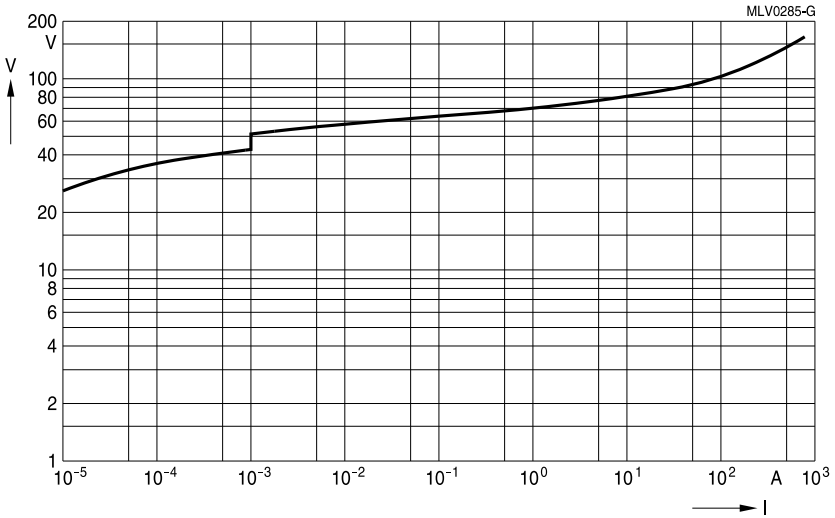
V/I characteristics for surge protection types



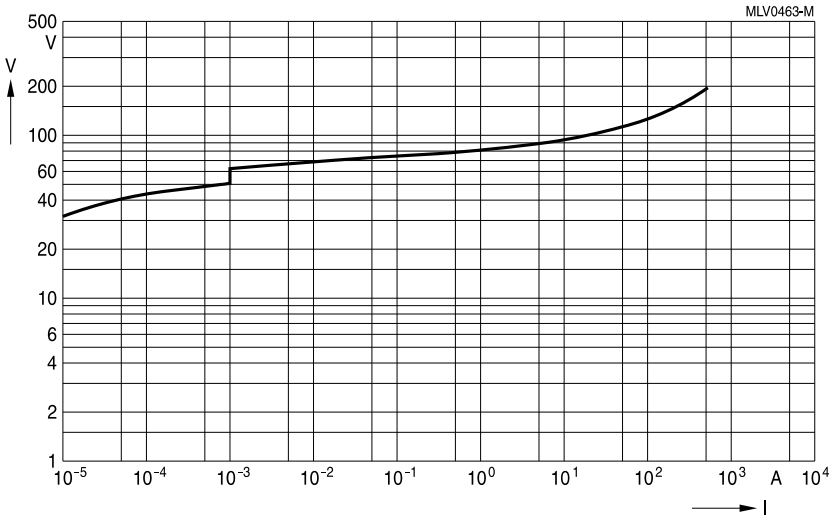
CT1210K60G

SMD

V/I characteristics for surge protection types



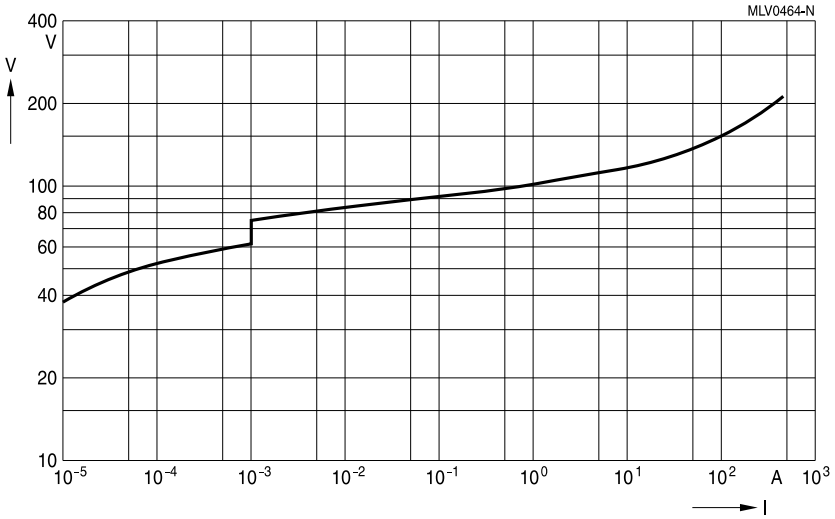
CT1812K30G



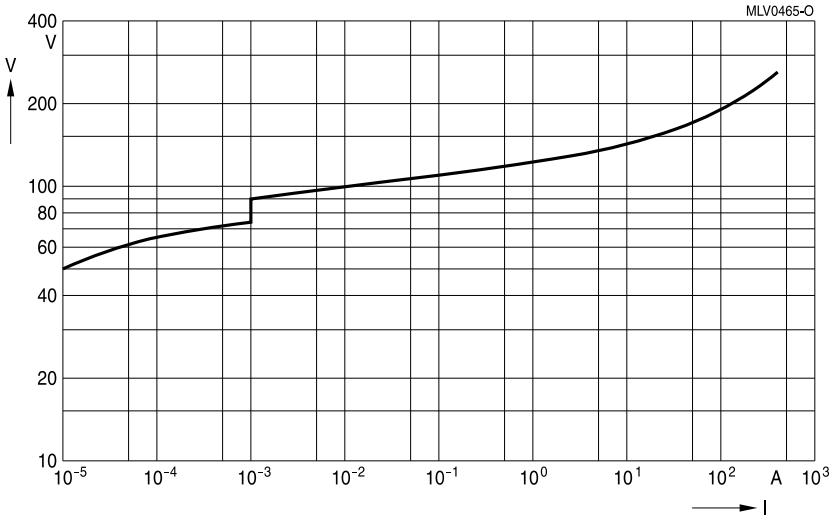
CT1812K35G

SMD

V/I characteristics for surge protection types



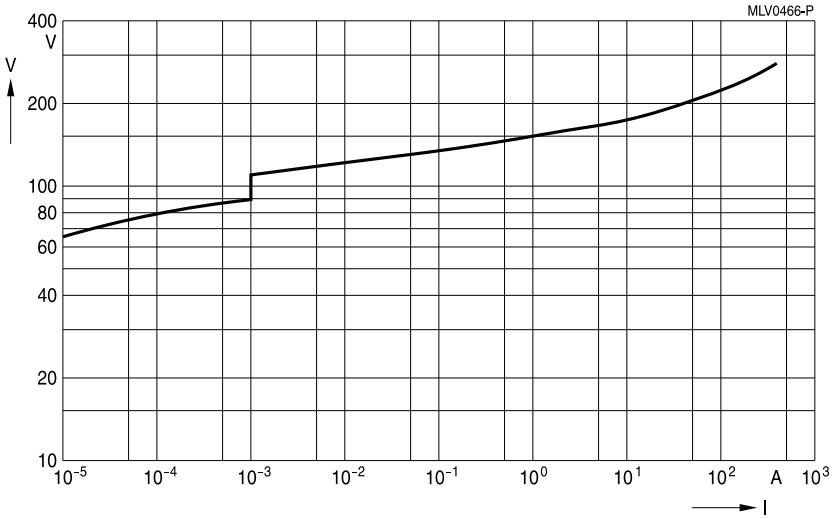
CT1812K40G



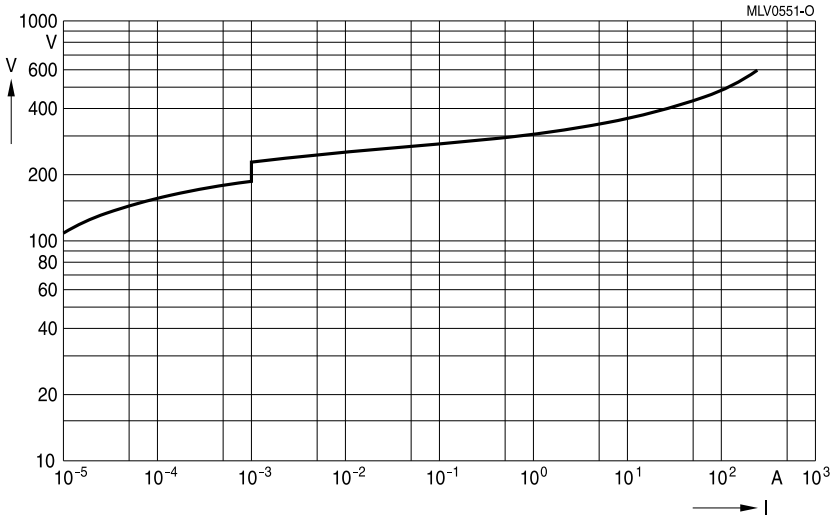
CT1812K50G

SMD

V/I characteristics for surge protection types



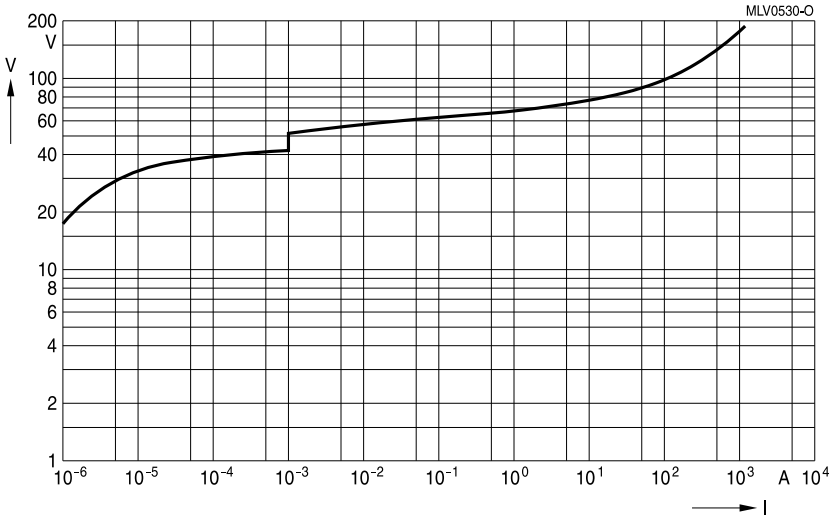
CT1812K60G



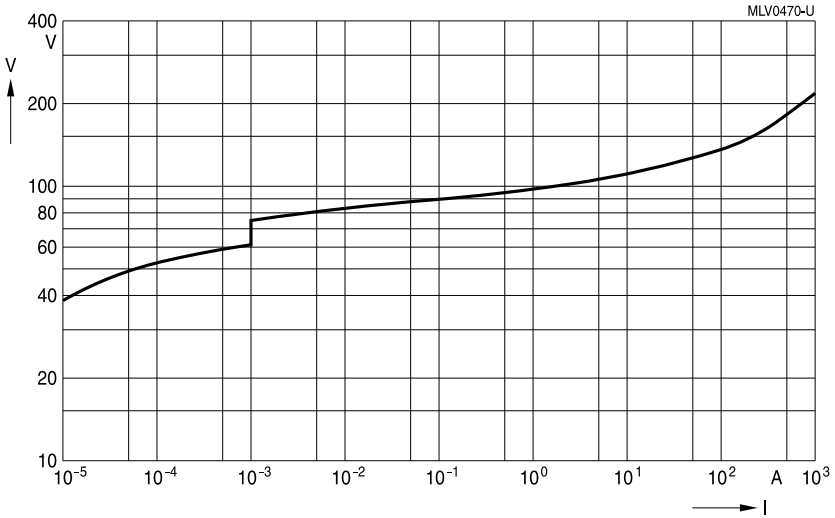
CT1812K130G2

SMD

V/I characteristics for surge protection types



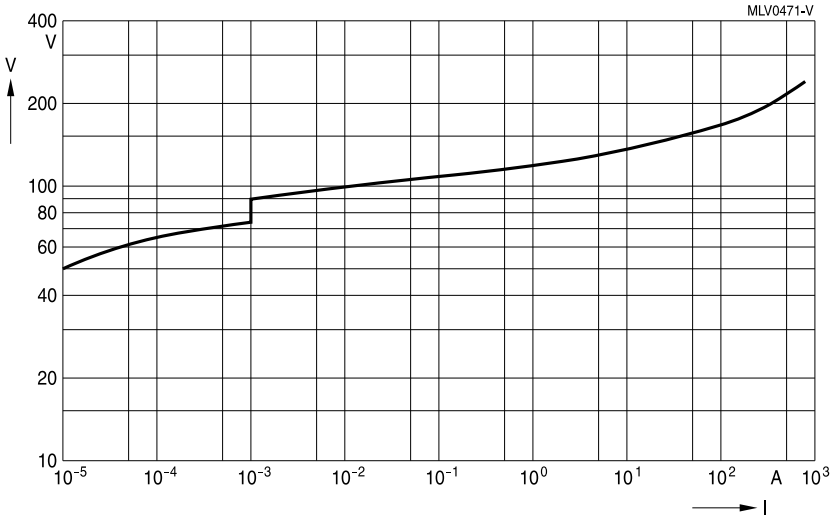
CT2220K30G



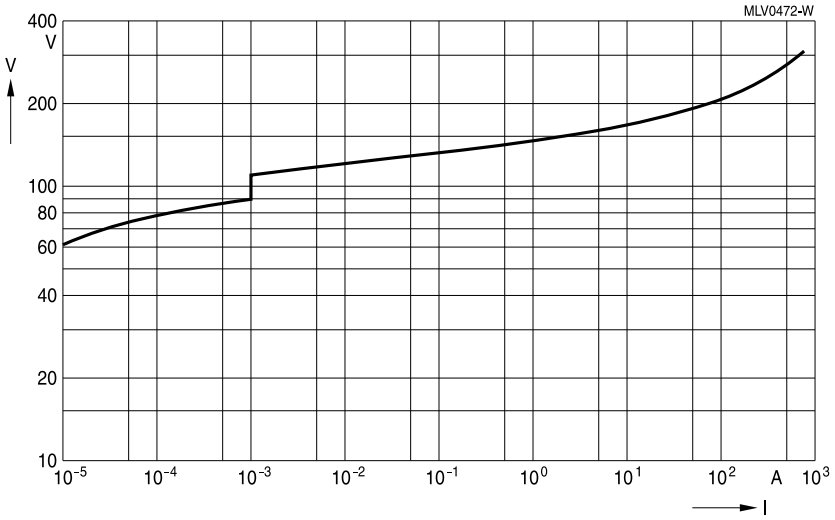
CT2220K40G

SMD

V/I characteristics for surge protection types



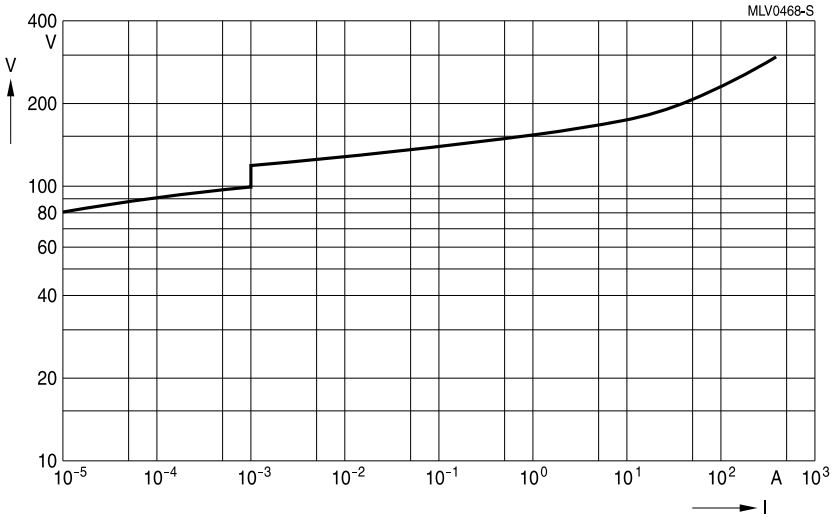
CT2220K50G



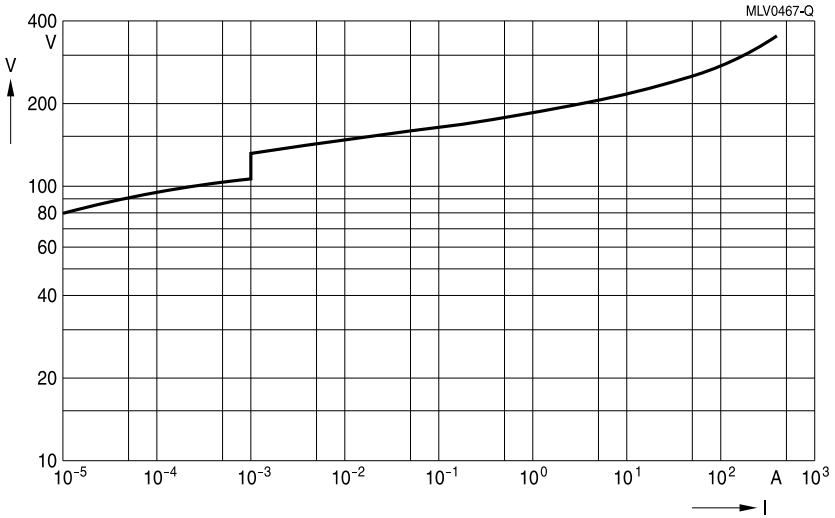
CT2220K60G

SMD

V/I characteristics for telecom types



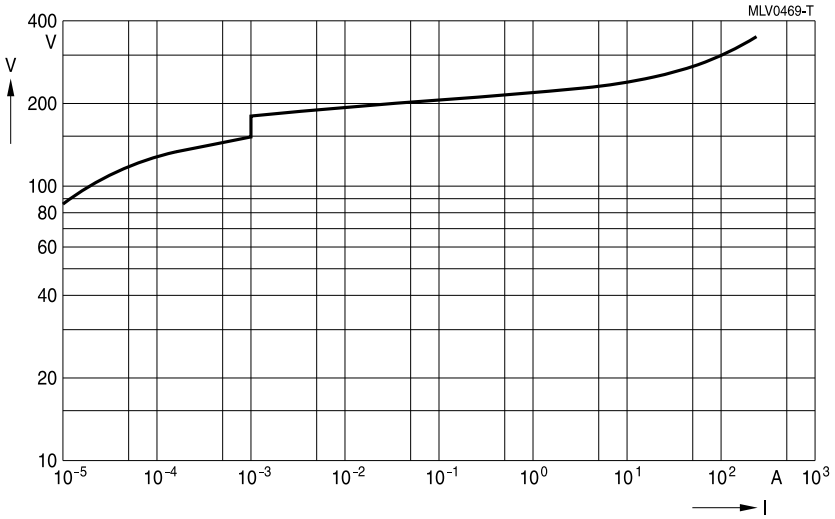
CT1812S60AG2



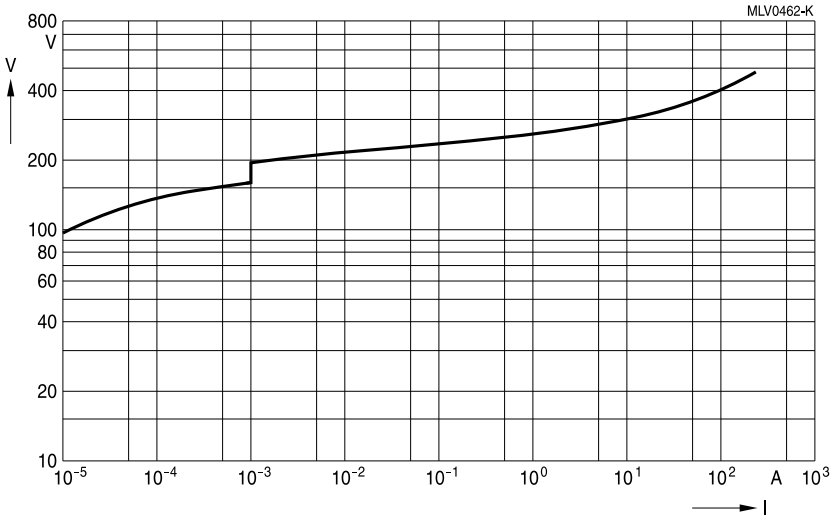
CT1812K75TELEG2

SMD

V/I characteristics for telecom types



CT1812S95AG2

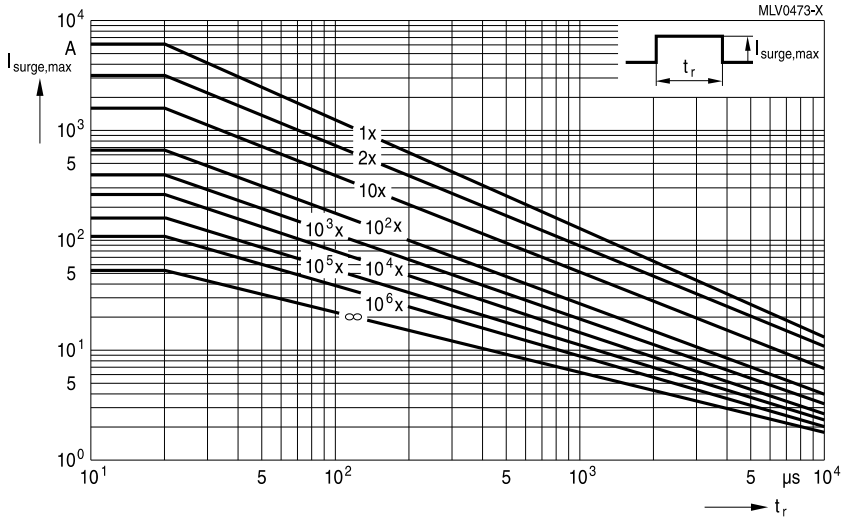


CT1812K115TELEG2

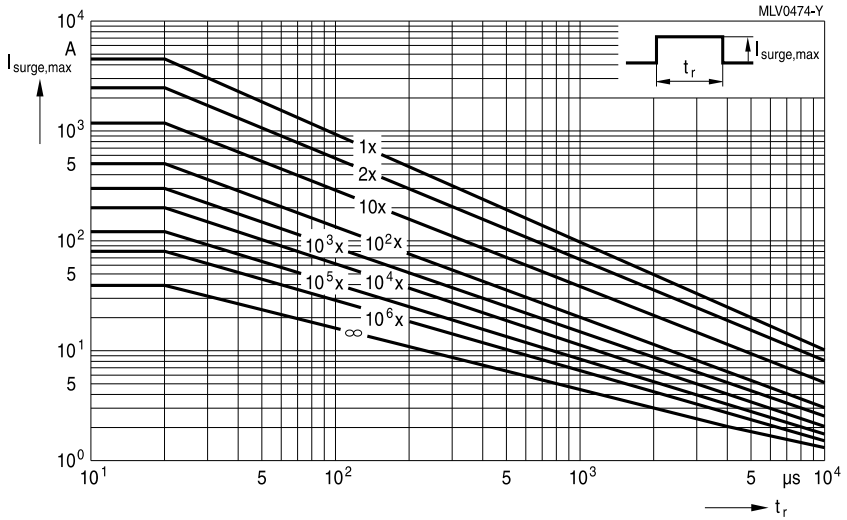
SMD

Derating curves for high surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CN2220K30E2GK2

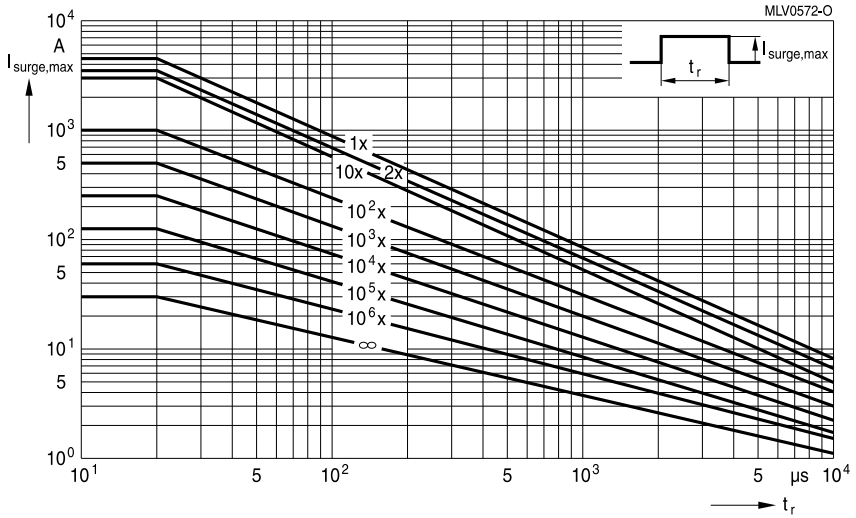


CN2220K50E2GK2, CT2220K50E2G

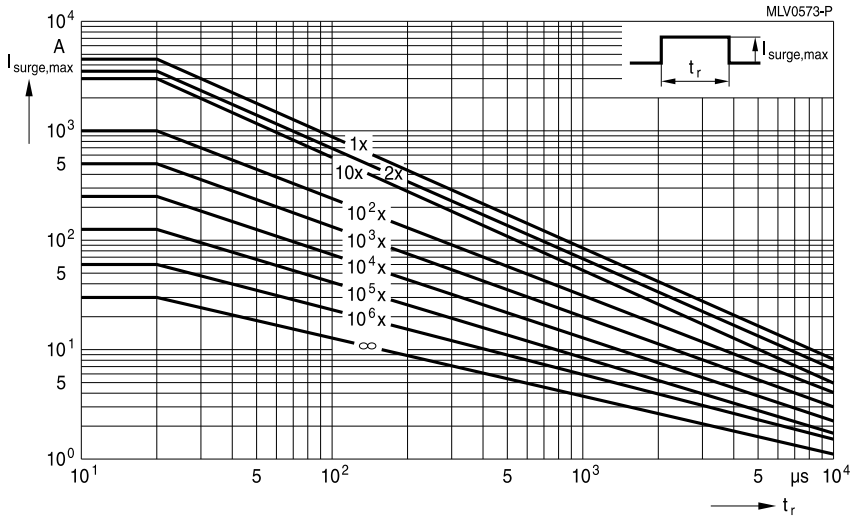
SMD

Derating curves for high surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CN2220S50E2GK2

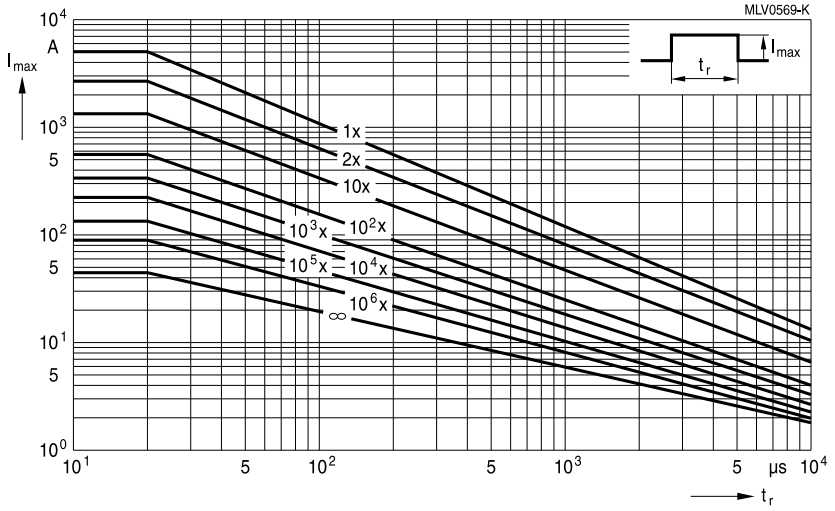


CN2220K60E2GK2

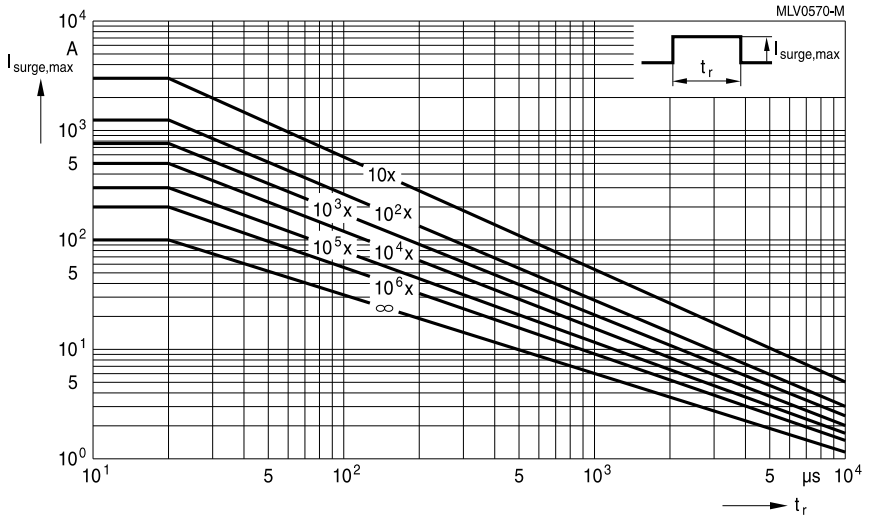
SMD

Derating curves for high surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT2220K30E2G

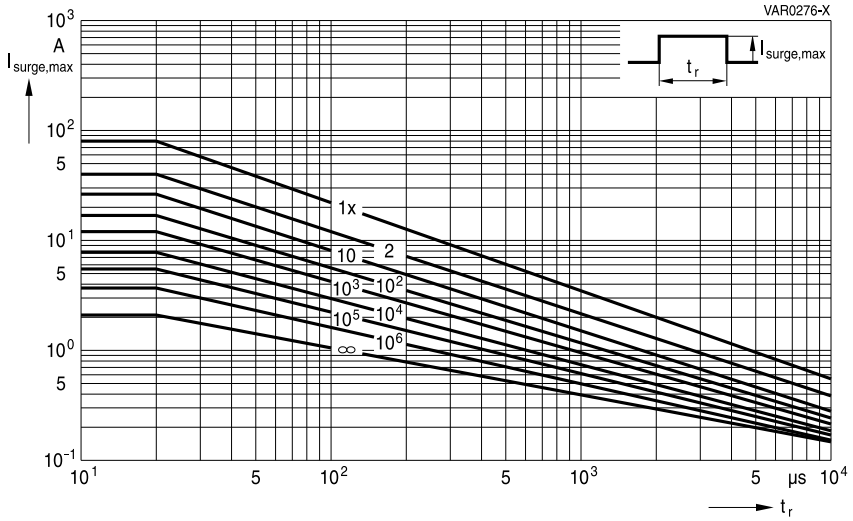


CT2220S50E3G

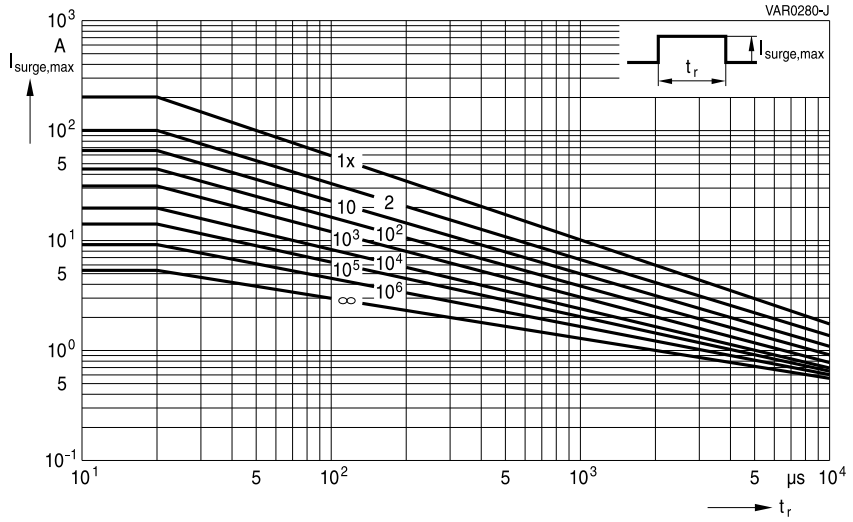
SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT0805K30G CT0805K35G

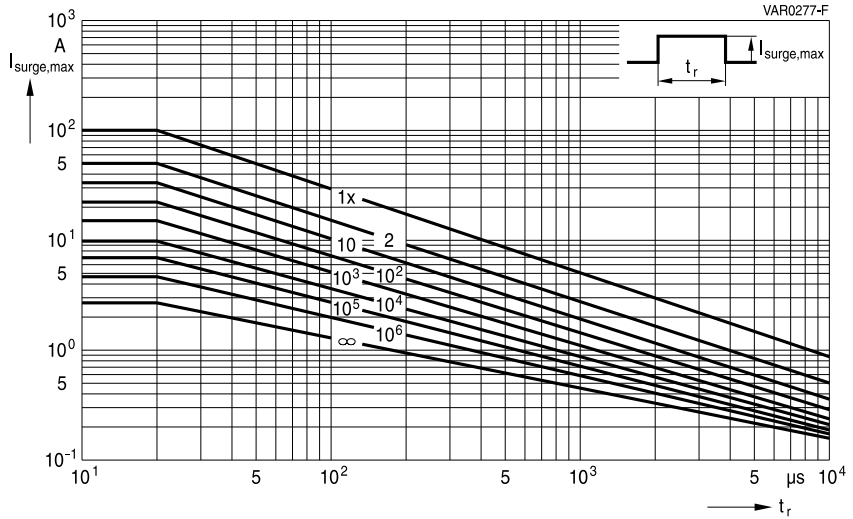


CT1206K30G CT1210K35G ... K60G

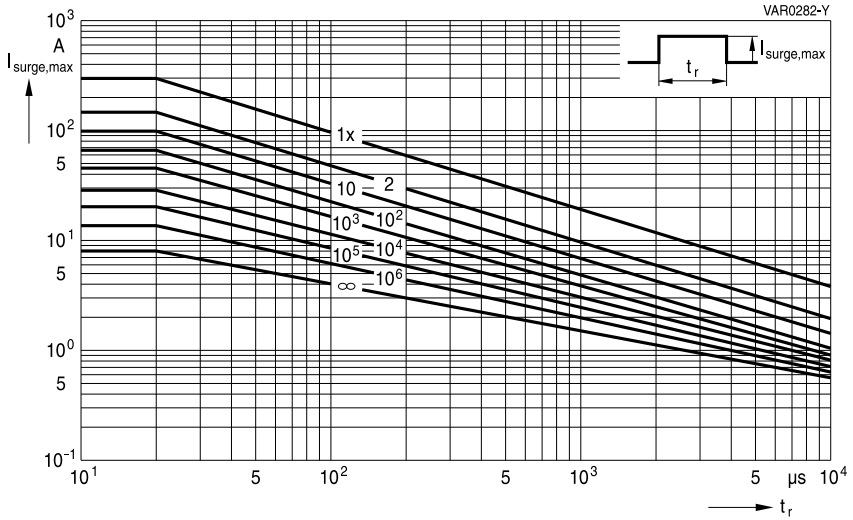
SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT1206K35G ... K60G

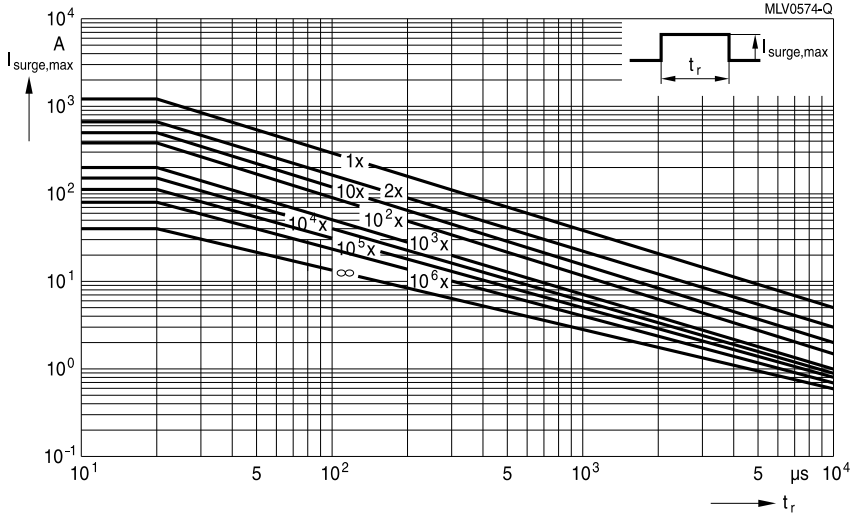


CT1210K30G

SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1

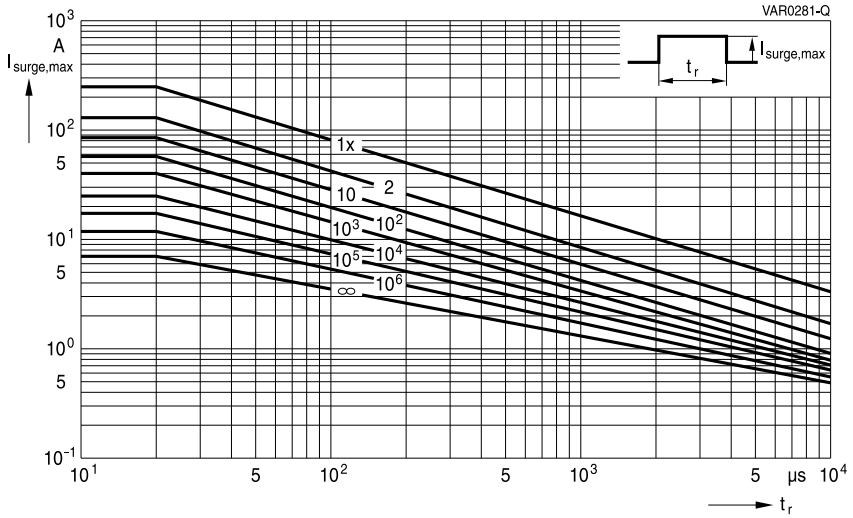


CT1210K50E2G

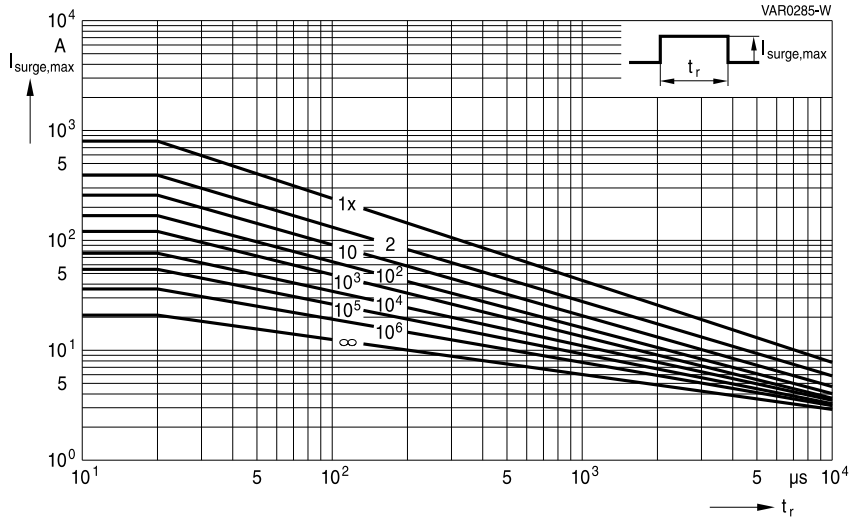
SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT1210K40G CT2220K30G

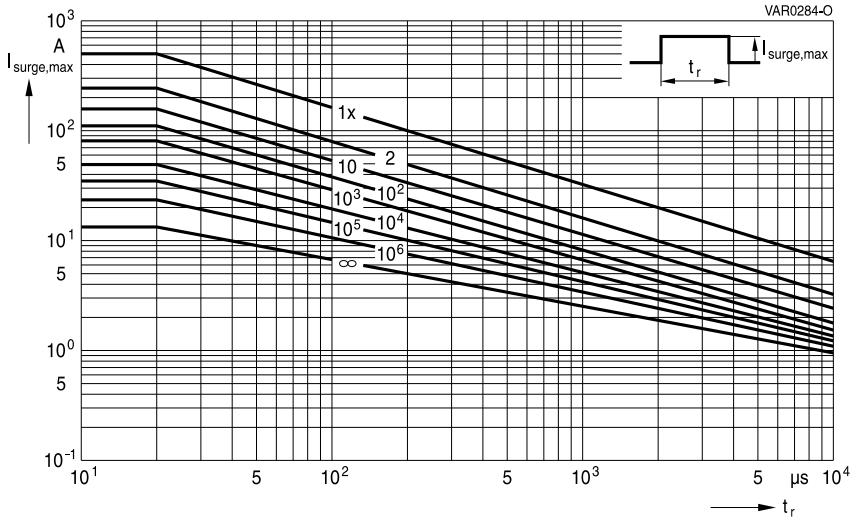


CT1812K30G

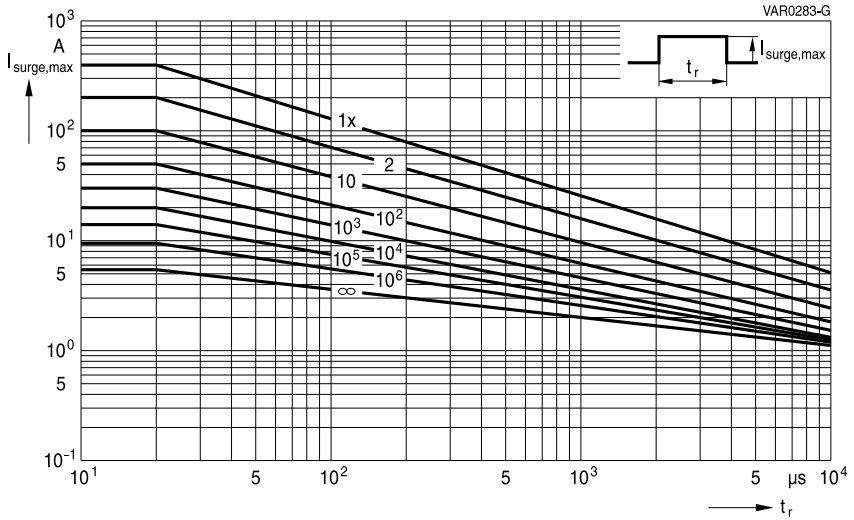
SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT1812K35G ... K40G

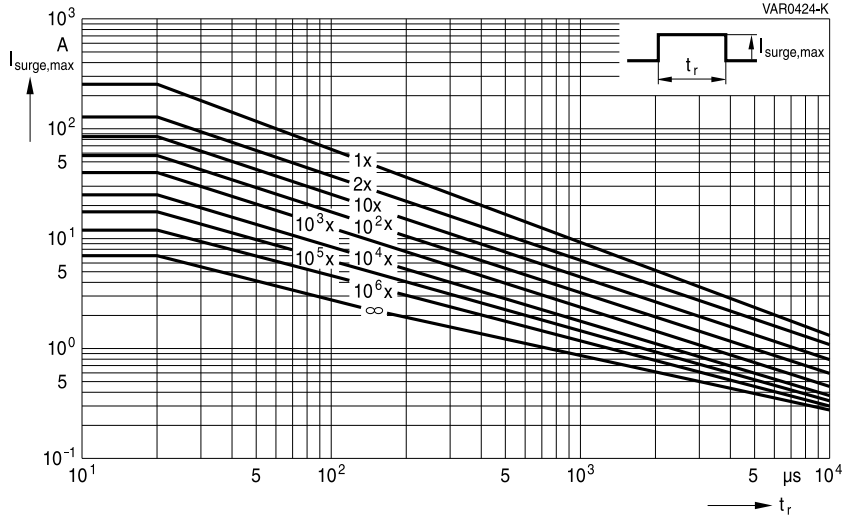


CT1812K50G ... K60G

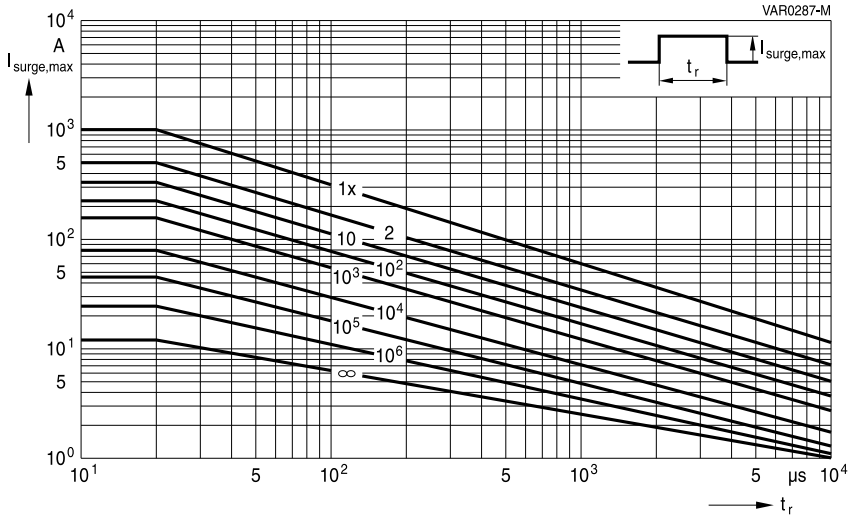
SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT1812K130G2

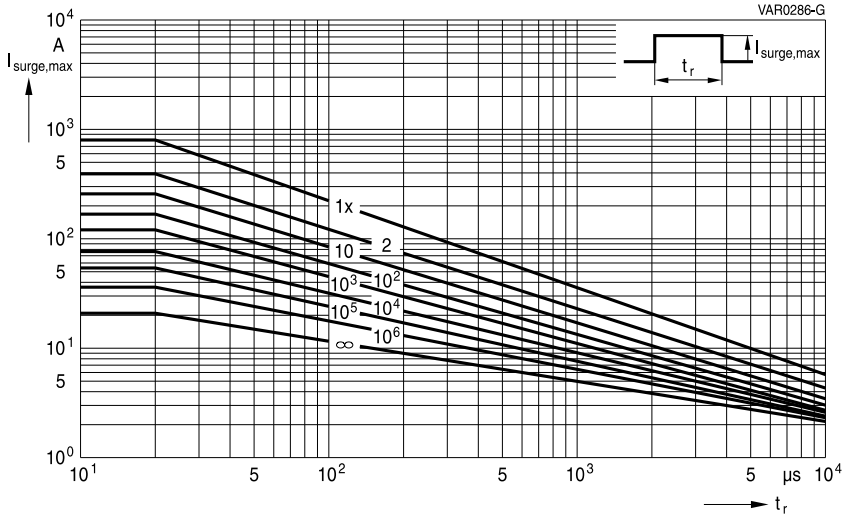


CT2220K40G

SMD

Derating curves for surge protection types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1

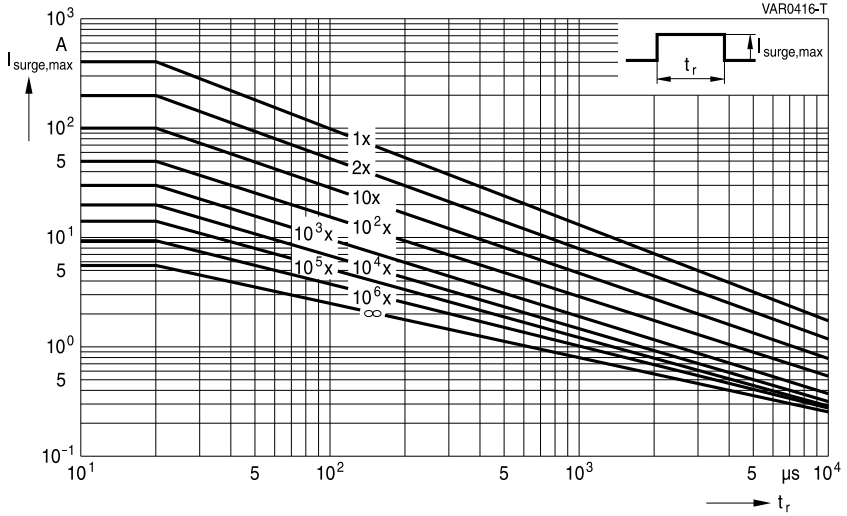


CT2220K50G ... K60G

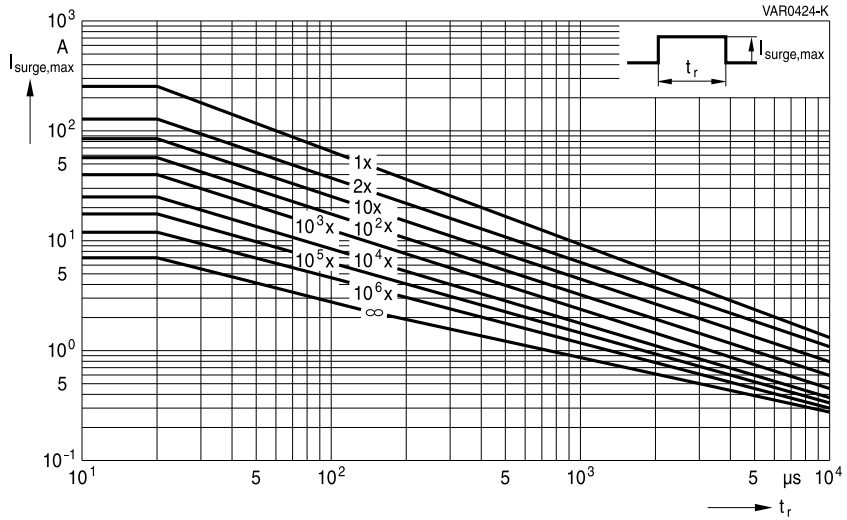
SMD

Derating curves for telecom types

Maximum surge current $I_{surge,max}$ = f (t_r, pulse train)
For explanation of the derating curves refer to "General technical information", chapter 2.7.1



CT1812S60AG2 CT1812K75TELEG2



CT1812S95AG2 CT1812K115TELEG2

SMD

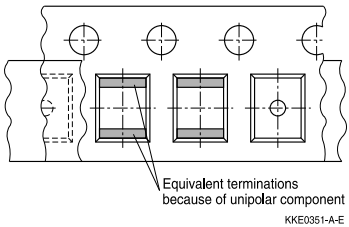
Taping and packing

1 Taping and packing for SMD components

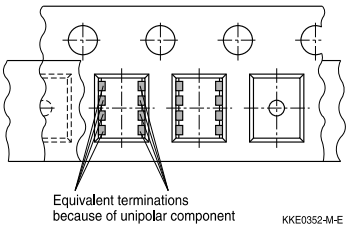
1.1 Blister tape (taping to IEC 60286-3)

Part orientation in tape pocket for blister tape

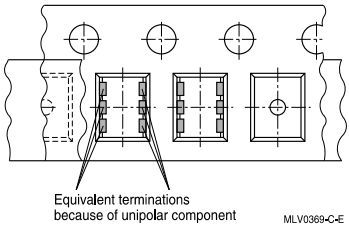
For discrete chip, EIA case sizes 0603, 0805, 1206, 1210, 1812 and 2220



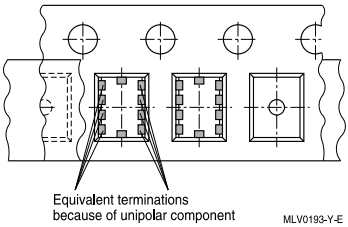
For array, EIA case size 0612



For arrays, EIA case sizes 0506 and 1012



For filter array, EIA case size 0508



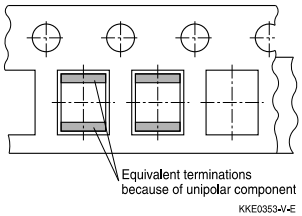
Additional taping information

Reel material	Polystyrol (PS)
Tape material	Polystyrol (PS) or Polycarbonat (PC) or PVC
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N for 8-mm tape and 0.1 to 1.3 N for 12-mm tape at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

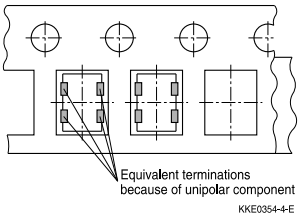
1.2 Cardboard tape (taping to IEC 60286-3)

Part orientation in tape pocket for cardboard tape

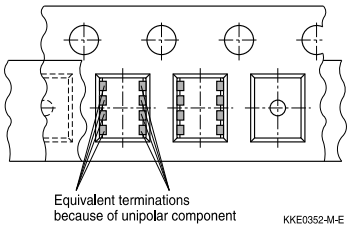
For discrete chip, EIA case sizes 0201, 0402, 0603 and 1003



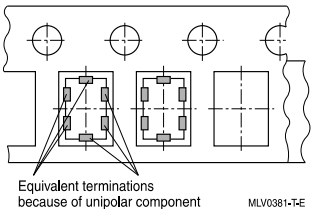
For array, EIA case size 0405



For array, EIA case size 0508



For filter array, EIA case size 0405

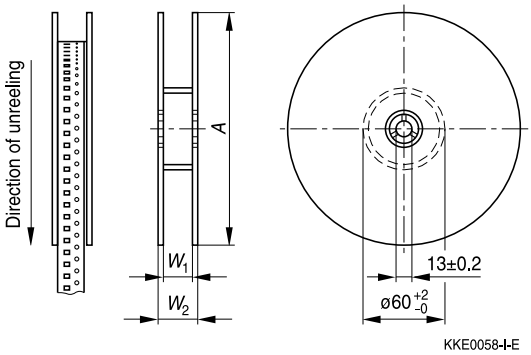


Additional taping information

Reel material	Polystyrol (PS)
Tape material	Cardboard
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

SMD

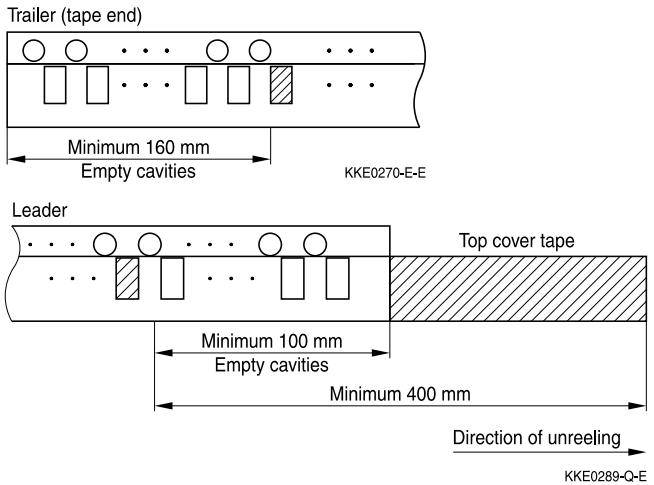
1.3 Reel packing



Dimensions in mm

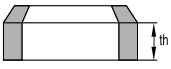
	8-mm tape		12-mm tape	
	180-mm reel	330-mm reel	180-mm reel	330-mm reel
A	180 +0/−3	330 +0/−2.0	180 +0/−3	330 +0/−2.0
W_1	8.4 +1.5/−0	8.4 +1.5/−0	12.4 +1.5/−0	12.4 +1.5/−0
W_2	14.4 max.	14.4 max.	18.4 max.	18.4 max.

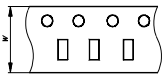
Leader, trailer

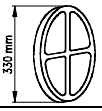


SMD

1.4 Packing units for discrete chip and array chip







Case size	Chip thickness	Cardboard tape	Blister tape	∅ 180-mm reel	∅ 330-mm reel
inch/mm	th	W	W	pcs.	pcs.
0201/0603	0.33 mm	8 mm	–	15000	–
0402/1005	0.6 mm	8 mm	–	10000	50000
0405/1012	0.7 mm	8 mm	–	5000	–
0506/1216	0.5 mm	–	8 mm	4000	–
0508/1220	0.9 mm	8 mm	8 mm	4000	–
0603/1608	0.9 mm	8 mm	8 mm	4000	16000
0612/1632	0.7 mm	–	8 mm	3000	–
0805/2012	0.7 mm	–	8 mm	3000	–
	0.9 mm	–	8 mm	3000	12000
	1.3 mm	–	8 mm	3000	12000
1003/2508	0.9 mm	8 mm	–	4000	–
1012/2532	1.0 mm	–	8 mm	2000	–
1206/3216	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	12000
	1.4 mm	–	8 mm	2000	8000
	1.6 mm	–	8 mm	2000	8000
1210/3225	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	12000
	1.4 mm	–	8 mm	2000	8000
	1.6 mm	–	8 mm	2000	8000
1812/4532	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	1.6 mm	–	12 mm	1000	4000
	2.0 mm	–	12 mm	–	3000
	2.3 mm	–	12 mm	–	3000
2220/5750	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	1.6 mm	–	12 mm	1000	–
	2.0 mm	–	12 mm	–	3000
	2.3 mm	–	12 mm	–	3000
	2.7 mm	–	12 mm	600	–
	3.0 mm	–	12 mm	600	–

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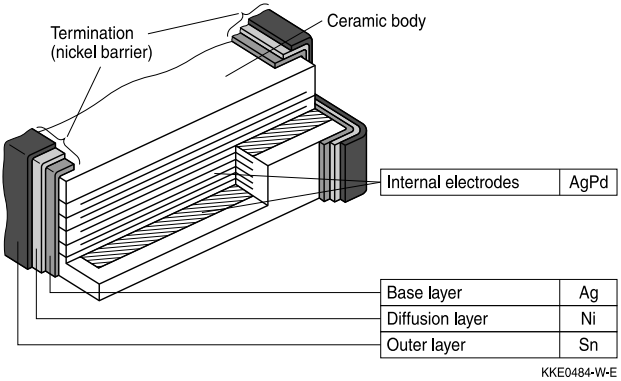
Soldering directions

1 Terminations

1.1 Nickel barrier termination

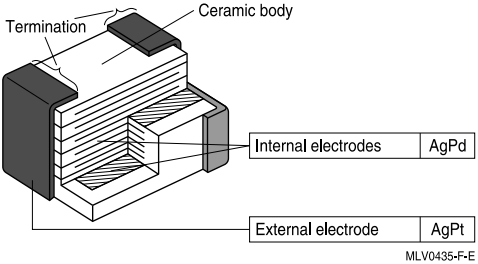
The nickel barrier layer of the silver/nickel/tin termination prevents leaching of the silver base metallization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents the nickel layer from oxidizing and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly-used soldering methods, including lead-free soldering.



Multilayer CTVS: Structure of nickel barrier termination

1.2 Silver-platinum termination

Silver-platinum terminations are mainly used for the large EIA case sizes 1812 and 2220. The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free soldering with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.



Multilayer varistor: Structure of silver-platinum termination

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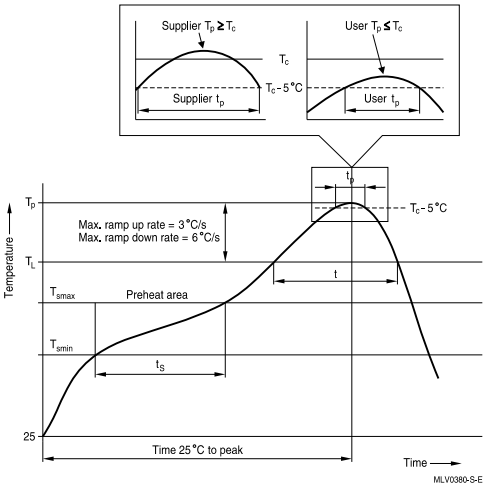
2 Recommended soldering temperature profiles

2.1 Reflow soldering temperature profile

Recommended temperature characteristic for reflow soldering following JEDEC J-STD-020D



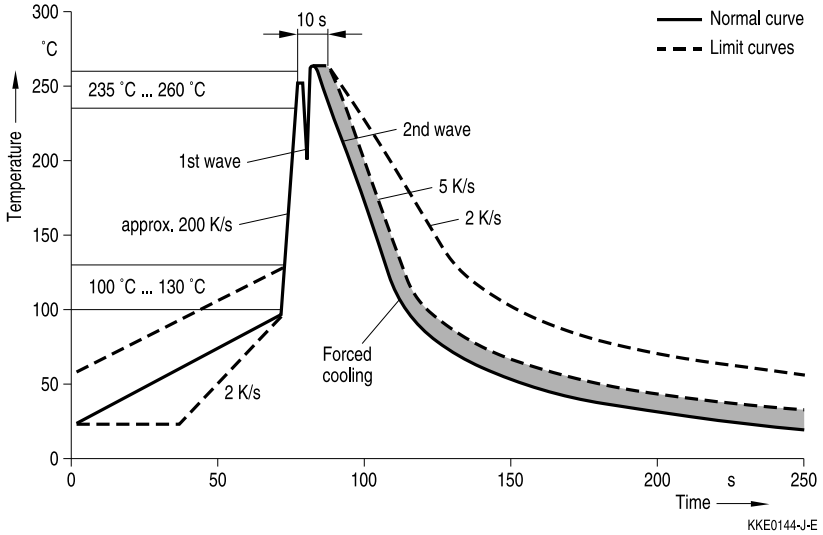
Profile feature		Sn-Pb eutectic assembly	Pb-free assembly
Preheat and soak			
- Temperature min	T_{smin}	100 °C	150 °C
- Temperature max	T_{smax}	150 °C	200 °C
- Time	t_{smin} to t_{smax}	60 ... 120 s	60 ... 180 s
Average ramp-up rate	T_{smax} to T_p	3 °C/ s max.	3 °C/ s max.
Liquidous temperature	T_L	183 °C	217 °C
Time at liquidous	t_L	60 ... 150 s	60 ... 150 s
Peak package body temperature	T_p [1)]	220 °C ... 235 °C[2)]	245 °C ... 260 °C[2)]
Time (t_P)[3)] within 5 °C of specified classification temperature (T_c)		20 s[3)]	30 s[3)]
Average ramp-down rate	T_p to T_{smax}	6 °C/ s max.	6 °C/ s max.
Time 25 °C to peak temperature		maximum 6 min	maximum 8 min

1) Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.
2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.
3) Tolerance for time at peak profile temperature (t_P) is defined as a supplier minimum and a user maximum.

Note: All temperatures refer to topside of the package, measured on the package body surface. Number of reflow cycles: 3

2.2 Wave soldering temperature profile

Temperature characteristics at component terminal with dual-wave soldering



2.3 Lead-free soldering processes

EPCOS multilayer CTVS with AgNiSn termination are designed for the requirements of lead-free soldering processes only.
Soldering temperature profiles to JEDEC J-STD-020D, IEC 60068-2-58 and ZVEI recommendations.

3 Recommended soldering methods - type-specific releases by EPCOS

3.1 Overview

		Reflow soldering		Wave soldering	
Type	EIA case size	SnPb	Lead-free	SnPb	Lead-free
CT... / CD...	0201/ 0402	Approved	Approved	No	No
CT... / CD...	0603 ... 2220	Approved	Approved	Approved	Approved
CN...K2	1812, 2220	Approved	Approved	No	No
Arrays	0405 ... 1012	Approved	Approved	No	No
ESD/EMI filters	0405, 0508	Approved	Approved	No	No
SHCV	-	No	No	Approved	Approved

3.2 Nickel barrier and AgPt terminated multilayer MLVs

All EPCOS MLVs with nickel barrier and AgPt termination are suitable and fully qualiyfied for lead-free soldering. The nickel barrier layer is 100% matte tin-plated.

3.3 Silver-platinum terminated MLVs

The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.

3.4 Tinned iron wire

All EPCOS SHCV types with tinned termination are approved for lead-free and SnPb soldering.

4 Solder joint profiles / solder quantity

4.1 Nickel barrier termination

If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations.

If the solder meniscus is too high, i.e. the solder quantity is too large, the vise effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break, as in a vise.

The figures below show good and poor solder joints for dual-wave and infrared soldering.

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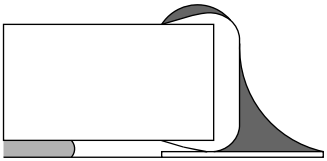
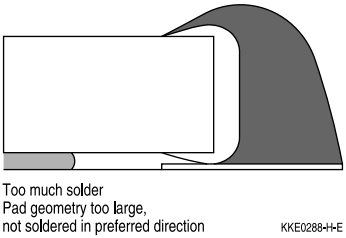
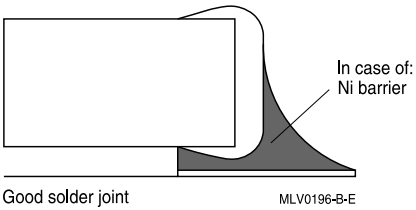
4.1.1 Solder joint profiles for nickel barrier termination - dual-wave soldering

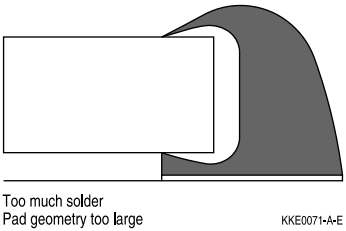


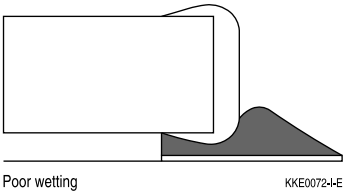


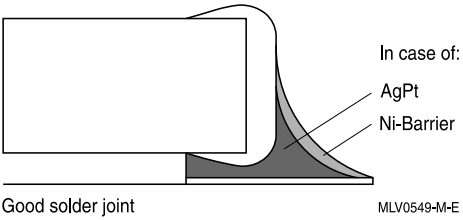
Good and poor solder joints caused by amount of solder in dual-wave soldering.

4.1.2 Solder joint profiles for nickel barrier termination / silver-platinum termination - reflow soldering









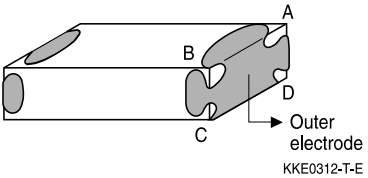
Good and poor solder joints caused by amount of solder in reflow soldering.

5 Solderability tests

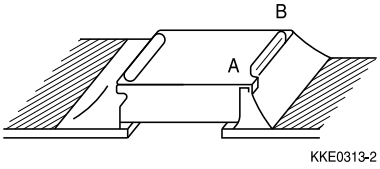
Test	Standard	Test conditions Sn-Pb soldering	Test conditions Pb-free soldering	Criteria/ test results
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ±3 °C for 3 ±0.3 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux at 245 ±5 °C for 3 ±0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 260 ±5 °C for 10 ±1 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux without preheating at 255 ±5 °C for 10 ±1 s	No leaching of contacts
Thermal shock (solder shock)		Dip soldering at 300 °C/5 s	Dip soldering at 300 °C/5 s	No deterioration of electrical parameters. Capacitance change: $\lvert\Delta C/C_0\rvert \leq 15\%$
Tests of resistance to soldering heat for SMDs	IEC 60068-2-58	Immersion in 60/40 SnPb for 10 s at 260 °C	Immersion in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $\lvert\Delta V/V\ (1\ mA)\rvert \leq 5\%$
Tests of resistance to soldering heat for radial leaded components (SHCV)	IEC 60068-2-20	Immersion of leads in 60/40 SnPb for 10 s at 260 °C	Immersion of leads in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $\lvert\Delta V/V\ (1\ mA)\rvert \leq 5\%$ Change of capacitance X7R: $\leq -5/+10\%$

Note:
Leaching of the termination

Effective area at the termination might be lost if the soldering temperature and/or immersion time are not kept within the recommended conditions. Leaching of the outer electrode should not exceed 25% of the chip end area (full length of the edge A-B-C-D) and 25% of the length A-B, shown below as mounted on substrate.



As a single chip



As mounted on substrate

6 Notes for proper soldering

6.1 Preheating and cooling

- According to JEDEC J-STD-020D. Please refer to section 2 of this chapter.

6.2 Repair/ rework

Manual soldering with a soldering iron must be avoided, hot-air methods are recommended for rework purposes.

6.3 Cleaning

All environmentally compatible agents are suitable for cleaning. Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metallized surfaces.

6.4 Solder paste printing (reflow soldering)

An excessive application of solder paste results in too high a solder fillet, thus making the chip more susceptible to mechanical and thermal stress. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface.

6.5 Selection of flux

Used flux should have less than or equal to 0.1 wt % of halogenated content, since flux residue after soldering could lead to corrosion of the termination and/or increased leakage current on the surface of the component. Strong acidic flux must not be used. The amount of flux applied should be carefully controlled, since an excess may generate flux gas, which in turn is detrimental to solderability.

6.6 Storage of CTVSs

Solderability is guaranteed for one year from date of delivery for multilayer varistors, CeraDiodes and ESD/EMI filters (half a year for chips with AgPt terminations) and two years for SHCV components, provided that components are stored in their original packages.

Storage temperature: −25 °C to +45 °C

Relative humidity: ≤75% annual average, ≤95% on 30 days a year

The solderability of the external electrodes may deteriorate if SMDs and leaded components are stored where they are exposed to high humidity, dust or harmful gas (hydrogen chloride, sulfurous acid gas or hydrogen sulfide).

Do not store SMDs and leaded components where they are exposed to heat or direct sunlight. Otherwise the packing material may be deformed or SMDs/ leaded components may stick together, causing problems during mounting.

After opening the factory seals, such as polyvinyl-sealed packages, it is recommended to use the SMDs or leaded components as soon as possible.

Solder CTVS components after shipment from EPCOS within the time specified:

CTVS with Ni barrier termination:	12 months
CTVS with AgPt termination:	6 months
SHCV (leaded components):	24 months

6.7 Placement of components on circuit board

Especially in the case of dual-wave soldering, it is of advantage to place the components on the board before soldering in that way that their two terminals do not enter the solder bath at different times.
Ideally, both terminals should be wetted simultaneously.

6.8 Soldering cautions

- An excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion and a change of electrical properties of the varistor due to the loss of contact between electrodes and termination.
- Wave soldering must not be applied for MLVs designated for reflow soldering only (see table "Overview", section 3.1).
- Keep the recommended down-cooling rate.

6.9 Standards

CECC 00802

IEC 60068-2-58

IEC 60068-2-20

JEDEC J-STD-020D

Symbols and terms

For ceramic transient voltage suppressors (CTVS)

Symbol	Term
$C_{line,max}$	Maximum capacitance per line
$C_{line,min}$	Minimum capacitance per line
$C_{line,typ}$	Typical capacitance per line
C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
C_{nom}	Nominal capacitance
ΔC_{nom}	Tolerance of nominal capacitance
C_{typ}	Typical capacitance
$f_{cut-off,max}$	Maximum cut-off frequency
$f_{cut-off,min}$	Minimum cut-off frequency
$f_{cut-off,typ}$	Typical cut-off frequency
$f_{res,typ}$	Typical resonance frequency
I	Current
I_{clamp}	Clamping current
I_{leak}	Leakage current
$I_{leak,max}$	Maximum leakage current
$I_{leak,typ}$	Typical leakage current
I_{PP}	Peak pulse current
$I_{surge,max}$	Maximum surge current (also termed peak current)
LCT	Lower category temperature
L_{typ}	Typical inductance
$P_{diss,max}$	Maximum power dissipation
P_{PP}	Peak pulse power
R_{ins}	Insulation resistance
R_{min}	Minimum resistance
R_S	Resistance per line
$R_{S,typ}$	Typical resistance per line
T_A	Ambient temperature
T_{op}	Operating temperature
$T_{op,max}$	Maximum operating temperature
T_{stg}	Storage temperature

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Symbol	Term
t_r	Duration of equivalent rectangular wave
t_{resp}	Response time
$t_{resp,max}$	Maximum response time
UCT	Upper category temperature
V	Voltage
$V_{BR,min}$	Minimum breakdown voltage
$V_{clamp,max}$	Maximum clamping voltage
$V_{DC,max}$	Maximum DC operating voltage (also termed working voltage)
$V_{ESD,air}$	Air discharge ESD capability
$V_{ESD,contact}$	Contact discharge ESD capability
V_{jump}	Maximum jump-start voltage
$V_{RMS,max}$	Maximum AC operating voltage, root-mean-square value
V_V	Varistor voltage (also termed breakdown voltage)
V_{LD}	Maximum load dump voltage
V_{leak}	Measurement voltage for leakage current
$V_{V,min}$	Minimum varistor voltage
$V_{V,max}$	Maximum varistor voltage
ΔV_V	Tolerance of varistor voltage
W_{LD}	Maximum load dump energy
W_{max}	Maximum energy absorption (also termed transient energy)
α_{typ}	Typical insertion loss
tan δ	Dissipation factor
e	Lead spacing
≪*≫	Maximum possible application conditions

All dimensions are given in mm.
The commas used in numerical values denote decimal points.

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Cautions and warnings

General

Some parts of this publication contain statements about the suitability of our ceramic transient voltage suppressor (CTVS) components (multilayer varistors (MLVs)), CeraDiodes, ESD/EMI filters, leaded transient voltage/ RFI suppressors (SHCV types)) for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CTVS devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CTVS components for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CTVS devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CTVS components for purposes not identified in our specifications, application notes and data books.
- Ensure the suitability of a CTVS in particular by testing it for reliability during design-in. Always evaluate a CTVS component under worst-case conditions.
- Pay special attention to the reliability of CTVS devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Always connect a CTVS in parallel with the electronic circuit to be protected.
- Consider maximum rated power dissipation if a CTVS has insufficient time to cool down between a number of pulses occurring within a specified isolated time period. Ensure that electrical characteristics do not degrade.
- Consider derating at higher operating temperatures. Choose the highest voltage class compatible with derating at higher temperatures.
- Surge currents beyond specified values will puncture a CTVS. In extreme cases a CTVS will burst.
- If steep surge current edges are to be expected, make sure your design is as low-inductance as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure. Only use CTVS components from the automotive series in safety-relevant applications.

- Specified values only apply to CTVS components that have not been subject to prior electrical, mechanical or thermal damage. The use of CTVS devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures like thermal fuses.

Storage

- Only store CTVS in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 to +45°C, relative humidity ≤75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CTVS devices where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CTVS may stick together, causing problems during mounting.
- Avoid contamination of the CTVS surface during storage, handling and processing.
- Avoid storing CTVS devices in harmful environments where they are exposed to corrosive gases for example (SO_x, Cl).
- Use CTVS as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CTVS components after shipment from EPCOS within the time specified:
  - CTVS with Ni barrier termination, 12 months
  - CTVS with AgPt termination, 6 months
  - SHCV, 24 months

Handling

- Do not drop CTVS components and allow them to be chipped.
- Do not touch CTVS with your bare hands - gloves are recommended.
- Avoid contamination of the CTVS surface during handling.
- Washing processes may damage the product due to the possible static or cyclic mechanical loads (e.g. ultrasonic cleaning). They may cause cracks to develop on the product and its parts, which might lead to reduced reliability or lifetime.

Mounting

- When CTVS devices are encapsulated with sealing material or overmolded with plastic material, electrical characteristics might be degraded and the life time reduced.
- Make sure an electrode is not scratched before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CTVS components are clean before mounting.
- The surface temperature of an operating CTVS can be higher. Ensure that adjacent components are placed at a sufficient distance from a CTVS to allow proper cooling.
- Avoid contamination of the CTVS surface during processing.

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Soldering

- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.

Operation

- Use CTVS only within the specified operating temperature range.
- Use CTVS only within specified voltage and current ranges.
- Environmental conditions must not harm a CTVS. Only use them in normal atmospheric conditions. Reducing the atmosphere (e.g. hydrogen or nitrogen atmosphere) is prohibited.
- Prevent a CTVS from contacting liquids and solvents. Make sure that no water enters a CTVS (e.g. through plug terminals).
- Avoid dewing and condensation.
- EPCOS CTVS components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content
- EPCOS CTVS devices are not suitable for switching applications or voltage stabilization where static power dissipation is required.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

Display of ordering codes for EPCOS products

The ordering code for one and the same EPCOS product can be represented differently in data sheets, data books, other publications, on the EPCOS website, or in order-related documents such as shipping notes, order confirmations and product labels. **The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products**. Detailed information can be found on the Internet under www.epcos.com/orderingcodes

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.
5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.

   We also **reserve the right to discontinue production and delivery of products**. Consequently, we cannot guarantee that all products named in this publication will always be available. The aforementioned does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.
6. Unless otherwise agreed in individual contracts, **all orders are subject to our General Terms and Conditions of Supply.**
7. **Our manufacturing sites serving the automotive business apply the IATF 16949 standard.** The IATF certifications confirm our compliance with requirements regarding the quality management system in the automotive industry. Referring to customer requirements and customer specific requirements (“CSR”) TDK always has and will continue to have the policy of respecting individual agreements. Even if IATF 16949 may appear to support the acceptance of unilateral requirements, we hereby like to emphasize that **only requirements mutually agreed upon can and will be implemented in our Quality Management System.** For clarification purposes we like to point out that obligations from IATF 16949 shall only become legally binding if individually agreed upon.

8. The trade names EPCOS, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, ExoCore, FilterCap, FormFit, LeaXield, MiniBlue, MiniCell, MKD, MKK, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, ThermoFuse, WindCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

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