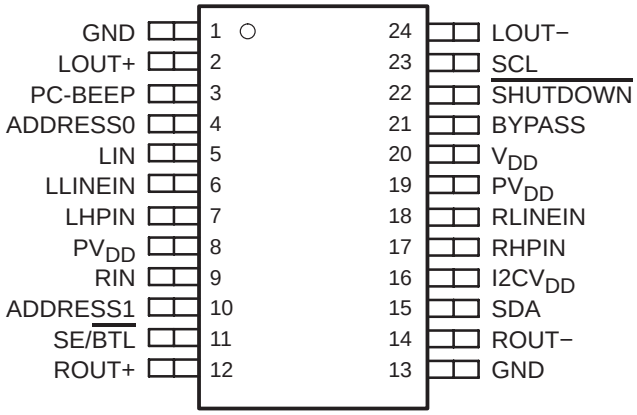
- **I²C Bus Controllable**
- **2-W/Ch Output Power Into 4-Ω Load**
- **Low Supply Current and Shutdown Current**
- **Depop Circuitry**
- **Digital Volume Control From 20 dB to −60 dB**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Fully Differential Input**
- **Stereo Input MUX**
- **PC-Beep Input**
- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0172 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 4-Ω loads. This device utilizes the I²C bus to control its functionality, which minimizes the number of external components needed, simplifies the design, and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0172 has less than 0.2% THD+N from 20 Hz to 20 kHz.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers at power up, power down, and while transitioning in and out of shutdown mode.

The overall gain of the amplifier is controlled digitally by the volume control registers which are programmed via the I²C interface. At power up, the amplifier defaults to –60 dB in BTL mode, or –66 dB in SE mode. There are four registers that contain the gains: left BTL, right BTL, left SE, and right SE. Each register contains six bits, which allows 64 gain steps from –60 dB to 20 dB in 1.25-dB steps, and two bits that mute the amplifier.

The TPA0172 only consumes 6.5 mA of supply current during normal operation. A shutdown mode is included that reduces supply current to less than 15 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable on TO-200-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0172 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
−40°C to 85°C	TPA0172PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0172PWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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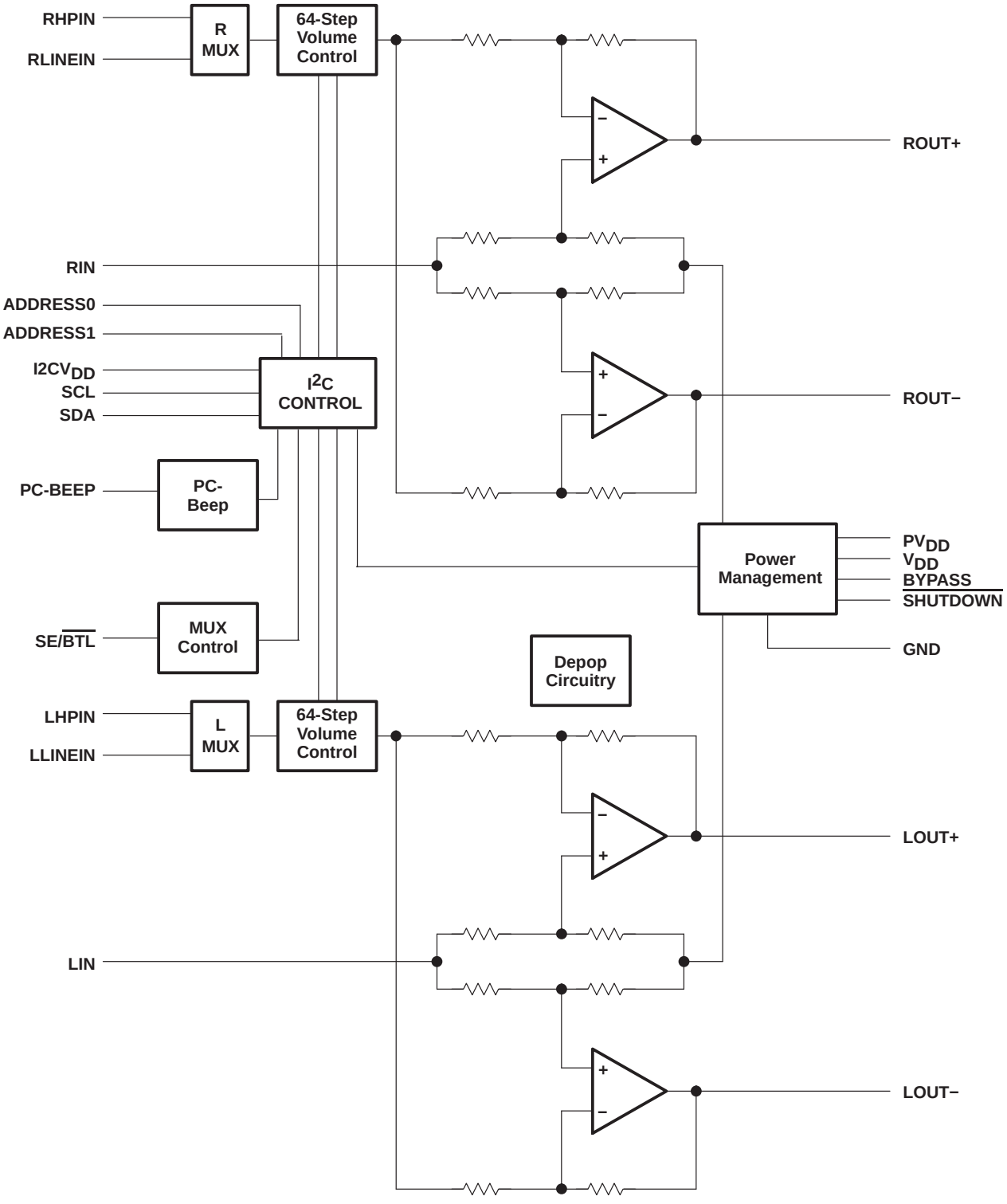
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS0	4	I	Bit 0 of user-setable portion of device's I2C address.
ADDRESS1	10	I	Bit 1 of user-setable portion of device's I2C address.
BYPASS	21		Tap to voltage divider for internal midsupply bias generator.
GND	1, 13		Ground connection for circuitry. Connect to thermal pad
LHPIN	7	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high, or programmed via I2C.
LIN	5	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	6	I	Left-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low, or programmed via I2C.
LOUT+	2	O	Left-channel positive output in BTL mode, and positive output in SE mode.
LOUT−	24	O	Left-channel negative output in BTL mode, and high impedance in SE mode.
PC-BEEP	3	I	The input for PC-BEEP mode which is enabled when a > 1-V (peak-to-peak) square wave is input to this terminal, when PCB ENABLE is held high, or programmed via I2C. If not used, ground this terminal.
$I2CV_{DD}$	16	I	The voltage on this terminal sets the trip points for the I2C interface. If the system I2C bus is running at 3.3 V, then tie this terminal to 3.3 V. If the system I2C bus is running at 5 V, then tie this terminal to 5 V.
PV_{DD}	8, 19	I	Power supply
RHPIN	17	I	Right-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high, or programmed via I2C.
RIN	9	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	18	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low, or programmed via I2C.
ROUT+	12	O	Right-channel positive output in BTL mode, and positive output in SE mode.
ROUT−	14	O	Right-channel negative output in BTL mode, and high impedance in SE mode.
SCL	23	I	I2C clock line
SDA	15		Serial data line of the I2C bus. Pullup resistor must comply with the I2C standard: minimum value = 3 kΩ, maximum value = 19 kΩ. Pull up to $I2CV_{DD}$
SE/$\overline{\text{BTL}}$	11	I	Input MUX control input. When this terminal is held high, the LHPIN or $\overline{\text{RHPIN}}$, and the SE output are selected. When this terminal is held low, the LLINEIN or RLINEIN, and the $\overline{\text{BTL}}$ output are selected. This functionality can also be programmed via I2C.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the device in the shutdown mode, except for the PC-BEEP input and the I2C bus.
V_{DD}	20	I	Power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Bus voltage, $I2CV_{DD}$ . . . . . 6 V
Input voltage, V_I . . . . . −0.3 V to V_{DD} 0.3 V
Continuous total power dissipation . . . . . Internally Limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Operating junction temperature range, T_J . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ See the Texas Instruments document, *PowerPAD™ Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD™* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
Bus voltage, $I2CV_{DD}$ (see Note1)		3	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
	ADDRESS0, ADDRESS1	3.5		
	SDA, SCL	0.7 $I2CV_{DD}$		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
	ADDRESS0, ADDRESS1		0.8	
	SDA, SCL		0.3 $I2CV_{DD}$	
Operating free-air temperature, T_A		−40	85	°C

NOTE 1: $I2CV_{DD}$ must be less than or equal to V_{DD}.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 20 dB			20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.5 V to 5.5 V		75		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			1	µA
Z_i	Input impedance		7.5			kΩ
I_{DD}	Supply current	BTL mode		8	12	mA
$I_{DD(SD)}$	Supply current, shutdown mode	PC-BEEP = 0 V		15	35	µA
		PC-BEEP = V_{DD}/2		50	90	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 20 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.08%, f = 1 kHz			2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 20 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	THD = 1%			>20		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		−58		dB
			SE mode		−52		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz, Gain = 6 dB BTL, 0 dB SE	BTL mode		29		μV_{RMS}
			SE mode		23		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 2, 4, 6
		vs Frequency	3, 5,
V_n	Output noise voltage	vs Frequency	7
	Supply ripple rejection ratio	vs Frequency	8, 9
	Crosstalk	vs Frequency	10, 11
	Shutdown attenuation	vs Frequency	12
	Closed loop response		13, 14
P_O	Output power	vs Load resistance	15, 16
P_D	Power dissipation	vs Output power	17, 18
		vs Ambient temperature	19

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

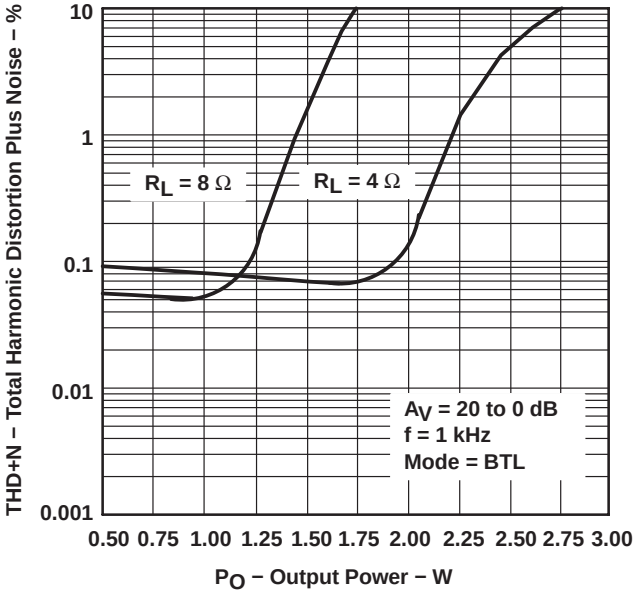


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

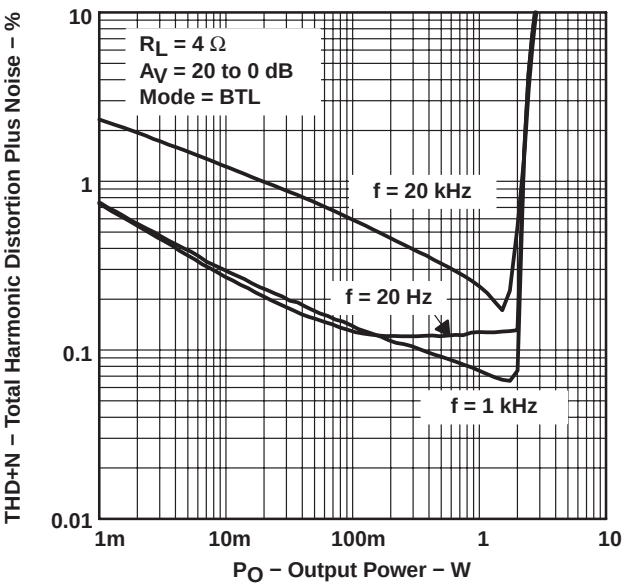


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

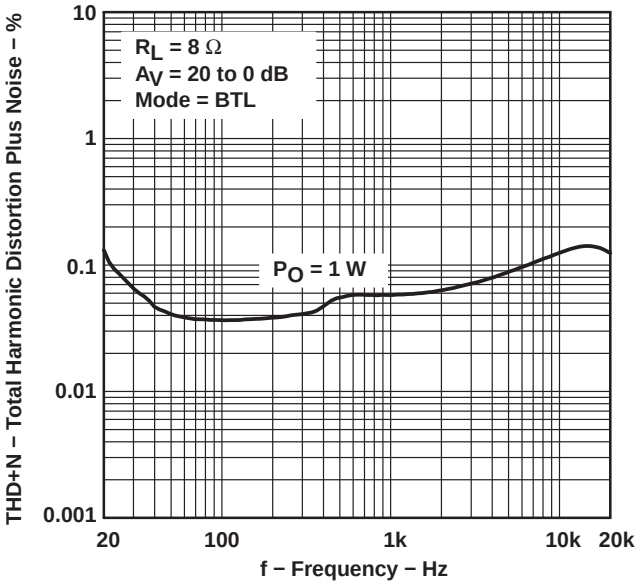


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

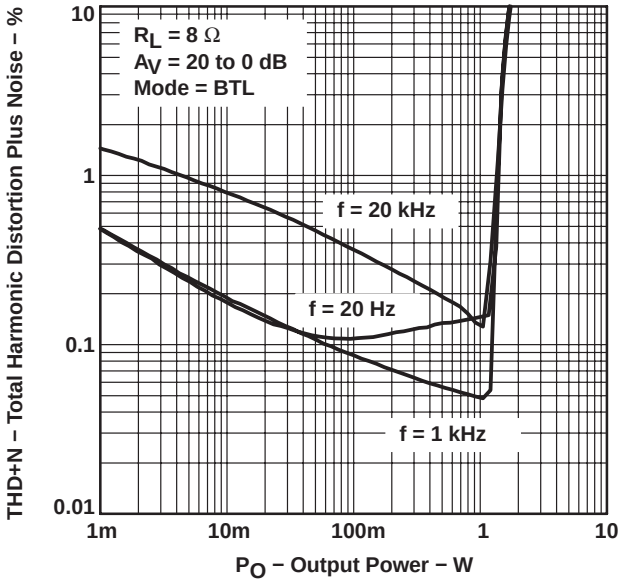


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

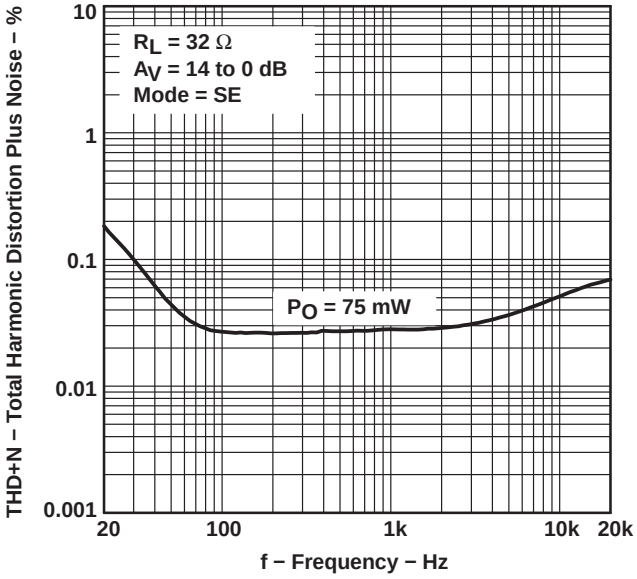


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

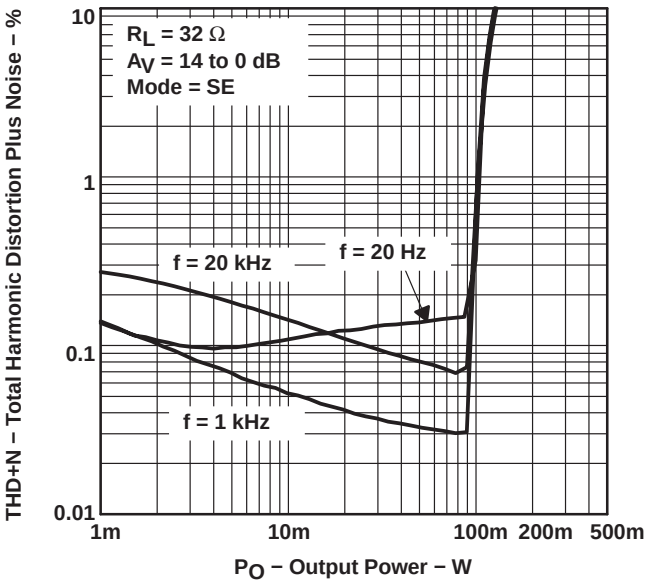


Figure 6

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

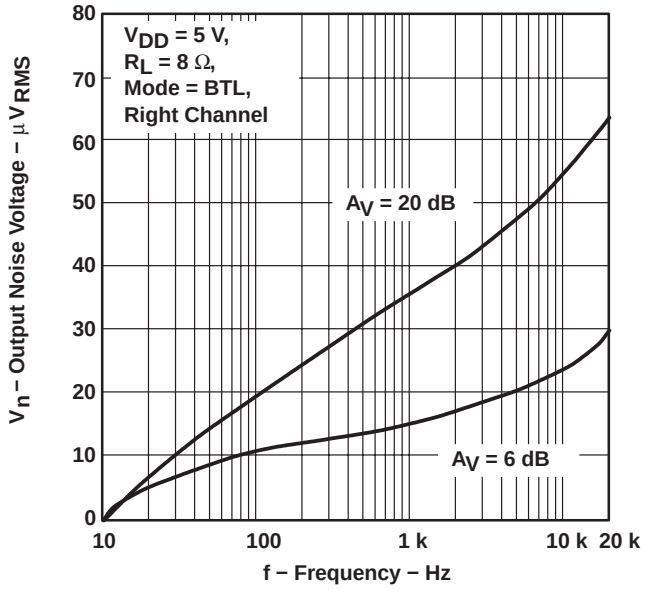


Figure 7

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

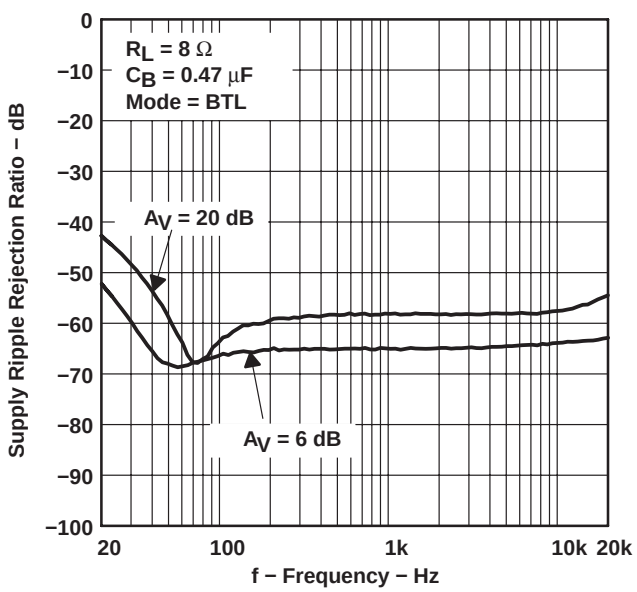


Figure 8

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

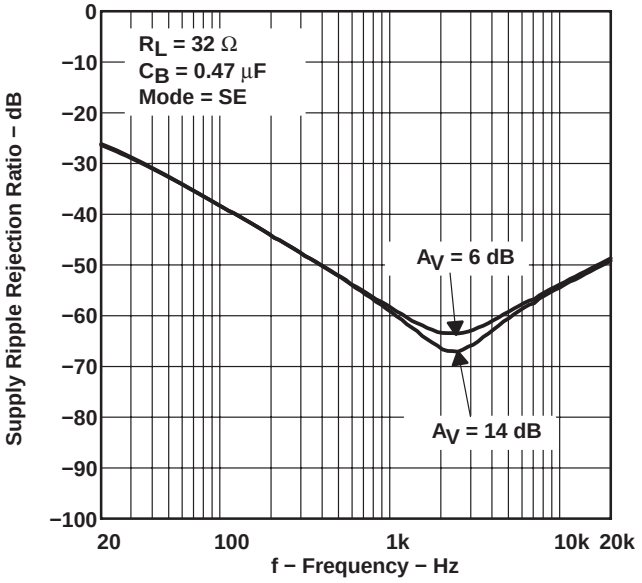


Figure 9

CROSSTALK
vs
FREQUENCY

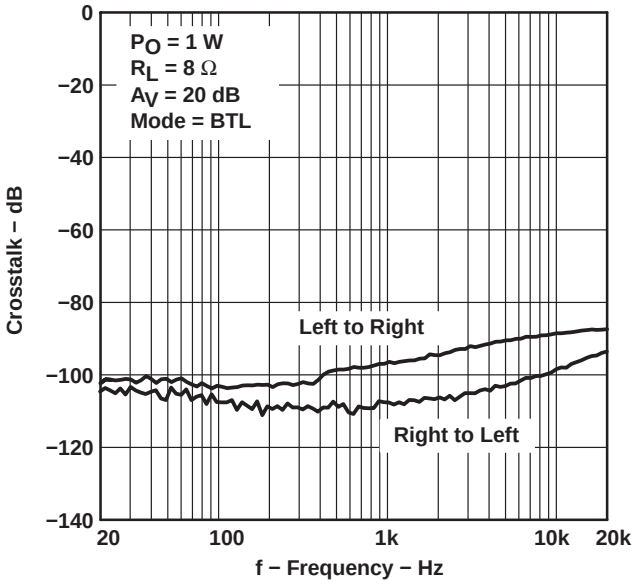


Figure 10

CROSSTALK
vs
FREQUENCY

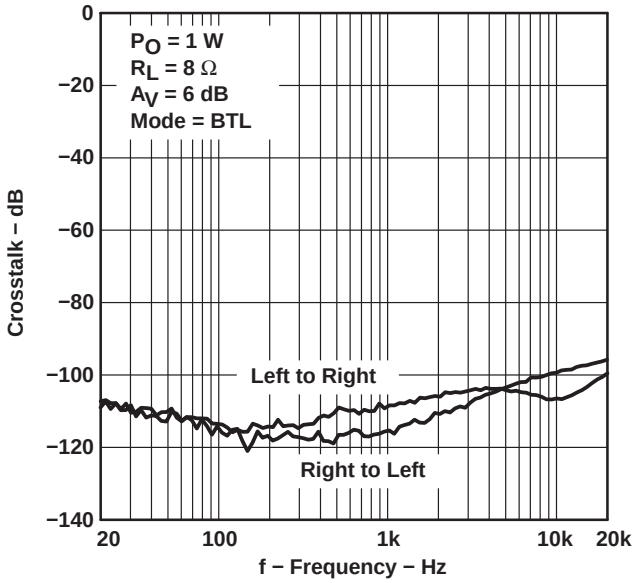


Figure 11

SHUTDOWN ATTENUATION
vs
FREQUENCY

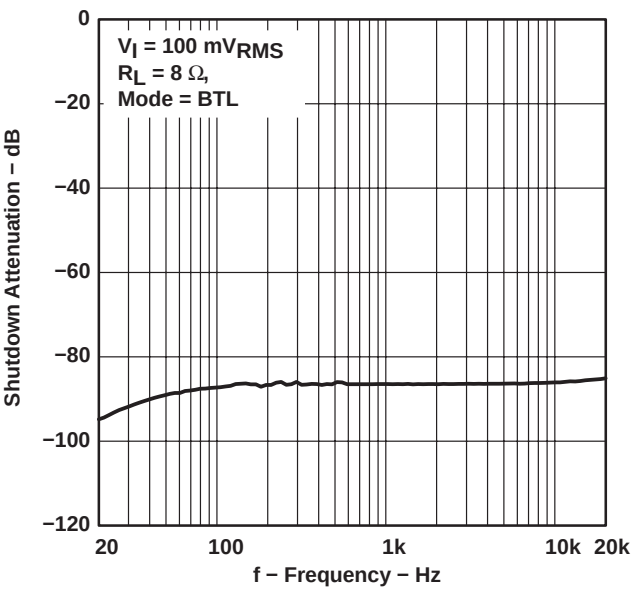


Figure 12

TYPICAL CHARACTERISTICS

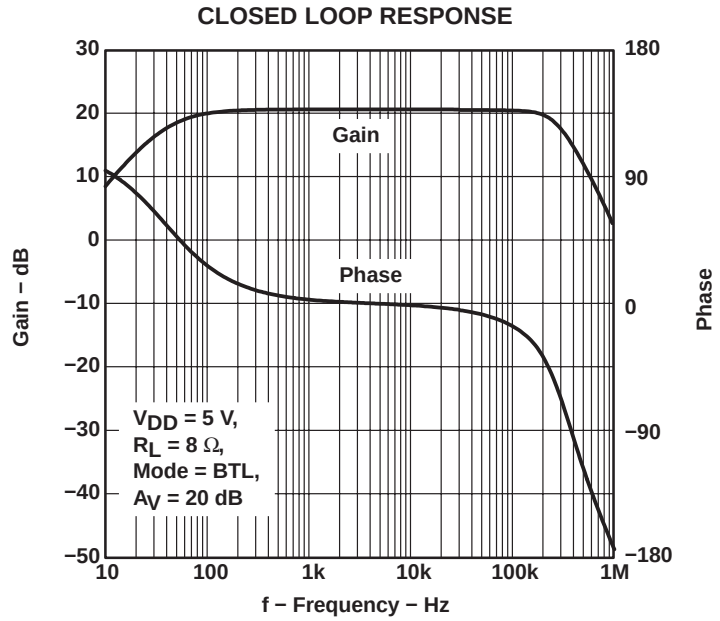


Figure 13

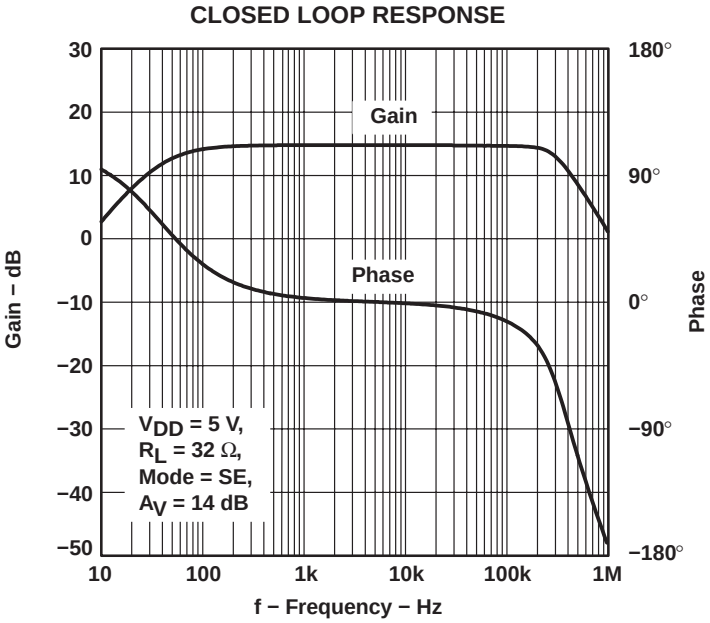


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

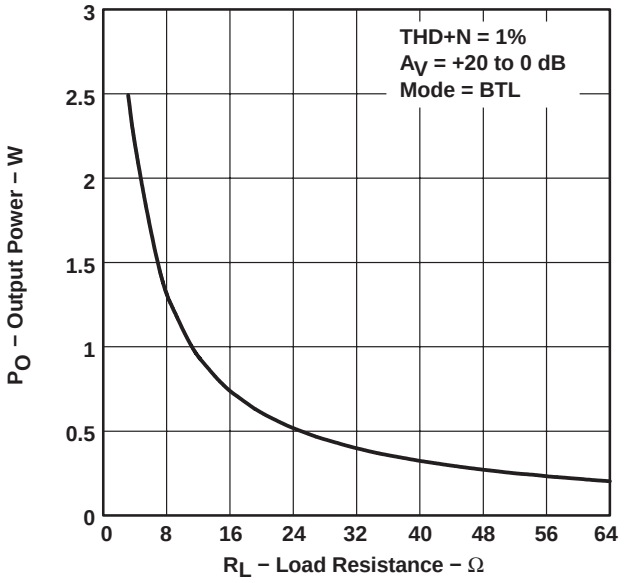


Figure 15

OUTPUT POWER
vs
LOAD RESISTANCE

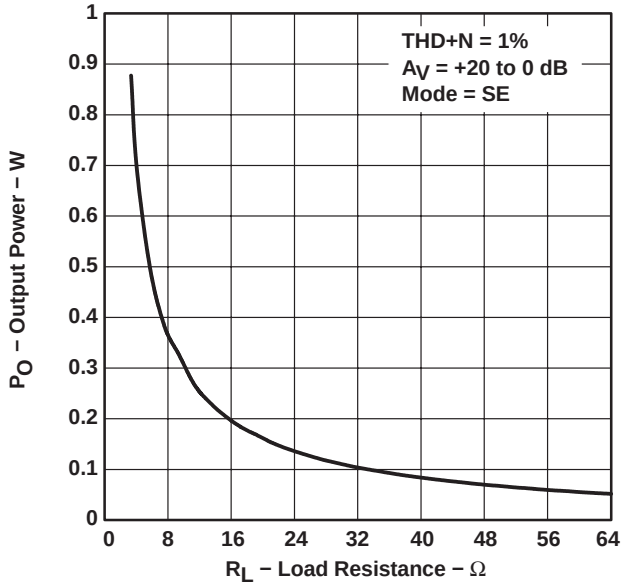


Figure 16

POWER DISSIPATION
vs
OUTPUT POWER

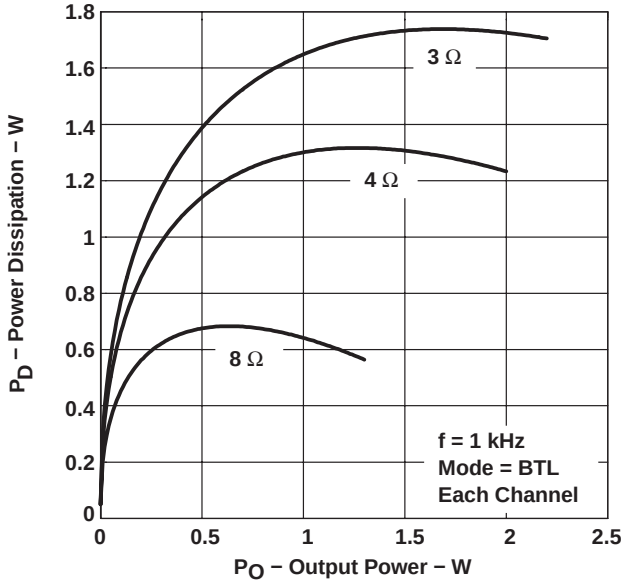


Figure 17

POWER DISSIPATION
vs
OUTPUT POWER

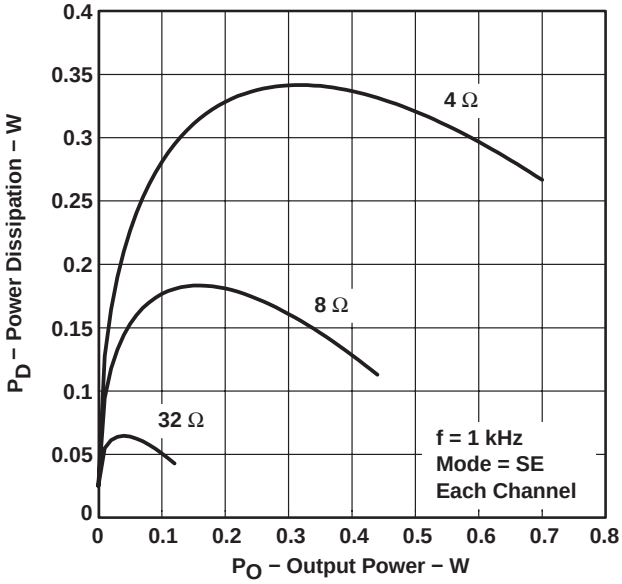


Figure 18

TYPICAL CHARACTERISTICS

**POWER DISSIPATION
vs
AMBIENT TEMPERATURE**

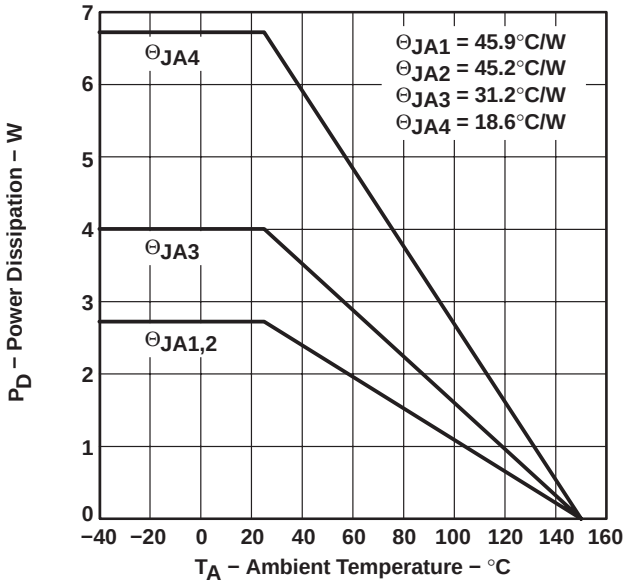
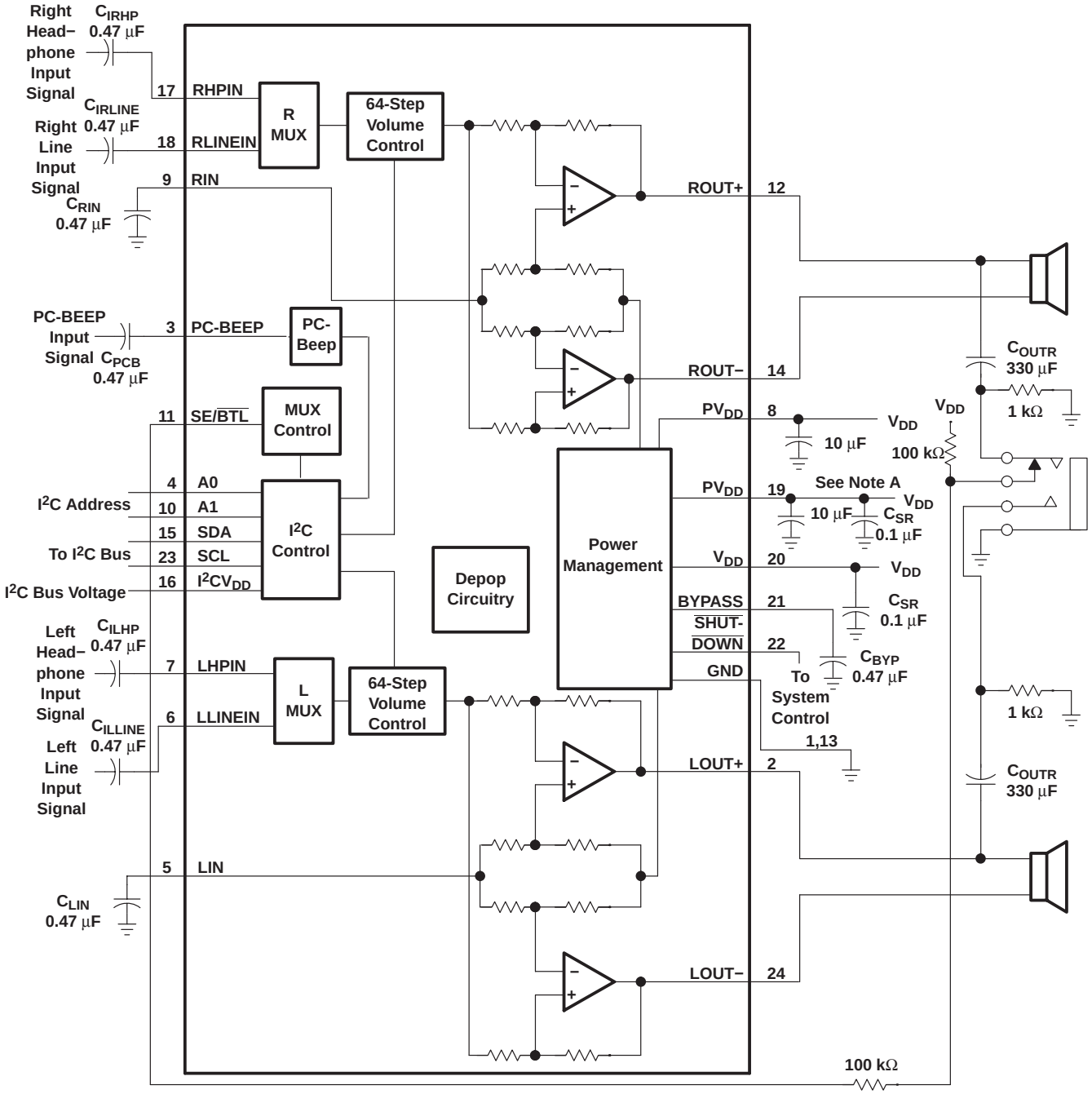


Figure 19

APPLICATION INFORMATION

selection of components

Figure 20 and Figure 21 are schematic diagrams of typical notebook computer application circuits.

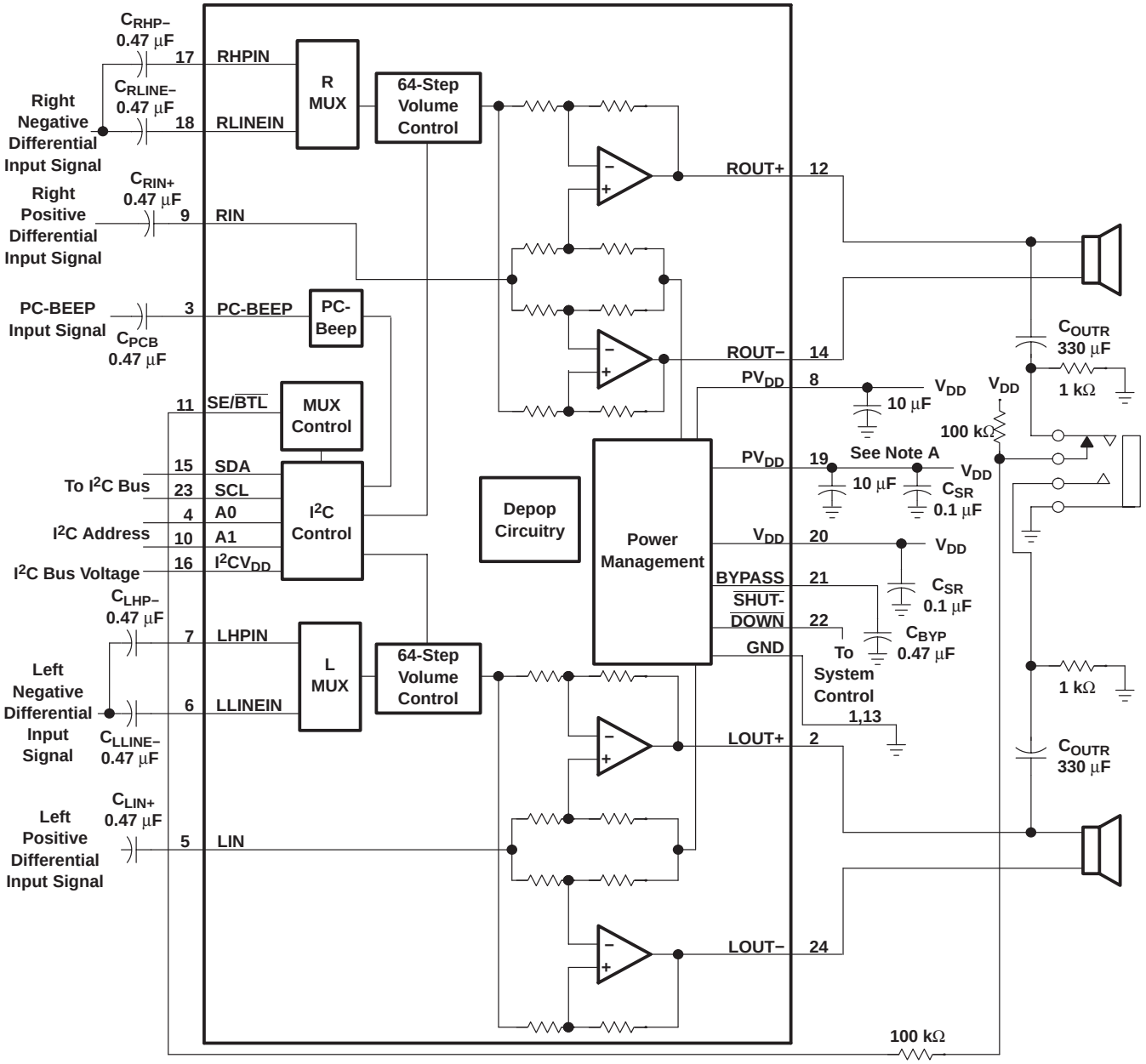


NOTE A: A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 20. Typical TPA0172 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION

selection of components (continued)



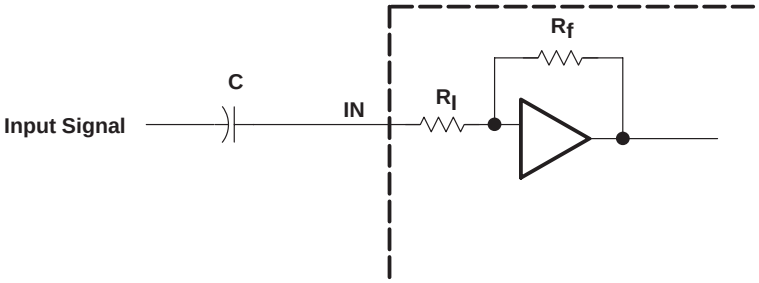
NOTE A: A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 21. Typical TPA0172 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the −3 dB or cutoff frequency will also change by over six times.



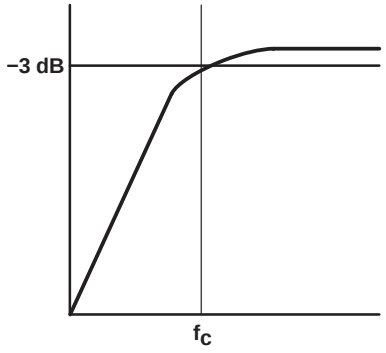
The −3-dB frequency can be calculated using equation 1.

$$f_{-3\ dB} = \frac{1}{2\pi CR_I} \quad (1)$$

input capacitor, C_I

In the typical application an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat-bass response down to 45 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

APPLICATION INFORMATION

input capacitor, C_I (continued)

In this example, C_I is 0.47 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0172 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

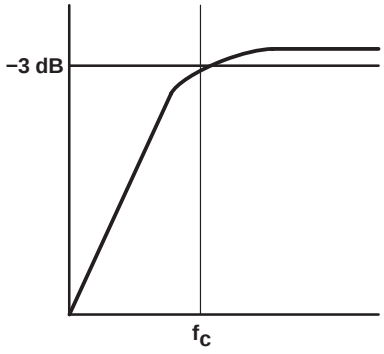
The midrail bypass capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply which is caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C_{BYP}) values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
3 Ω	330 μF	161 Hz
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
10,000 Ω	330 μF	0.05 Hz
47,000 Ω	330 μF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 22 shows a linear audio power amplifier (APA) in a bridged-tied load (BTL) configuration. The TPA0172 BTL amplifier consists of two class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

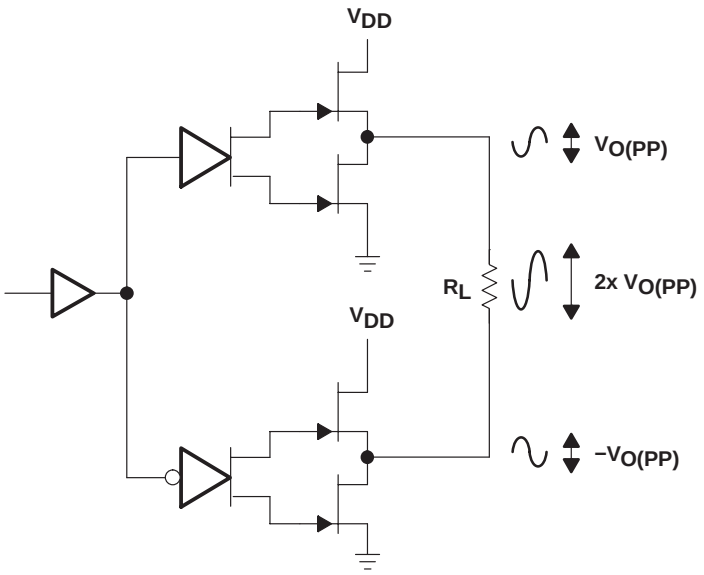


Figure 22. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 23. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated using equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

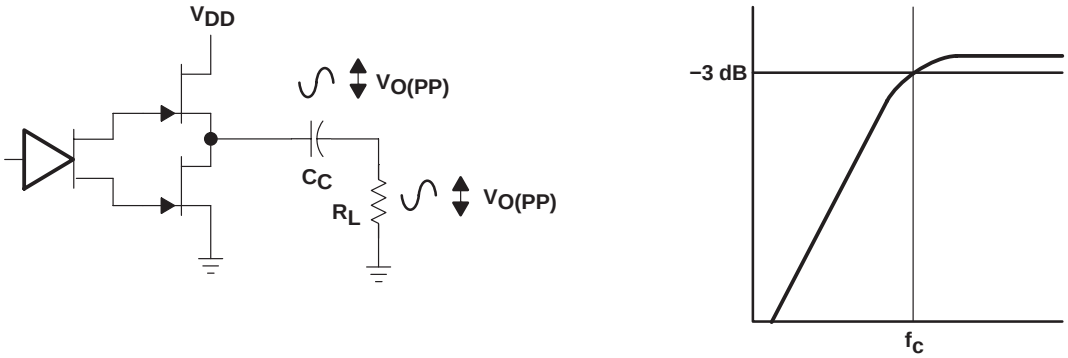


Figure 23. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

single-ended operation

In SE mode, the load is driven from the primary amplifier output for each channel (OUT+, terminals 2 and 12). The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 24).

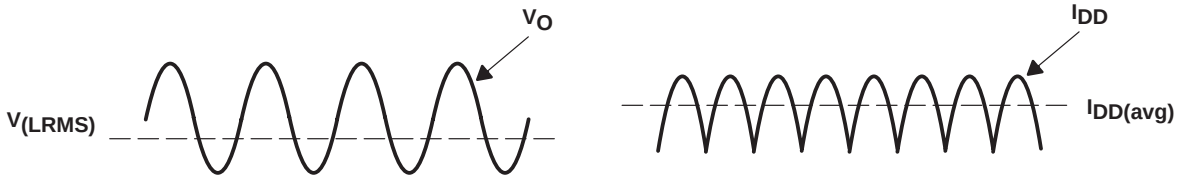


Figure 24. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L\,\text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

and $$P_{SUP} = V_{DD}\, I_{DD}\text{avg} \quad \text{and} \quad I_{DD}\text{avg} = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Therefore,

$$P_{SUP} = \frac{2 V_{DD} V_P}{\pi R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2 R_L}}{\frac{2 V_{DD} V_P}{\pi R_L}} = \frac{\pi V_P}{4 V_{DD}}$$

Where:

$$V_P = \sqrt{2 P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \quad (8)$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
I_{DD}avg = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2	0.55
0.5	44.4	2.83	0.62
1	62.8	4	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. When the TPA0172 is operating from a 5-V supply into a 3-Ω speaker, 4-W peaks are available. To convert watts to dB use equation 9.

$$P_{dB} = 10\,\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4W}{1W}\right) = 6\ \text{dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB − 15 dB = −9 dB (15-dB crest factor)
6 dB − 12 dB = −6 dB (12-dB crest factor)
6 dB − 9 dB = −3 dB (9-dB crest factor)
6 dB − 6 dB = 0 dB (6-dB crest factor)
6 dB − 3 dB = 3 dB (3-dB crest factor)

To convert dB back to watts use equation 10.

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18-dB crest factor)
= 125 mW (15-dB crest factor)
= 250 mW (12-dB crest factor)
= 500 mW (9-dB crest factor)
= 1000 mW (6-dB crest factor)
= 2000 mW (3-dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0172 and maximum ambient temperatures are shown in Table 3.

Table 3. TPA0172 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	−3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA0172 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3-dB crest factor)	0.55	100°C
2.5 W	1000 mW (4-dB crest factor)	0.62	94°C
2.5 W	500 mW (7-dB crest factor)	0.59	97°C
2.5 W	250 mW (10-dB crest factor)	0.53	102°C

The maximum dissipated power ($P_{D(max)}$) is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, use equation 11 for calculating $P_{D(max)}$ for an 8-Ω application.

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3-Ω load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. To convert this to Θ_{JA} use equation 12.

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given the maximum allowable junction temperature (Θ_{JA}) and the total internal dissipation, the maximum ambient temperature can be calculated using equation 13. The maximum recommended junction temperature for the TPA0172 is 150°C. The internal dissipation figures are taken from the power dissipation vs output power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$
$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15-dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0172 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced, the numbers in the table change significantly. Also, using 8-Ω speakers significantly increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0172 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0172, two separate amplifiers drive OUT+ and OUT−. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT− and ROUT−. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0172 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT− amplifiers are in a high output impedance state, which configures the TPA0172 as an SE driver for LOUT+ and ROUT+. I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source (see recommended operating conditions for levels) or, more typically, from a resistor divider network as shown in Figure 25.

The SE/$\overline{\text{BTL}}$ pin also selects the audio input and gain registers. When SE/$\overline{\text{BTL}}$ is held low, the RLINEIN input is selected and the BTL gain register values are used to set the gain of the input signal. When SE/$\overline{\text{BTL}}$ is held high, the RHPIN input is selected and the SE gain register values are used to set the gain. Table 5 shows the operation of the SE/$\overline{\text{BTL}}$ input pin in selecting different modes of operation.

Table 5. SE/$\overline{\text{BTL}}$ Operation

SE/$\overline{\text{BTL}}$	INPUT	GAIN REGISTER	OUTPUT
Low	Line	BTL	BTL
High	Headphone	SE	SE

The external SE/$\overline{\text{BTL}}$ pin may also be disabled and its function controlled through the I²C interface. Refer to the I²C interface section.

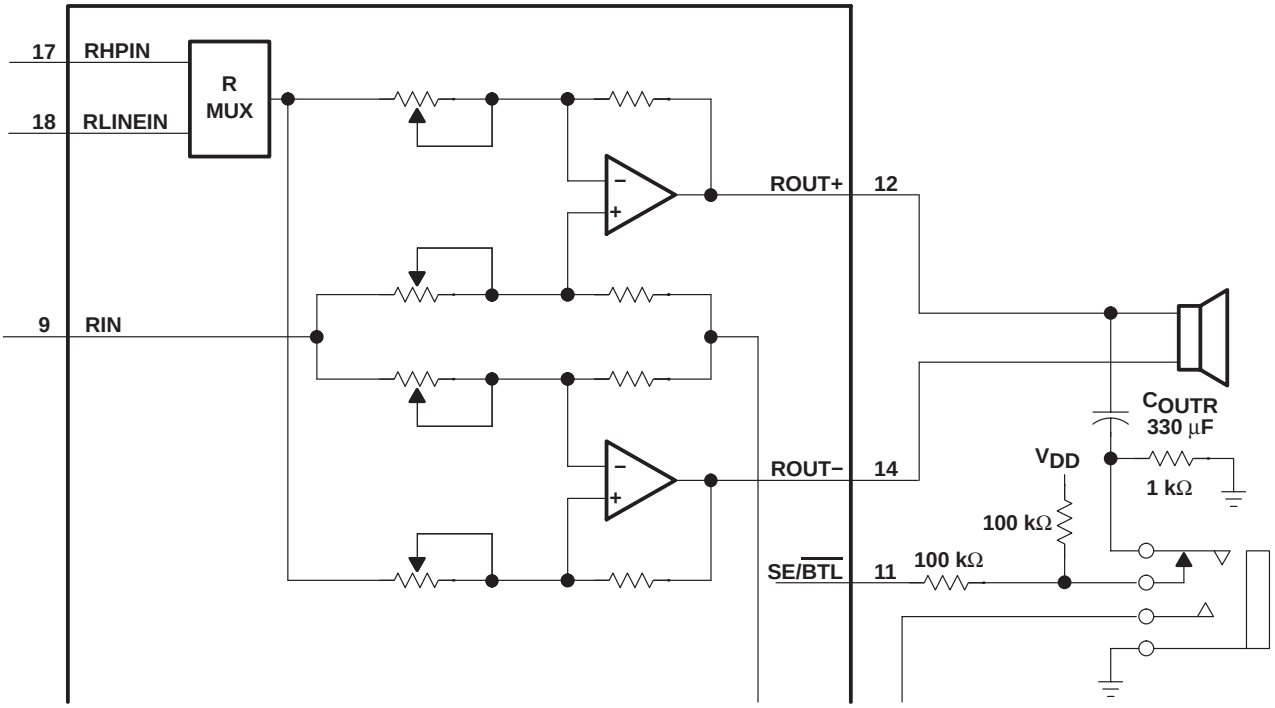


Figure 25. TPA0172 Resistor Divider Network Circuit

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation (continued)

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT− amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC-BEEP operation

The PC-BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically but may be selected manually through the I²C interface. Refer to the I²C interface section. When the PC-BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC-BEEP. The gain from the PC-BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC-BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC-BEEP will take the device out of shutdown and output the PC-BEEP signal, and then return the amplifier to shutdown mode.

In auto-detect mode, the amplifier will automatically switch to PC-BEEP mode after detecting a valid signal at the PC-BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1-V_{pp} amplitude, rise and fall times of less than 0.1 µs, and a minimum of eight rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When manually selected, the PC-BEEP input is selected, and the LINEIN and HPIN inputs are deactivated regardless of the input signal.

If it is desired to ac couple the PC-BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC-BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

shutdown modes

The TPA0172 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state (I_{DD} = 15 μA). $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

The external $\overline{\text{SHUTDOWN}}$ pin may also be disabled and its function controlled through the I2C interface. Refer to the I2C interface section.

I2C interface

The I2C interface is used to access the internal registers of the TPA0172. This two pin interface consists of one clock line (SCL) and one serial data line (SDA). The basic I2C access cycles are shown in Figure 26.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

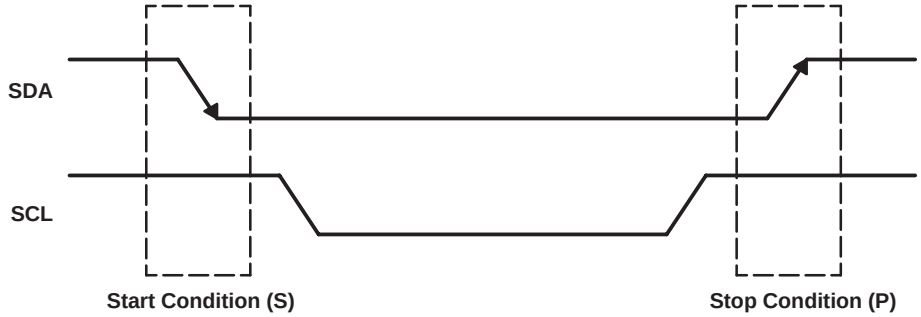


Figure 26. I2C Start and Stop Conditions

The start and stop conditions are shown in Figure 26. The high-to-low transition of SDA while SCL is high, defines the start condition. The low-to-high transition of SDA while SCL is high, defines the stop condition. Each cycle, data, or address consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains nine bits as shown in Figure 27.

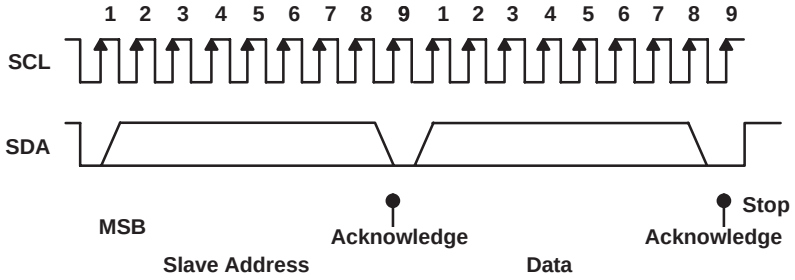


Figure 27. I2C Access Cycles

APPLICATION INFORMATION

As indicated in Figure 27, following a start condition, each I2C device decodes the slave address. The TPA0172 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle, if it decodes the address as its address.

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device will pull the SDA line low for one SCL clock cycle. A stop condition will be initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 28 and Figure 29.

During a read cycle, the slave receiver will acknowledge the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 30 and Figure 31.

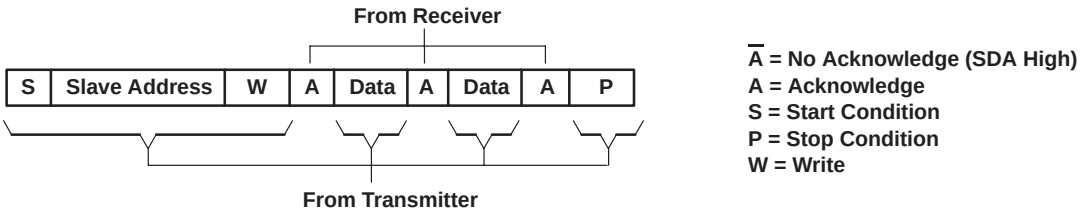


Figure 28. I2C Write Cycle

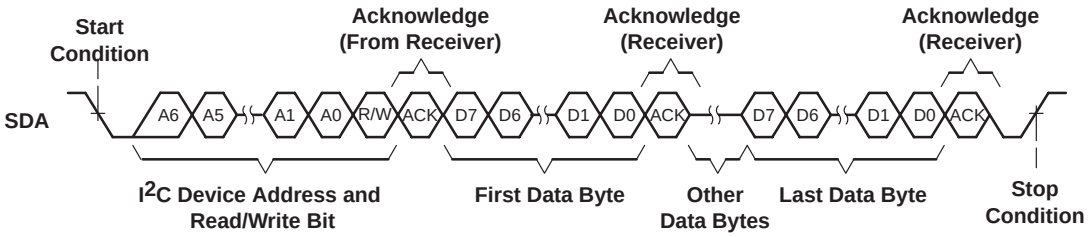


Figure 29. Multiple Byte Write Transfer

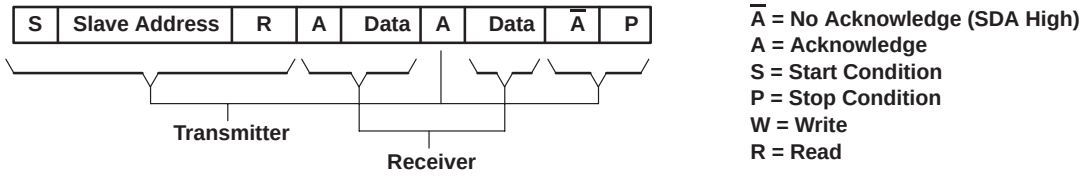


Figure 30. I2C Read Cycle

APPLICATION INFORMATION

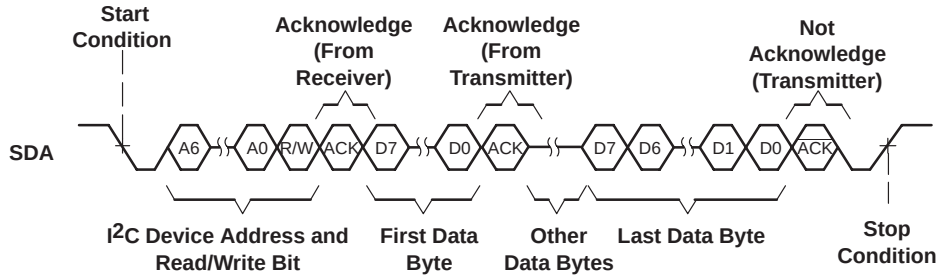


Figure 31. Multiple Byte Read Transfer

timing characteristics for I²C interface

PARAMETER		STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start condition	4.7		1.3		µs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		µs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		µs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		µs

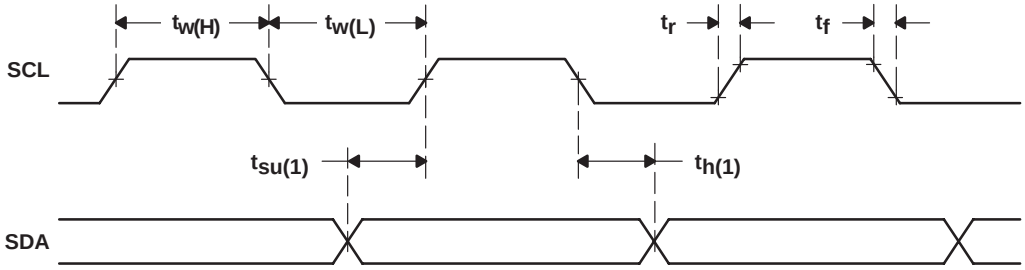


Figure 32. SCL and SDA Timing

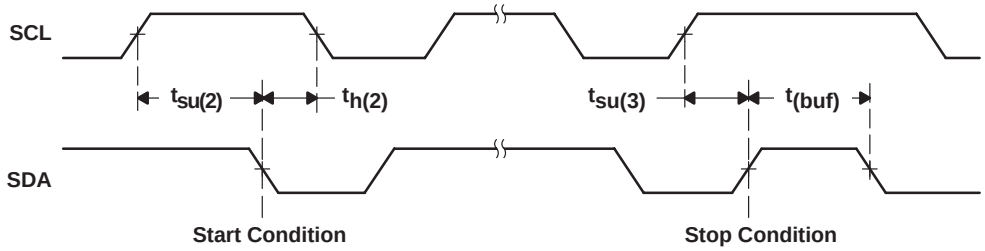


Figure 33. Start and Stop Conditions

APPLICATION INFORMATION

I2C operation specific to the TPA0172 device

The TPA0172 operates using only a multiple byte transfer protocol as shown in Figures 29 and 31. The six internal registers and the functionality of each can be found in Table 6. When writing to the device, all 6 bytes corresponding to all six registers must be sent to the device in a single multiple byte transfer. During a read cycle, the TPA0172 will send 6 bytes in a single transfer to the master device requesting the information.

Table 6. Internal Registers

REGISTER NAME	POWER-UP/RESET VALUE ($b_7b_6b_5...b_0$)	BIT ASSIGNMENT
Right Gain Register 1 (BTL Gain Register)	0011 1111	0−5: Gain level 6: Mute 7: Mute
Left Gain Register 1 (BTL Gain Register)	0011 1111	0−5: Gain level 6: Mute 7: Mute
Right Gain Register 2 (SE Gain Register)	0011 1111	0−5: Gain level 6: Mute 7: Mute
Left Gain Register 2 (SE Gain Register)	0011 1111	0−5: Gain level 6: Mute 7: Mute
Mask Register	1111 1111	0: Disable internal SHUTDOWN control 1: Disable internal SE/BTL control 2: Disable internal PC-BEEP control 3−6: Unused 7: Powering-up indicator (read-only)
Control Register	0000 0000	0: SHUTDOWN 1: HP/LINE 2: Reserved 3: Mute 4: Reserved 5: SE/BTL 6: Gain register select 7: PC-BEEP

APPLICATION INFORMATION

slave address

The slave address for the TPA0172 consists of 7 bits of address information along with 1 bit, the LSB, reserved for read/write information. There are eight possible addresses (including the read/write bit) for this device that can be selected with the external A1 and A0 address pins. The most significant 5 bits of the address are fixed. Table 7 lists the possible addresses for the TPA0172.

Table 7. Valid Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2 (A1)	BIT 1 (A0)	BIT 0 (R/W)
1	1	0	1	1	0	0	0
1	1	0	1	1	0	0	1
1	1	0	1	1	0	1	0
1	1	0	1	1	0	1	1
1	1	0	1	1	1	0	0
1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0
1	1	0	1	1	1	1	1

gain register operation

The gain of the TPA0172 ranges from 20 dB to −60 dB in 64 1.25-dB steps. At power-up, both the right and left channels are set at −60 dB. The truth table shown in Table 8 gives examples of valid values that may be read from or written to the four gain setting registers. Note that the amplifier is muted if either bit 7 or bit 6 is set. Furthermore, to avoid any unwanted clicks or pops, the gain settings should not be changed until the amplifier has completed the power-up sequence, which can be determined by monitoring bit 7 of the mask register. When the bit goes to 0, the power-up sequence is complete.

Table 8. Gain Settings Truth Table

GAIN (dB)	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
20	0	0	0	0	0	0	0	0
18.75	0	0	0	0	0	0	0	1
17.5	0	0	0	0	0	0	1	0
16.25	0	0	0	0	0	0	1	1
…	…	…	…	…	…	…	…	…
−57.5	0	0	1	1	1	1	0	1
−58.75	0	0	1	1	1	1	1	0
−60	0	0	1	1	1	1	1	1
−85 (mute)	1	1	X	X	X	X	X	X

APPLICATION INFORMATION

mask register operation

The mask register allows the user to select whether SHUTDOWN, SE/$\overline{\text{BTL}}$, and PC-BEEP are to be controlled by the external pins or by the internal control register. Since PC-BEEP does not have an external control pin available, writing a 1 to this bit will disable all internal register control and place the PC-BEEP input in auto-detect mode. When a bit is set, the corresponding internal control register bit is masked or ignored and the external pin controls the operating mode. Conversely, when a bit is set to 0, the corresponding external pin is disabled and the internal control register bit determines the operating mode. For example, writing XXXXX010 to the register allows the control register to control the operation of the PC-BEEP input and SHUTDOWN, while allowing the external pin to control SE/$\overline{\text{BTL}}$.

The MSB of the mask register is read-only. It is set when the TPA0172 is executing its power-up sequence and is set to 0 upon completion of the sequence and during normal operation. To avoid any unwanted clicks or pops, the gain registers should not be changed while this bit is set.

control register operation

Each bit of the control register allows the user to control the operating mode of the TPA0172, as shown in Table 9.

Table 9. Control Register Bit Assignments

BIT	FUNCTION	VALUE	RESULT
0	SHUTDOWN	0 1	Normal operation Shutdown mode
1	HP/$\overline{\text{LINE}}$	0 1	Line inputs selected Headphone inputs selected
2	Reserved	0	
3	Mute	0 1	Normal operation Mute mode
4	Reserved	1	
5	SE/$\overline{\text{BTL}}$	0 1	BTL mode SE mode
6	Gain register select	0 1	Use BTL gain registers Use SE gain registers
7	PC-BEEP enable	0 1	Auto-detect PC-BEEP PC-BEEP always on

Bit 0 operates in the same manner as the external $\overline{\text{SHUTDOWN}}$ pin, but the logic is active high in the internal register.

Bit 1 allows the user to select the input source. If bit 1 of the mask register is set, however, the HP/LINE function is tied to the external SE/$\overline{\text{BTL}}$ pin.

Bit 2 should always be set to 0. Reserved for future functionality.

Bit 3 performs the same mute function as setting either bit 6 or 7 in the gain registers.

Bit 4 should always be set to 1. Reserved for future functionality.

Bit 5 operates in the same manner as the external SE/$\overline{\text{BTL}}$ pin.

Bit 6 allows the user to select which gain registers will determine the gain settings for each channel. For example, the amplifier may be configured to operate in SE mode, but with the gain settings taken from the BTL registers. This function is tied to the SE/$\overline{\text{BTL}}$ pin if bit 1 of the mask register is set, which results in the SE gain registers controlling the gain in SE mode, and the BTL registers controlling the gain in BTL mode.

Bit 7 allows the user to either auto-detect a signal at the PC-BEEP input or manually override that input to always be on.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA0172PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0172	Samples
TPA0172PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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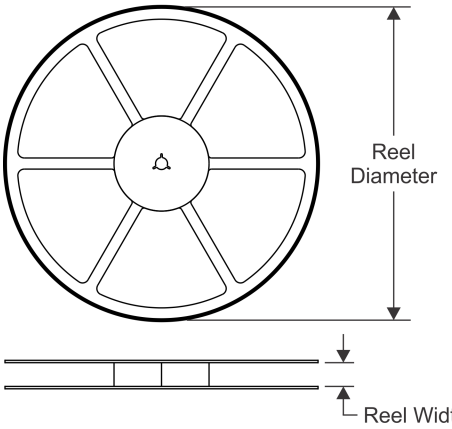
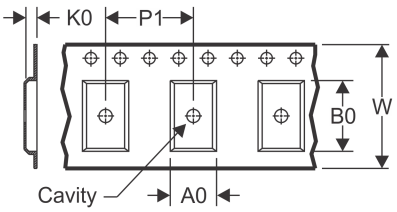
TAPE AND REEL INFORMATION

REEL DIMENSIONS

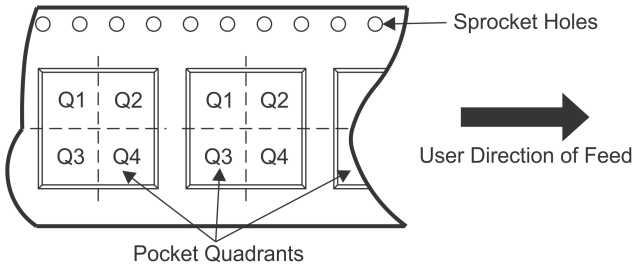


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

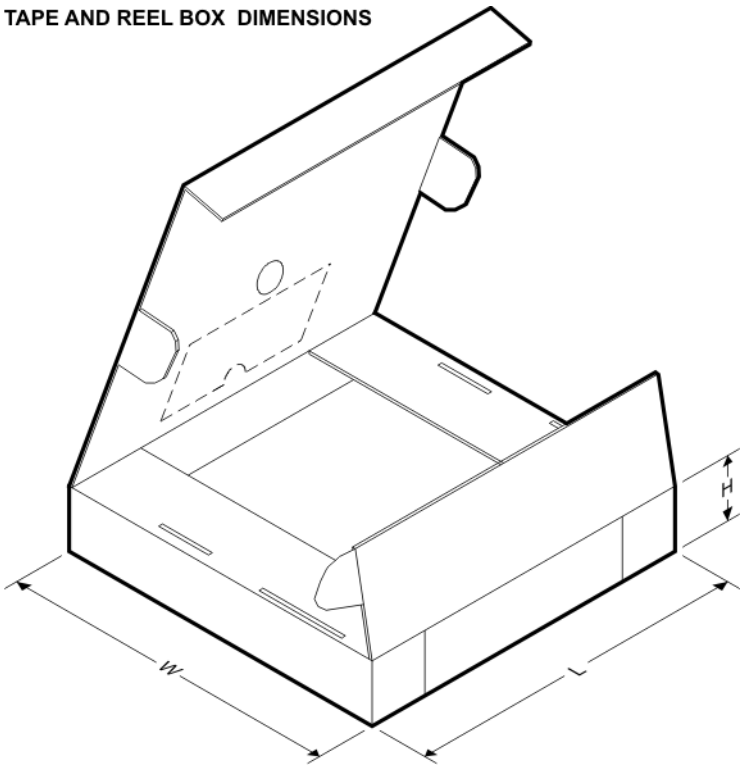
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0172PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0172PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

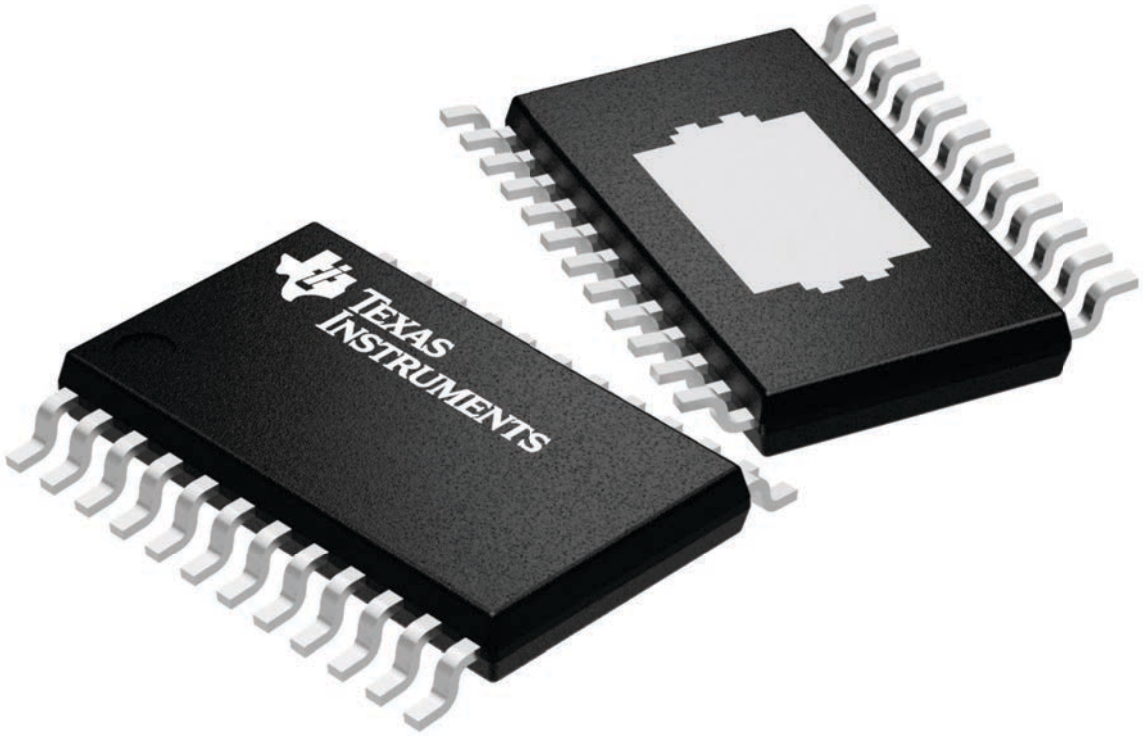
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



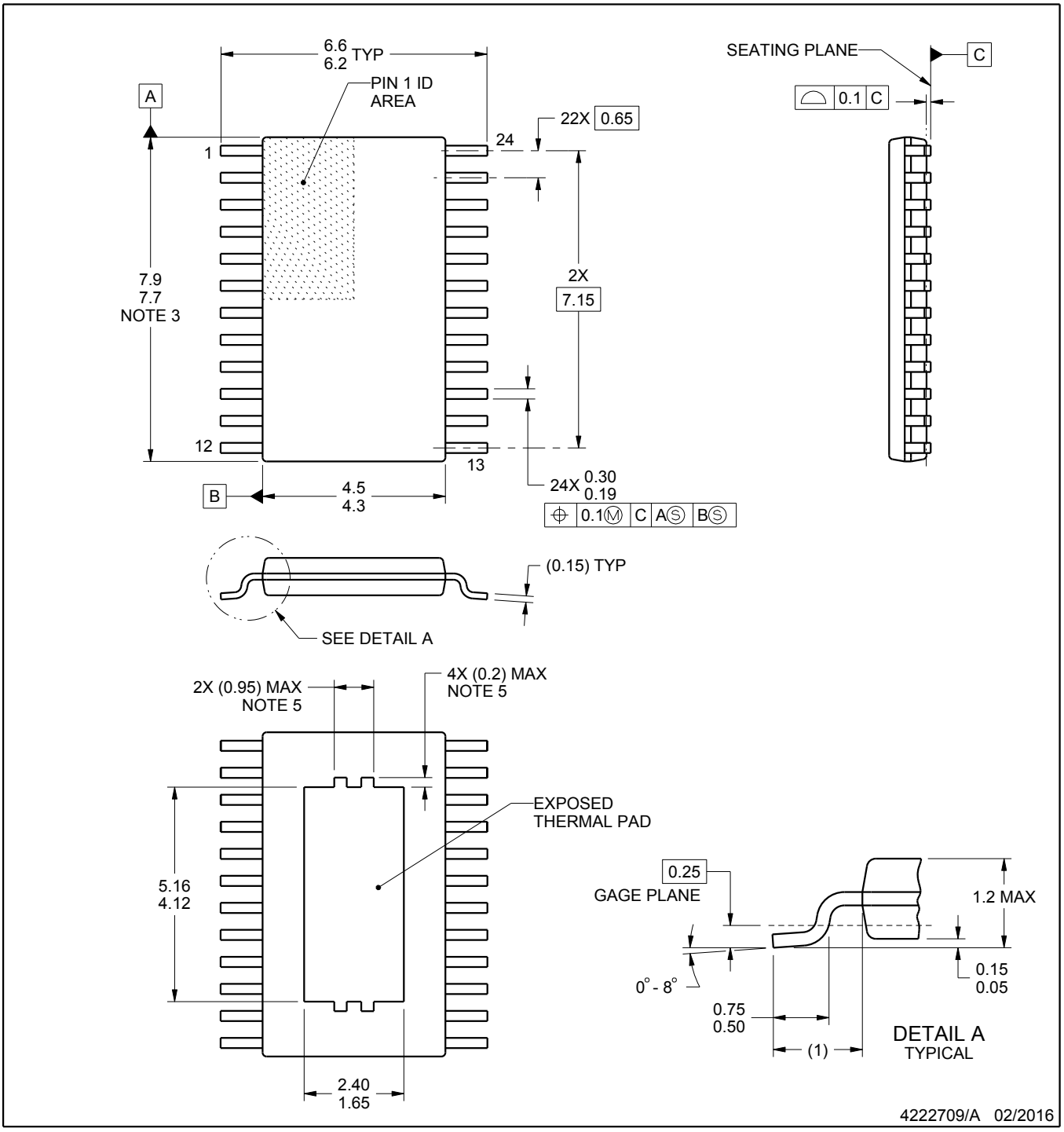
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

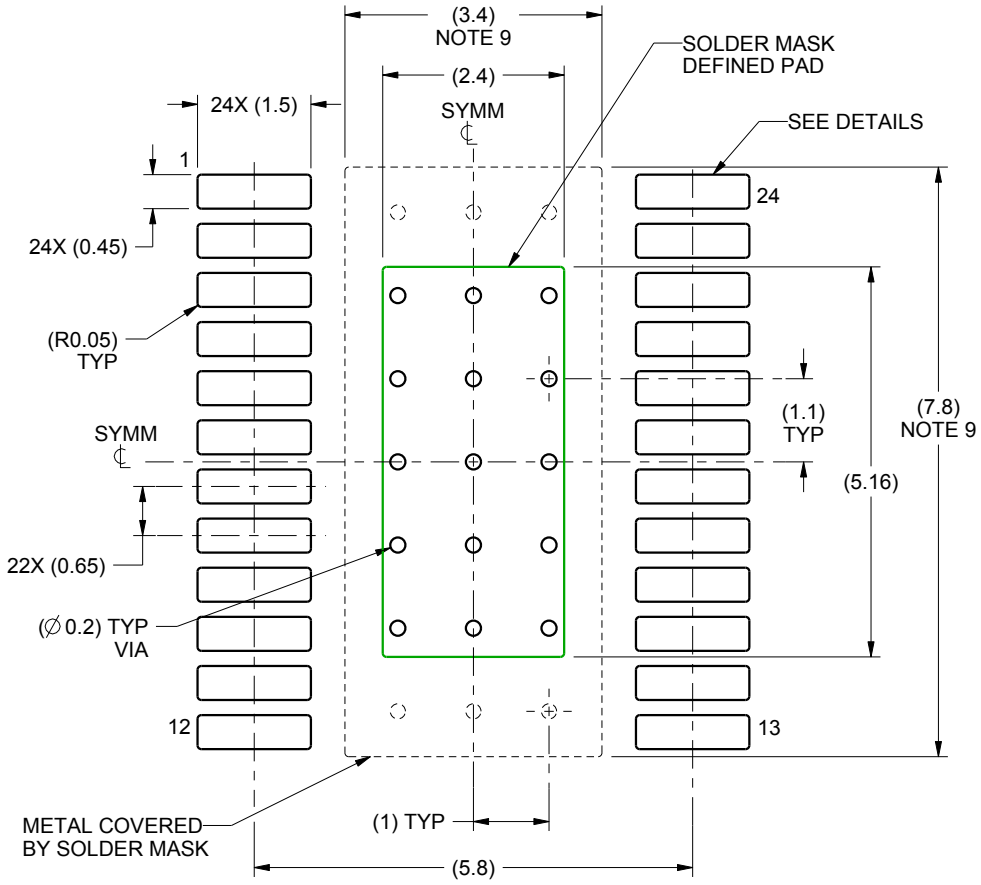
PLASTIC SMALL OUTLINE



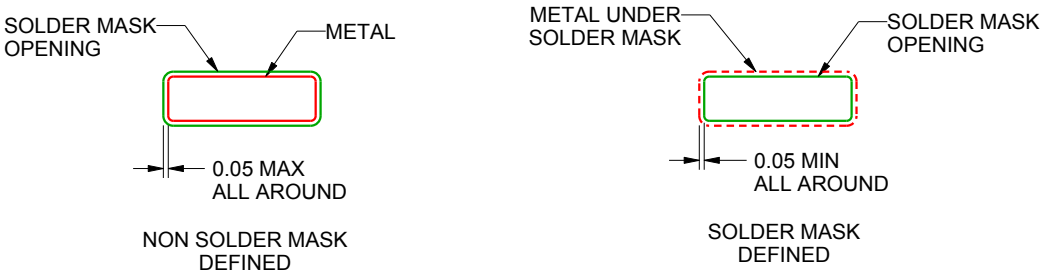
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

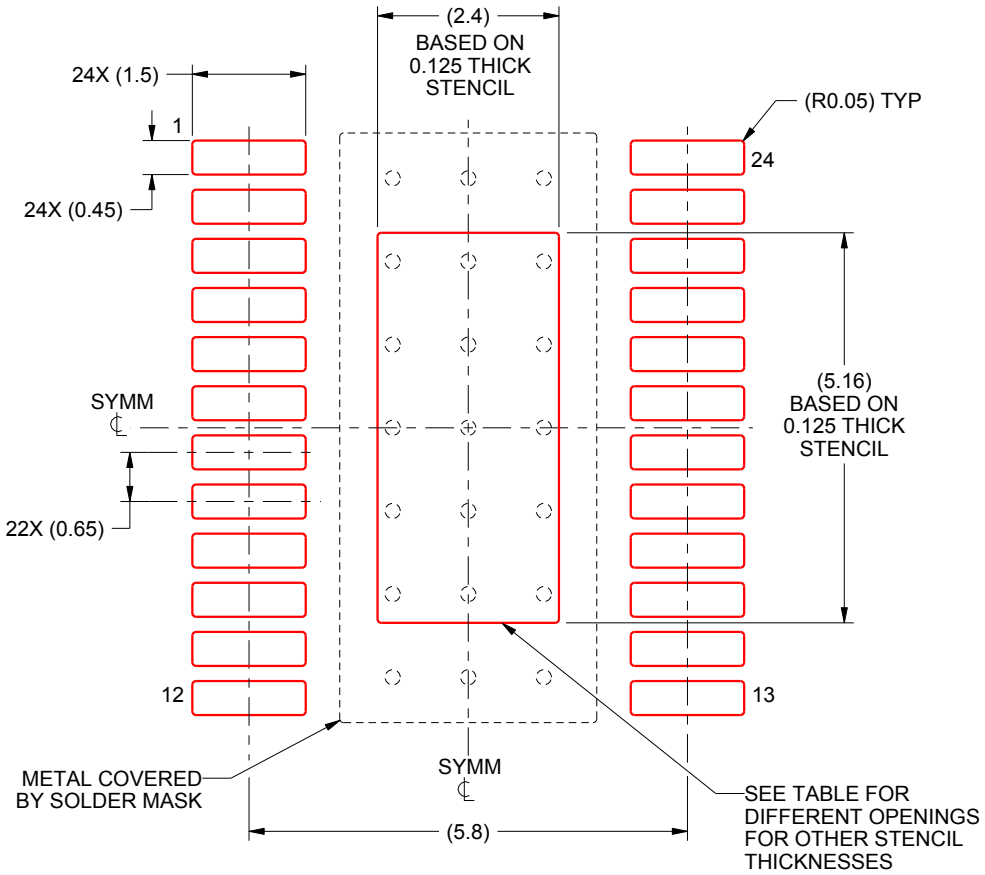


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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