FEATURES

- Dual output (2+1) Digital Controller with proprietary control algorithm
- Two-phase operation available on Output #1 for powering very high current ASICs and DSPs
- I2C /PMBus interface for configuration & telemetry with pin programmable address
- Operating ambient temperature: -40°C to 85°C
- 3.3V bias operation
- Independent loop switching frequencies from 200kHz to 2MHz per phase
- IR Efficiency Shaping with Dynamic Phase Control (DPC)
- Active Diode Emulation modes for light load efficiency
- IR Adaptive Transient Algorithm (ATA) minimizes output bulk capacitors and system cost
- Independent OVP, UVP, OCP for each output
- Thermal Protection (OTP) and VRHOT# flag
- Multiple time programmable (MTP) memory for custom configuration
- Flexible I2C bus security features
- Pb-Free, RoHS, 32-pin 5mm X 5mm QFN package

DESCRIPTION

The IR36021 is a dual-loop digital multi-phase buck controller designed for point of load applications.

The IR36021 include Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. Dynamic Phase Control adds/drops active phases based upon load current and can be configured to enter 1-phase operation and diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors and Multiple Time Programmable (MTP) storage saves pins and enables a small package size. Device configuration and fault parameters are easily defined using the IR Intuitive Power Designer (IPD) GUI and stored in on-chip MTP.

The IR36021 provides extensive OVP, UVP, OCP and OTP fault protection and includes thermistor based temperature sensing with VRHOT signal.

The IR36021 includes numerous features like register diagnostics for fast design cycles and platform differentiation, truly simplifying VRD design and enabling fastest time-to-market (TTM) with "set-and-forget" methodology.

APPLICATIONS

- Embedded Telecom Systems
- Netcom Applications
- Server Application
- Distributed Point of Load Power Architectures

BASIC APPLICATION

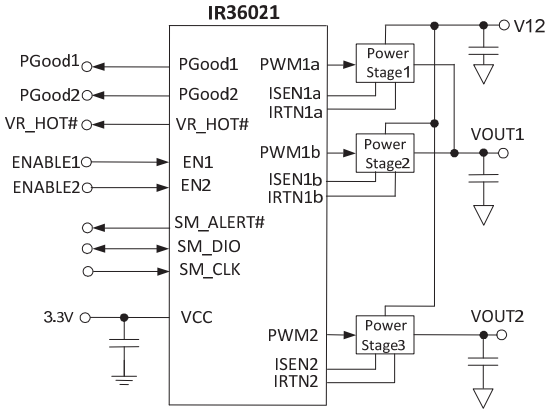


Figure 1: IR36021 Basic Application Circuit

PIN DIAGRAM

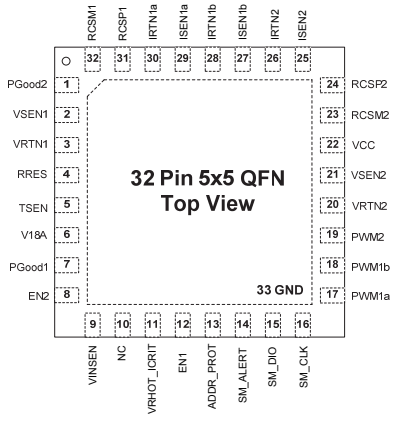


Figure 2: IR36021 Package Top View

PIN DIAGRAM

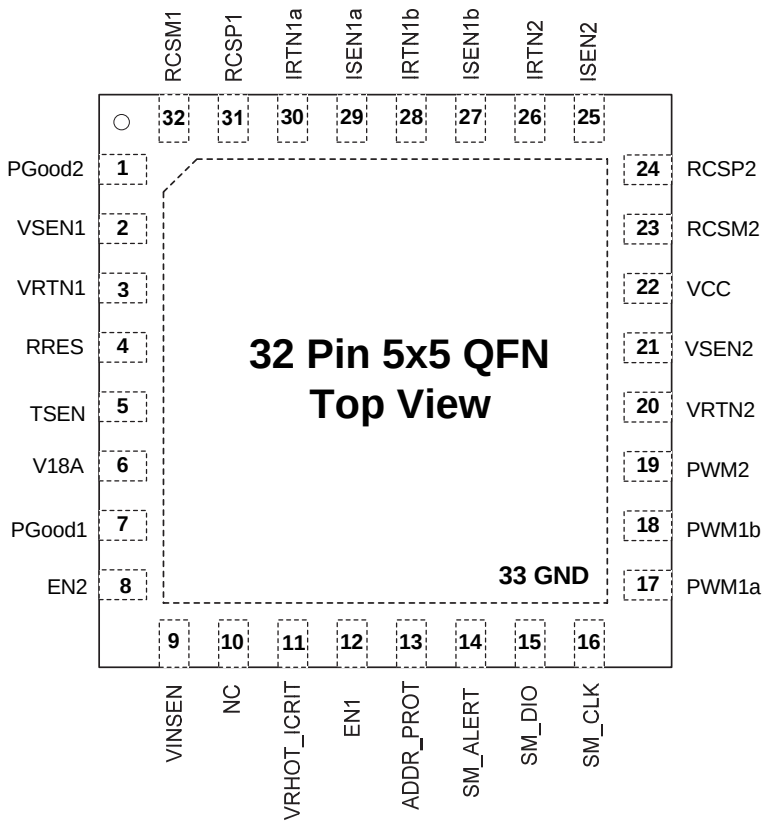


Figure 3: IR36021 Package Bottom View
5mm X 5mm QFN

ORDERING INFORMATION

Package	Tape and Reel Qty	Part Number
M	3000	**IR36021MTRPbF**

FUNCTIONAL BLOCK DIAGRAM

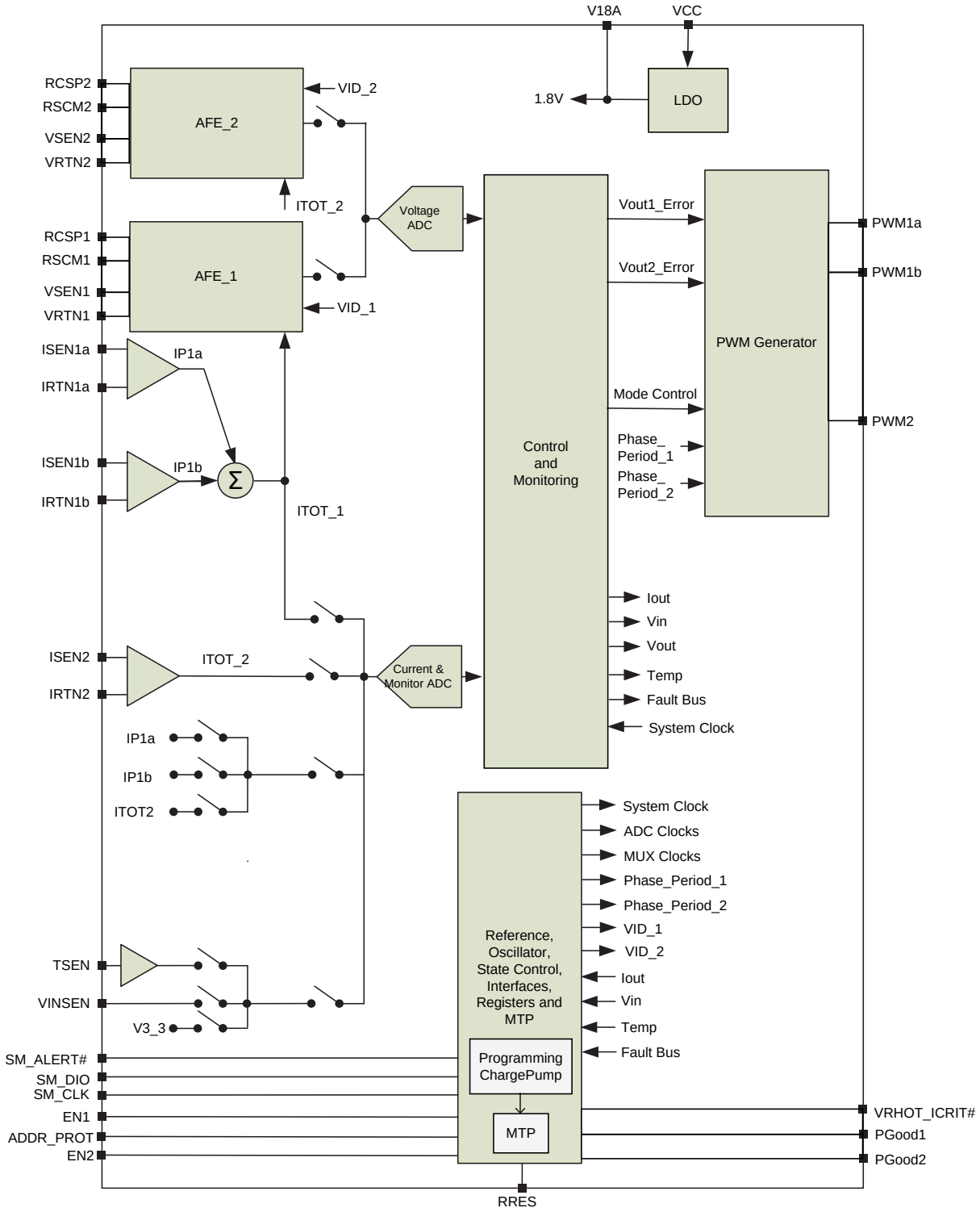


Figure 4: IR36021 Simplified Block Diagram

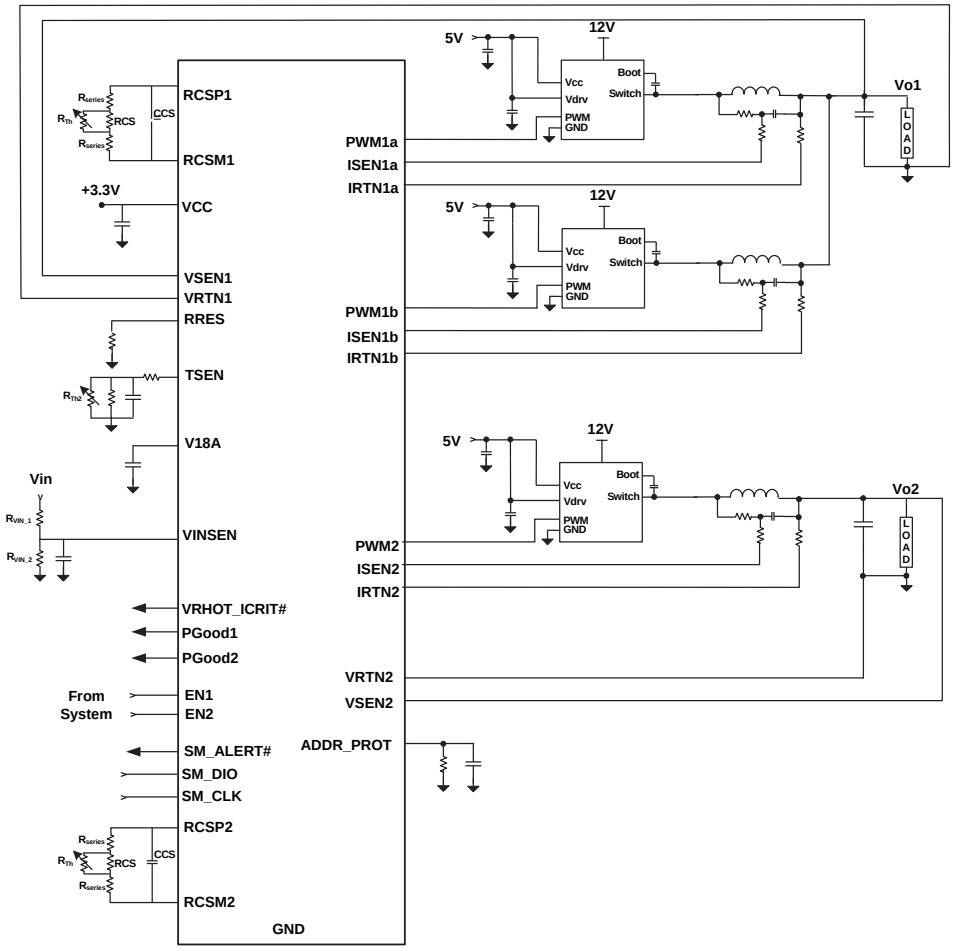


Figure 5: Dual-loop VR using IR36021 Controller and IR PowerStage in 2+1 Configuration

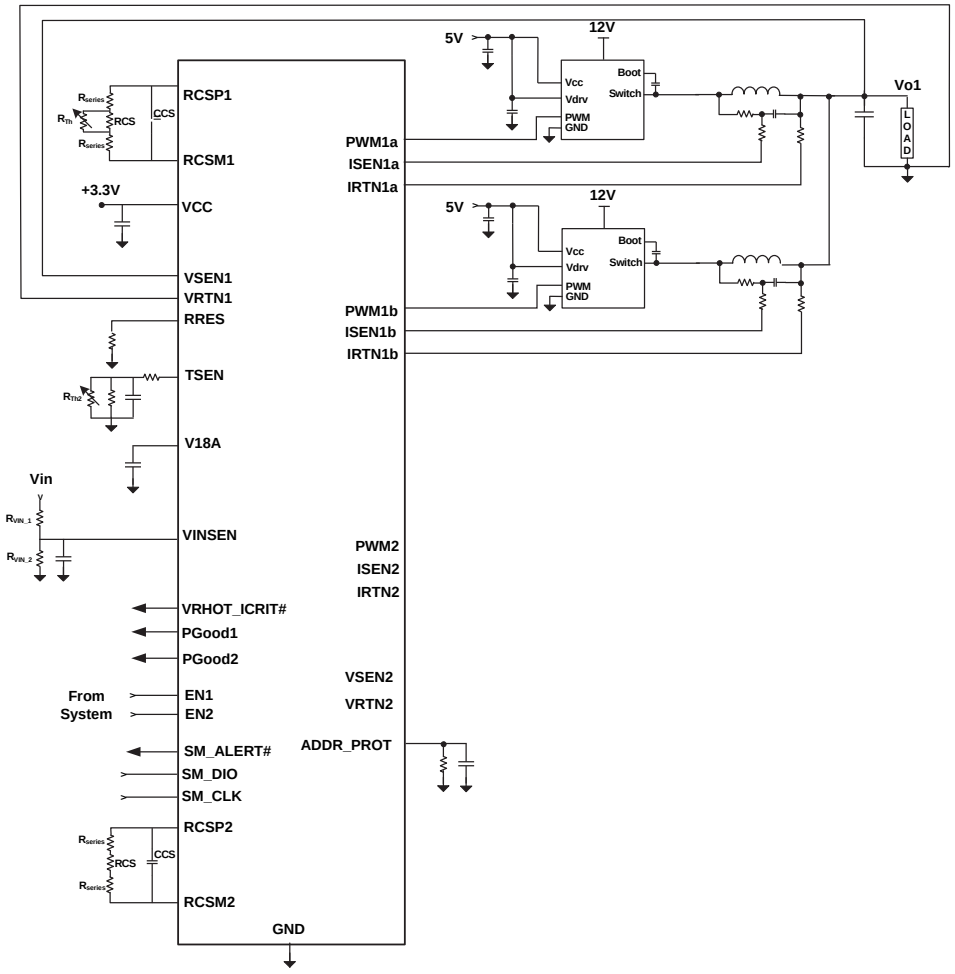


Figure 6: Dual-loop VR using IR36021 Controller and IR PowerStage in 2+0 Configuration

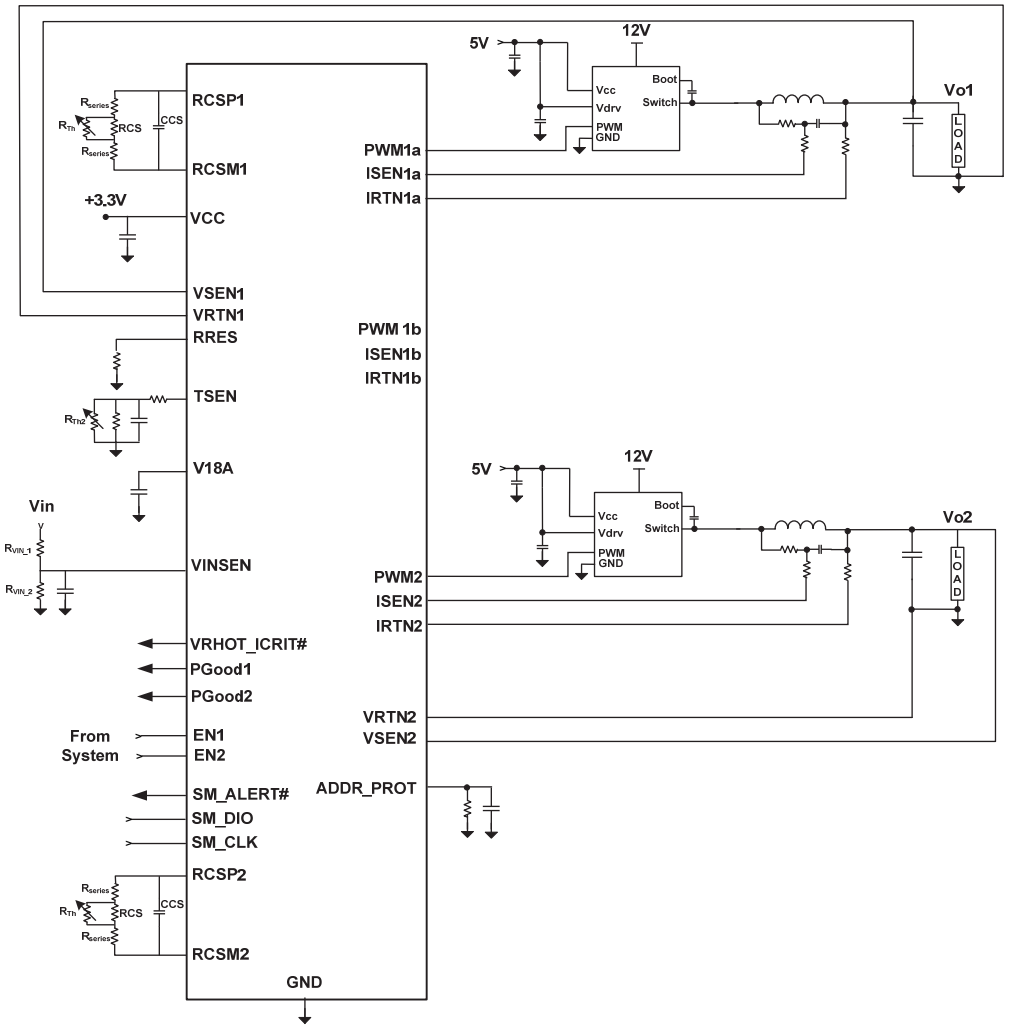


Figure 7: Dual-loop VR using IR36021 Controller and IR PowerStage in 1+1 Configuration

PIN DESCRIPTION

PIN #	PIN NAME	PIN DESCRIPTION
1	PGood2	**Voltage Regulator Ready Output (Loop #2).** Open-drain output that asserts high when the VR has completed soft-start to Loop #2 boot voltage.
2	VSEN1	**Voltage Sense Input Loop#1**. This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN
3	VRTN1	**Voltage Sense Return Input Loop#1.** This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN.
4	RRES	**Current Reference Resistor.** A 1% resistor is connected to this pin to set an internal precision current reference
5	TSEN	**NTC Temperature Sense Input.** An NTC network is connected to this pin to measure temperature.
6	V18A	**1.8V Decoupling.** Two capacitors on this pin provide decoupling for the internal 1.8V supply
7	PGood1	**Voltage Regulator Ready Output (Loop #1).** Open-drain output that asserts high when the VR has completed soft-start to Loop #1 boot voltage.
8	EN2	**VR Enable Input.** ENABLE is an active high system input to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts PGOOD2 and shuts down the regulator.
9	VINSEN	**VIN Voltage Sense Input.** This is used to detect a valid 5V-12V supply voltage and measure the input voltage to the VR.
10	NC	
11	VRHOT-ICRIT	**VRHOT_ICRIT# Output.** Active low alert pin that can be programmed to assert if temperature or average load current exceeds user-definable thresholds.
12	EN1	**VR Enable Input.** ENABLE is an active high system input to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts PGOOD1 and shuts down the regulator.
13	ADDR_PROT	**Bus Address & I2C Bus Protection** A resistor to ground on this pin defines the I2C address which is latched when VCC becomes valid. Subsequently, this pin becomes a logic input to enable or disable communication on the I2C bus,
14	SM_ALERT	SMBus Alert line
15	SM_DIO	**Serial Data Line I/O.** I2C bus bi-directional serial data line.
16	SM_CLK	**Serial Clock Line Input.** I2C bus clock input.
17	PWM1a	**Loop 1 Phase 1 Pulse Width Modulation Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Refer to the TBD section for unused/disabled phases.
18	PWM1b	**Loop 1 Phase 2 Pulse Width Modulation Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Refer to the TBD section for unused/disabled phases.
19	PWM2	**Loop 2 Pulse Width Modulation Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Refer to the TBD section for unused/disabled phases.
20	VRTN2	**Voltage Sense Return Input Loop#2.** This pin is connected directly to Loop#2 ground at the load and should be routed differentially with VSEN.
21	VSEN2	**Voltage Sense Input Loop#1**. This pin is connected directly to the VR output voltage of Loop #2 at the load and should be routed differentially with VRTN
22	VCC	**Input supply voltage.** 3.3V supply to power the device
23	RCSM2	**Resistor Current Sense Minus Loop 2**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #2.

PIN #	PIN NAME	PIN DESCRIPTION
24	RCSP2	**Resistor Current Sense Positive Loop 2**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #2.
25	ISEN2	**Loop 2 Current Sense Input.** Loop 2 sensed current input (+)
26	IRTN2	**Loop 2 Current Sense Return Input.** Loop 2 sensed current input return (-)
27	ISEN1b	**Loop1 Phase 2 Current Sense Input.** Phase 2 sensed current input (+)
28	IRTN1b	**Loop 1 Phase 2 Current Sense Return Input.** Phase 2 sensed current input return (-)
29	ISEN1a	**Loop1 Phase 1 Current Sense Input.** Phase 1 sensed current input (+)
30	IRTN1a	**Loop1 Phase 1 Current Sense Return Input.** Phase 1 sensed current input return (-)
31	RCSP1	**Resistor Current Sense Positive Loop#1**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #1
32	RCSM1	**Resistor Current Sense Minus Loop#1**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #1
33	GND	**Ground.** Ground reference for the IC. The large metal pad on the bottom must be connected to Ground.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC)	GND-0.3V to 4.0V
RCSPx, RCSMx	0 to 2.2 V
VSENx, VRTNx, ISENx, IRTNx	GND-0.2V to 2.7V
RRES, V18A, TSEN, VINSEN	GND-0.2V to 2.2V
PWMx	GND-0.3V to VCC
PGoodx, ENx, ADDR_PROT, VRHOT_ICRIT#	GND-0.3V to VCC
SM_DIO, SM_CLK, SM_ALERT	GND-0.3V to 5.5V
ESD Rating	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Moisture Sensitivity Level	JEDEC Level 2@260°C

THERMAL INFORMATION

Thermal Resistance (θ_{JA} & θ_{JC})*	29°C/W & 3°C/W
Maximum Operating Junction Temperature	-40°C to +125°C
Maximum Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

* θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. These devices are ESD sensitive, observe handling precautions to prevent electrostatic discharge damage.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
VCC	Supply Voltage	2.9	3.63	V
T_A	Ambient Temperature	0	85	°C

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply	**VCC/GND**					
Supply voltage	V_{cc}		2.9	3.3	3.63	V
Supply current	I_{vcc}	PWM not switching	95	105	125	mA
3.3V UVLO turn on threshold				2.80	2.9	V
3.3V UVLO turn off threshold			2.6	2.7		V
Input voltage sense input						
Input impedance			1			MΩ
Input range	V12	With 14:1 divider	0	0.857	1.1	V
UVLO turn on programmable range[1]		With 14:1 divider		4.5-15.9375		V
UVLO turn off programmable range[1]		With 14:1 divider		4.5-15.9375		V
OVP threshold (if enabled)		Desktop mode	14.3	14.6	14.9	V
		Notebook mode		23.5		V
Reference Voltage and DAC						
Boot Voltage Range[1]				0.25-1.52		V
System Accuracy[3]		VID = 1.55V-2.3V	-1.1		1.1	%VID
		VID = 1.0V–1.5V	-0.5		0.5	%VID
		VID = 0.8 –0.995V	-5.0		5.0	mV
		VID = 0.25 –0.795V	-8		8	mV
External reference resistor	RRES	1% external bias resistor		7.5		kΩ
Oscillator & PWM Generator						
Internal oscillator[1]				96		MHz
Frequency Accuracy[2]			-2.5		2.5	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PWM Frequency Range[1]				200-2000		kHz
PWM frequency step size[1]				0.83-83		kHz
PWM resolution[1]					160	ps
NTC Temperature Sense	**TSEN1**					
Output Current		For TSEN = 0 to 1.2V	96	100	104	µA
Accuracy[1]		at 100°C (ideal NTC)	96		104	°C
Digital Inputs – Low Vth Type 1	**EN, VR_HOT (during PoR)**					
Input High Voltage			0.7	-	-	V
Input Low Voltage			-	-	0.35	V
Input Leakage Current		Vpad = 0 to 2V	-	-	±5	µA
Digital inputs - LVTTL	**SM_DIO, SM_CLK, ADDR_PROT**					
Input voltage high			2.1			V
Input voltage low					0.8	V
Input leakage		Vpad=0 to 3.6V			±1	µA
Remote voltage sense inputs	**VSEN, VRTN, VSEN_L2, VRTN_L2**					
VSENx Input current		Vout = 0.5V to 1.5V		-250 to +250		uA
VRTNx Input current				-500		uA
Differential Input voltage range[1]		VRTN= ±100mV		0 to 2.6		V
VRTN Input CM voltage[1]				-100 to 100		mV
Remote current sense inputs	**ISEN/IRTNx**					
Voltage range[1]				-0.1 to 2.7		V
Analog Address/Level Inputs	**ADDR_PROT**	**16 levels**				
Output Current[1]		Vpad = 0 to 1.2V	96	100	104	µA
Open-Drain outputs - 4mA drive	**PGood1, PGood2, SM_DIO, SM_ALERT**					
Output low voltage		4mA			0.3	V
Output leakage		Vpad=0 to 3.6V			±5	µA
Open-Drain outputs - 20mA drive	**VRHOT_ICRIT#**					
Output low voltage [1]		I=20mA			0.26	V
On resistance[1]		I=20mA	7	9	13	Ω
Tri-state leakage	I_{leak}	Vpad=0 to 3.6V			±5	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PWM I/O	**PWMx**					
Output low voltage (Tri-state mode)		I=-4mA			0.4	V
Output high voltage (Tri-state mode)		I=+4mA	2.9			V
Tri-state leakage		Vpad = 0 to Vcc			±1	µA
PWM auto-detect inputs (when 3.3V is applied) – if enabled						
Input voltage high			1.3			V
Input voltage low					0.5	V
I2C/PMBus & Reporting						
Bus Speed [1]		Normal		100		kHz
		Fast		400		
		Maximum		1000		
Iout & Vout filter [1]		Selectable		3.2 or 52		Hz
Iout & Vout Update rate [1]				20.8		kHz
Vin & Temperature filter [1]		Selectable		3.2 or 52		Hz
Vin & Temperature update rate [1]				20.8		kHz
Vin range reporting [1]		With 14:1 divider		0-15		V
		With 22:1 divider		0-25		
Vin accuracy reporting		With 1% resistors,	-2		+2	%
Vin resolution reporting [1]				62.5		mV
Vout range reporting [1]					2.2	V
Vout accuracy reporting [1]		No load-line		± 0.5		%
Vout resolution reporting [1]		Vout < 2V		7.8		mV
Iout range reporting [1]		Per phase	0		62	A
Iout accuracy reporting [1]		Maximum load, all phases active (based on DCR, NTC and # active phases)		±2		%
Iout resolution reporting [1]		Loop 1 (Iout<80A)		0.5		A
		Loop 2 (Iout<40A)		0.25		
Temperature range reporting[1]			0		135	°C
Temperature accuracy reporting [1]		At 100°C, with ideal NTC	-4		4	%
Temperature resolution reporting [1]				1		°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Fault Protection						
OVP threshold during Start-up (until output reaches 1V)		Selectable	1.2	1.275	1.35	V
OVP Operating threshold [1] (programmable)		Relative to VID (selectable)		150-500		mV
OVP filter delay [1]				160		ns
Output UVP threshold [1] (Programmable)		Relative to VID (selectable)		-150 to -500		mV
Fast OCP range [1]		Per phase		0-62		A
Fast OCP filter bandwidth [1]				60		kHz
Slow OCP filter bandwidth [1]		Programmable (equal to telemetry band-width)		3.2 or 52		Hz
OCP System accuracy [1]		System excluding DCR/sense resistor		±2		%
VR_HOT range[1]				64 to 127		°C
OTP range[1]		VR_HOT level + OTP Range		64 to 135		°C
Dynamic Phase Control						
Current filter bandwidth [1]		For Phase drop		5.3		KHz
Timing Information						
Automatic Configuration from MTP [1]	t_3-t_2 (figure 8)	3.3V ready to end of configuration			1	ms
Automatic trim time [1]	t_4-t_3 (Figure 8)				4	ms
EN Delay (to ramp start) [1]				3		us
VID Delay (to ramp start) [1]		Loop bandwidth dependent		5		us
PGood1/PGood2 Delay [1]		After reaching boot voltage		20		us

Notes

1. Guaranteed by design but not tested in production
2. PWM operating frequency will vary slightly as the number of phases changes (increases/decreases) because of the internal calculation involved in dividing a switching period evenly into the number of active phases.
3. System accuracy is for a temperature range of 0°C to +85°C. Accuracies will derate by a factor of 1.5x for temperatures outside the 0°C to +85°C range.

GENERAL DESCRIPTION

The IR36021 is a flexible, dual-loop (dual-channel), digital multiphase PWM buck controller optimized to convert a 12V input supply to a voltage below 2.445V (for VCC>3.1V). It is easily configurable for 1-2 phase operation on Loop #1 and 0-1 phase operation on Loop #2.

The unique partitioning of analog and digital circuits within the IR36021 provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip Multiple Time Programming memory (MTP) to store the IR36021 configuration parameters enables power supply designers to optimize their designs without changing external components.

The IR36021 controls two independent output voltages. Each voltage is controlled in an identical fashion, so that the user can configure and optimize each control loop individually. Unless otherwise described, the following functions are performed on the IR36021 on each control loop independently.

DIGITAL CONTROLLER & PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from the high-speed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user configurable to enable optimized system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

ADAPTIVE TRANSIENT ALGORITHM (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear digital transient control loop based on a proprietary algorithm.

MULTIPLE TIME PROGRAMMING MEMORY

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by cyclic redundancy code (CRC) checking on each power up. The controller will not start in the event of a CRC error.

The IR36021 offers up to 9 writes to configure basic device parameters such as frequency fault operating characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. The following pseudocode illustrates how to write the MTP:

 # write data
Set MTP Command Register = WRITE,
Line Pointer = An unused line
Poll MTP Command Register until Operation = IDLE.

 # verify data was written correctly
Issue a READ Command; then poll OTP Operation Register till Operation = IDLE
Verify that the Read Succeeded

INTERNAL OSCILLATOR

The IR36021 has a single 96MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The single internal oscillator is also used to set the switching frequency on each loop. The switching frequency for the two loops can be set to different values independently. Therefore, the two channels switch asynchronously.

HIGH-PRECISION VOLTAGE REFERENCE

The internal high-precision voltage reference supplies the required reference voltages to the DACs, ADCs and other analog circuits. This factory trimmed reference is guaranteed over temperature and manufacturing variations.

HIGH PRECISION CURRENT REFERENCE

An on-chip precision current reference is derived using an off-chip precision resistor connected to the RRES pin of the IR36021. RRES must be a 7.5kΩ, 1% tolerance resistor, placed very close to the controller pin to minimize parasitics.

VOLTAGE SENSE

An error voltage is generated from the difference between the target voltage and load-line (if implemented), and the differential, remotely sensed, output voltage. For each loop, the error voltage is digitized by a high-speed, high-

precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

CURRENT SENSE

Lossless inductor DCR or precision resistor current sensing is used to accurately measure individual phase currents. Using a simple off-chip thermistor, resistor and capacitor network for each loop, a thermally compensated loadline is generated to meet the given power system requirement. A filtered voltage, which is a function of the total load current and the target loadline resistance, is summed into each voltage sense path to accomplish the Active Voltage Positioning (AVP) function.

MOSFET DRIVER AND DRMOS COMPATIBILITY

The output PWM signals of the IR36021 are designed for compatibility with the CHL85xx family of active tri-level (ATL) MOSFET drivers. CHL85xx drivers have a fast disable capability which enables any phase to be turned off on-the-fly. It supports power-saving control modes, improved transient response, and superior on the fly phase dropping without having to route multiple output disable (ODB or SMOD) signals.

In addition, the IR36021 provides the flexibility to configure PWM levels to operate with external MOSFET drivers or driver-MOSFET (DrMOS) devices that support Industry standard +3.3V tri-state signaling.

I2C & PMBUS INTERFACE

An I2C or PMBus interface is used to communicate with the IR36021. This two-wire serial interface consists of clock and data signals and operates as fast as 1MHz. The bus provides read and write access to the internal registers for configuration and monitoring of operating parameters and can also be used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the IR36021 is programmed into MTP. The IR36021, additionally, supports pin-programming of the address.

To protect customer configuration and information, the I2C interface can be completely locked to provide no access or configured for limited access with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry only mode which allows reads from the telemetry registers only.

The IR36021 provides a hardware pin security option to provide extra protection. The protect pin is shared with the ADDR_PROT pin and is automatically engaged once the address is read. The pin must be driven high to disable protection. The pin can be enabled or disabled by a configuration setting in MTP.

The IR36021 supports the packet error checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. Refer to the PMBus Command Codes section on page 37.

IR DIGITAL POWER DESIGN CENTER (DPDC) GUI

The IR DPDC GUI provides the designer with a comprehensive design environment that includes screens to calculate VR efficiency and DC error budget, design the thermal compensation networks and feedback loops, and produce calculated Bode plots and output impedance plots. The DPDC environment is a key utility for design optimization, debug, and validation of designs that save designer significant time, allowing faster time-to-market (TTM).

The DPDC also allows real-time design optimization and real-time monitoring of key parameters such as output current and power, input current and power, efficiency, phase currents, temperature, and faults.

The IR DPDC GUI allows access to the system configuration settings for switching frequency, MOSFET driver compatibility, soft start rate, automatic power state and diode emulation, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and over-temperature.

PROGRAMMING

Once a design is complete, the DPDC produces a complete configuration file.

The configuration file can be re-coded into an I2C/PMBus master (e.g. a Test System) and loaded into the IR36021 using the bus protocols described on page 35. The IR36021 has a special in-circuit programming mode that allows the MTP to be loaded at board test in mass production without powering on the entire board.

REAL-TIME MONITORING

The IR36021 can be accessed through the use of PMBus Command codes (described on page 37) to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, efficiency, and temperature.

THEORY OF OPERATION

DEVICE POWER-ON AND INITIALIZATION

The IR36021 is powered from a 3.3V DC supply. Figure 8 shows the timing diagram during device initialization. An internal LDO generates a 1.8V rail to power the control logic within the device. During initial startup, the 1.8V rail follows the rising 3.3V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at t_1 as the 1.8V rail is ramping up. Until soft-start begins, the IR36021 PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at t_2 when the 3.3V supply is high enough for the internal bias central to generate 1.8V. At this time, if enabled in MTP and when the VINSEN voltage is valid, the controller will detect the populated phases by sensing the voltage on the PWM pins. If the voltage is less than the Auto Phase Detect threshold (unused PWMs are grounded), the controller assumes the phase is unpopulated. Once the phase detection is complete the contents of the MTP are transferred to the registers by time t_3 and the automatic trim routines are complete by time t_4. The register settings and number of phases define the controller performance specific to the VR configuration - including trim settings, soft start ramp rate, boot voltage and PWM signal compatibility with the MOSFET driver.

Once the registers are loaded from MTP, the designer can use I2C to re-configure the registers to suit the specific VR design requirements if desired.

TEST MODE

Driving the ENABLE and VR_HOT pins low engages a special test mode in which the I2C address changes to 0Ah. This allows individual in-circuit programming of the controller. This is specifically useful in multi-controller systems that use a single I2C bus. Note that MTP will not load to the working registers until either Enable or VR_HOT goes high.

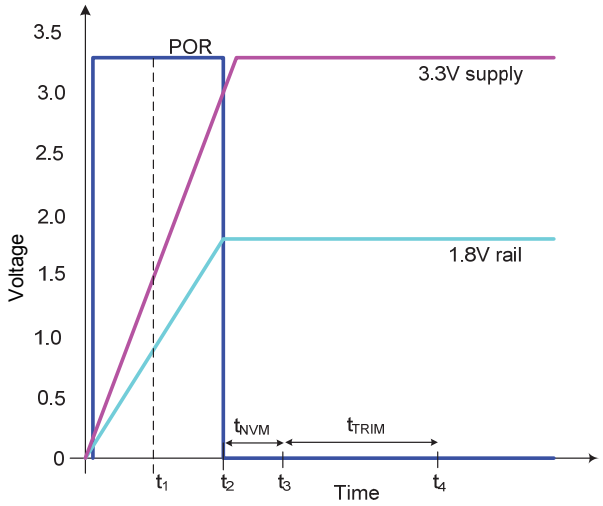


Figure 8: Controller Startup and Initialization

SUPPLY VOLTAGE

The controller is powered by the 3.3V supply rail. Once initialization of the device is complete, steady and stable supply voltage rails and a VR Enable signal (EN) are required to set the controller into an active state. A high EN signal is required to enable the PWM signals and begin the soft start sequence after the 3.3V and VIN supply rails are determined to be within the defined operating bands. To maintain proper operation of the device, glitches and narrow pulses should not be applied to EN pins.

The recommended decoupling for the 3.3V is shown in Figure 9a. The Vcc pins should have a 0.1µF X7R type ceramic capacitors placed as close as possible to the package. The V18A pin must have a 4.7µF, X5R type decoupling capacitor connected close to the package as shown in Figure 9b.

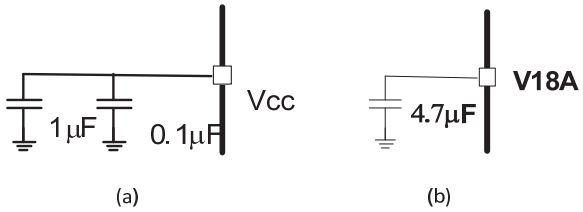


Figure 9: (a) Vcc 3.3V decoupling, (b) V18A decoupling

It should be noted that when powering up the system the 3.3V supply for IR36021 should be up before the bias voltage of the power stages ramp up. Likewise, when the system is shutdown, the bias voltage of the power stages should be disconnected before the 3.3V is ramped down (Figure 10).

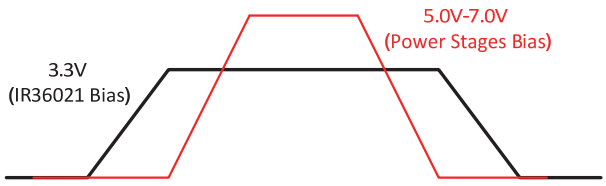


Figure 10: Correct sequencing of bias voltages

The IR36021 is designed to accommodate a wide variety of input power supplies and applications and offers programmability of the VINSEN turn-on/off voltages.

TABLE 1: VINSEN TURN-ON/OFF VOLTAGE RANGE

Threshold	Range
Turn-on	4.5V to 15.9375V in 1/16V steps[1]
Turn-off	4.5V to 15.9375V in 1/16V steps[1]

[1] *Must not be programmed below 4.5V*

The supply voltage on the VINSEN pin is compared against a programmable threshold. Once the rising VINSEN voltage crosses the turn-on threshold, EN is asserted and all PWM outputs become active. The VINSEN supply voltage is valid until it declines below its programmed turn-off level.

A 14:1 or 22:1 attenuation network is connected to the VINSEN pin as shown in Figure 11. Recommended values for a 12V system are R_{VIN_1} = 13kΩ and R_{VIN_2} = 1kΩ, with a 1% tolerance or better. Recommended values for a mobile 7V-19V system are R_{VIN_1} = 21kΩ and R_{VIN_2} = 1kΩ. C_{VINSEN} is required to have up to a maximum value of 10nF and a minimum 1nF for noise suppression.

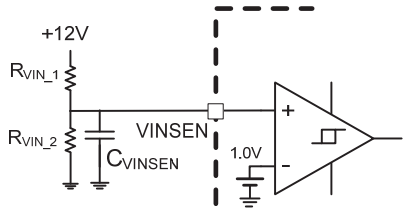


Figure 11: VINSEN resistor divider network

POWER-ON SEQUENCING

The VR poweron sequence is initiated when all of the following conditions are satisfied:

- IR36021 Vcc (+3.3V rail) > VCC UVLO
- Input Voltage (VINSEN rail) > Vin UVLO
- ENABLE is HIGH
- VR has no Over-current, Over-voltage or Under-voltage faults *on either rail depending on the settings*
- MTP transfer to configuration registers occurred without parity error

When the power-on sequence is initiated, and with VBoot set to > 0V, both rails will ramp to their configured boot voltages and assert PGood1 and PGood2. The slew rate to VBoot is programmed per Table 2. This table shows that the slew-rate of VBoot is either ½ or ¼ of the fast rate shown in the first two columns. There is a 1/10 multiplier, which if chosen will reduce the fast rate by a factor of 10. This multiplier can be chosen by setting the highest bit of the register# 31Hex (refer to IR36021 Register Map).

On the other hand, when the poweron sequence is initiated, If Vboot= 0V, the VR will stay at 0V and will not soft-start until an operation command (margin high/low) is received from the PMBUs or the manual_VID registers are loaded by a nonzero value through I2C (for example through GUI). Note that the slewrate of Vout when margining or manual_VID registers are used is equal to the fast rate shown in Table 2.

If a margining command is executed before EN goes high, the device will startup and rise to VBoot and then go to the margin voltage.

When EN1 and EN2 are both active, each loop starts when its own Enable goes high provided that other startup conditions are met as mentioned before. Under this condition, usually both loops start together when Vin voltage is applied.

The two loops can be configured to share a single Enable signal (EN1). Under this condition EN2 is configured to be Dont Care. This mode of operation is useful when sequencing is required. For example, one of the loops can be configured to follow the other loop with a delay at startup (Figure 12) or both loops can be configured to start simultaneously with a programmable delay from EN1 going high (Figure 13). The different options for delay are summarized in Table 3.

TABLE 2: SLEW RATES

	Fast Rate		½ Multiplier		¼ Multiplier	
mV/µs	**10**	1	**5.0**	0.5	**2.50**	0.25
	15	1.5	**7.5**	0.75	**3.75**	0.375
	20	2	**10**	1	**5.00**	0.5
	25	2.5	**12.5**	1.25	**6.25**	0.625

It should be noted that shutting down with Enable is always a soft shutdown meaning that Vout is ramped down to 0V (Figure 14). On the other hand, shutdown due to input under-voltage or most of the faults is a hard shutdown meaning that both high side and low side FETs are turned off (Figure 15).

TABLE 3: OPTIONS FOR STARTUP SEQUENCING DELAY (COMMON EN)

Delay [ms]
0
0.25
0.5
1
2.5
5
10

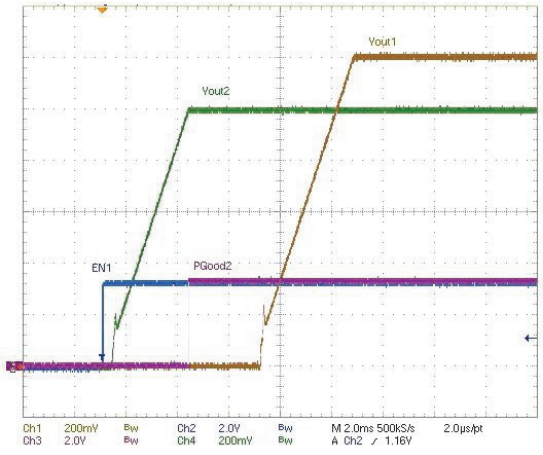


Figure 12: Enable-based Startup, loop1 follows loop2 with a delay of 2.5ms from PGood2 rising edge.

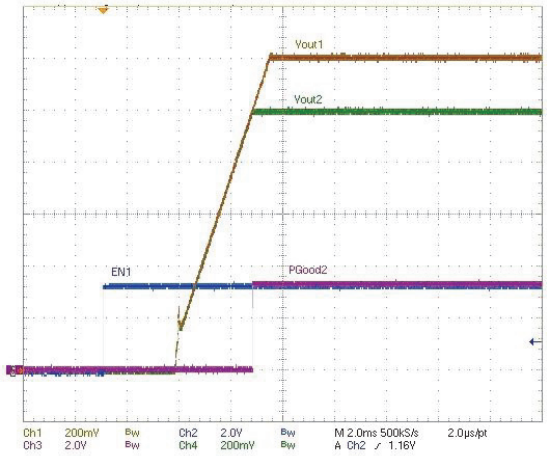


Figure 13: Enable-based startup, both loops start with a delay of 2.5ms from EN1 going high.

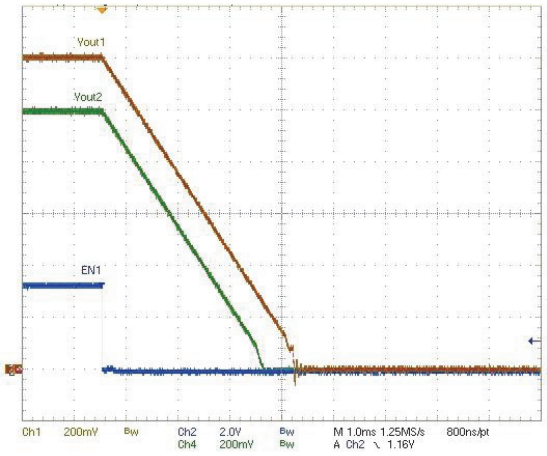


Figure 14: Enable based shutdown, both loops configured to follow EN1. Vout1 and Vout2 are ramped down to 0V.

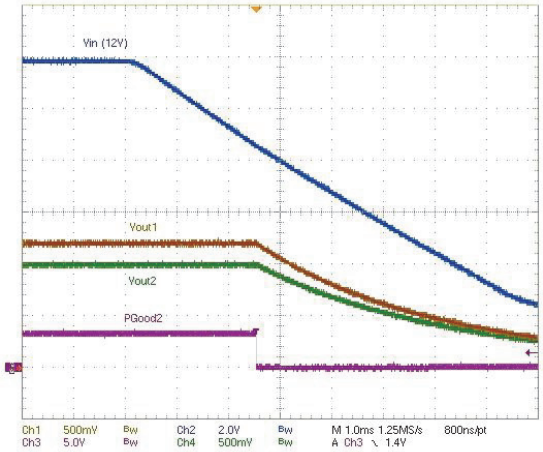


Figure 15: Vin based shutdown, the high side and low side FETs are turned off as soon as Vin falls below UVLO threshold.

Boot Voltage

The IR36021 Vboot voltage is fully programmable in MTP to the range shown in Table 4.

TABLE 4: VBOOT RANGE

Loop	Boot Voltage
Loop 1	0 to 1.52V in 5mV steps, 1st step=250mV
Loop 2	0 to 1.52V in 5mV steps, 1st step=250mV

I2C Address

A resistor connected from ADDR_PROT pin to ground defines the IC2 address when Vcc becomes valid. Note that a 0.01uF capacitor must be placed across the resistor

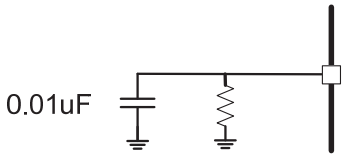


Figure 16: ADDR_PROT Pin Components

VID Offset

The boot voltage (VBoot) can be offset according to Table 5. This extends the range of the VBoot voltage a little and is useful when voltages a little above 1.52V or a little below 250mV is required. The offset is stored in register #26Hex and can be stored in MTP memory (for more information, refer to the Register-Map of the device). This offset is effective when the output voltage is controlled by the manual_VID registers as well. However, when the output voltage is controlled by margining commands this offset is not effective.

Note the Vmax register (reg 3D) must be set appropriately to allow the required output voltage offset.

PHASING

The number of phases enabled on each loop of the IR36021 is shown in Table 6. When operated in 2-phase mode, the two phases of loop1 are 180 degrees out of phase. This increases the effective ripple frequency and reduces the required output and input filter capacitances.

TABLE 5: VID OFFSET

Parameter	Memory	Range	Step Size
Output Voltage	R/W	-35mV to +40mV	5mV

TABLE 6: LOOP CONFIGURATION

Configuration	Loop1	Loop2
2+0	2-phases	-
1+0	1-phase	-
2+1	2-phases	1-phase
1+1	1-phase	1-phase

UNUSED PHASES

Based upon the configuration shown in Table 28 unused phases are disabled. Note that when loop1 operates in singlephase mode, PWM1b is disabled. Disabled PWM outputs should be left floating unless the 'populated phase detection' feature is used. If so, the unused PWM outputs should be grounded. The reason is that IR36021 detects the number of populated phases at start-up by comparing the voltage on the PWM pin against the phase detection threshold. It is easier and recommended to disable the 'populated phase detection' feature at startup.

SWITCHING FREQUENCY

The phase switching frequency (Fsw) of the IR36021 is set by a user configurable register independently for each loop. The IR36021 provides fine granularity as shown in Figure 17. The IR36021 oscillator is factory trimmed to guarantee accuracy.

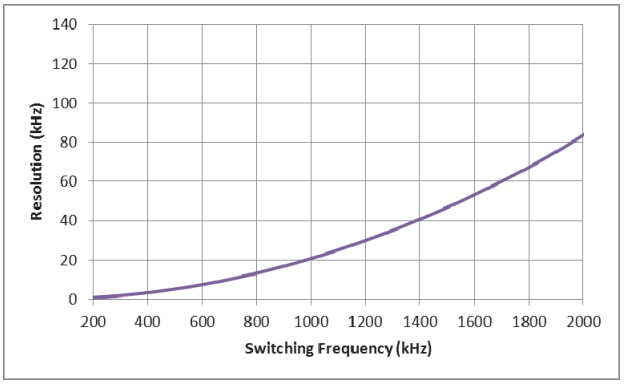


Figure 17: Switching Frequency Resolution

MOSFET DRIVER AND POWIRSTAGE SELECTION

The PWM signals from the active phases of the IR36021 are designed to operate industry standard tri-state type drivers or PowIRstage® devices. The logic operation for the tri-state drivers is depicted in Figures 18.

Note that the PWM outputs are tri-stated whenever the controller is disabled (EN = low), the shut-down ramp has completed or before the soft-start ramp is initiated.

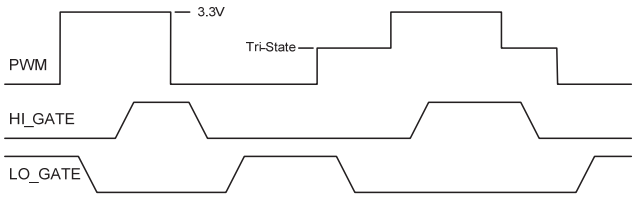


Figure 18: 3.3V Tri-state Driver Logic Levels

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The IR36021 VCPU and VRTN pins for each loop are connected to the load sense pins of each output voltage to provide true differential remote voltage sensing with high common-mode rejection. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC.

As shown in Figure 19, the Vsen and Vrtn inputs have a 2KΩ pull-up to an internal 1V rail. This causes some current flow in the Vsen and Vrtn lines so external impedance should be kept to a minimum to avoid creating an offset in the sensed output voltage.

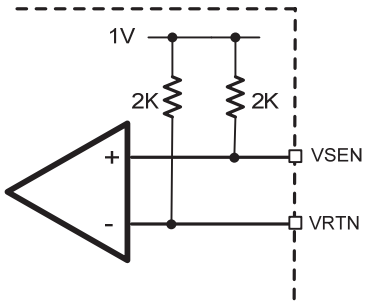


Figure 19: Output Voltage sensing impedance

CURRENT SENSING

The IR36021 provides per phase current sensing to support accurate Adaptive Voltage Positioning (AVP), current balancing, and over-current protection. The differential current sense scheme supports both lossless inductor DCR and per phase precision resistor current sensing techniques.

For DCR sensing, a suitable resistor-capacitor network of R_{sen} and C_{sen} is connected across the inductor in each phase as shown in Figure 20. The time constant of this RC network is set to equal the inductor time constant (L/DCR) such that the voltage across the capacitor C_{sen} is equal to the voltage across the inductor DCR.

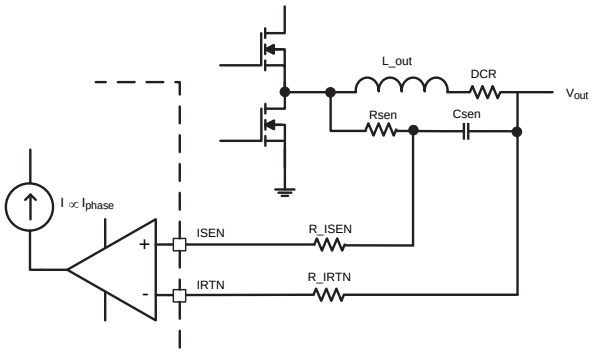


Figure 20: DCR Current Sensing

A current proportional to the inductor current in each phase is generated and used for per phase current balancing. The individual phase current signals are summed to arrive at the total current.

The phase currents and total current are quantized by the monitor ADC and used to implement the current monitoring and OCP features. The total current is also summed with the output the output voltage DAC (VID DAC) to implement the AVP function (load-line function).

The recommended value for C_{sen} is a 100nF NPO type capacitor. To prevent undershooting of the output voltage during load transients, the R_{sen} resistor can be calculated by:

$$R_{sen} = \frac{1.05 * L\_out}{C_{sen} * DCR}$$

Identical resistors (R_ISEN and R_IRTN) are connected to the ISEN and IRTN pins of each phase for the best common mode rejection. The required value is:

R_ISEN, R_IRTN = 301Ω, 1% resistor

These components must be placed close to the IR36021 pins.

CURRENT BALANCING & OFFSET

The IR36021 provides accurate digital phase current balancing for loop1 when it is configured to operate in 2-phase mode. Current balancing equalizes the current across the two phases. This improves efficiency, prevents hotspots and reduces the possibility of inductor saturation.

The sensed currents for each phase are converted to a voltage and are multiplexed into the monitor ADC. The digitized currents are lowpass filtered and passed through a proprietary current balance algorithm to enable the equalization of the current in two phases.

Figure 21 shows that due to component and layout mismatches and other offsets in the control and measurement circuits, the reported current values in the GUI are a little different for the two phases (loop1) when current balancing is disabled. Figure 22 shows that when current balancing is enabled the current in two phases become almost equal.

In addition, the IR36021 allows the user to offset phase currents to optimize the thermal solution. Figure 23 shows that Phase 1 current has been programmed to have approximately 30% more current than the other phase. 30% is the maximum offset that can be applied in the system. For the graphs shown in Figures 21, 22, and 23 the load current has been measured by a multi-meter whereas the phase currents are the values reported in the GUI.

In addition to the low speed phase balancing, mentioned above, there is a proprietary highspeed active phase current balancing (HSPB) which operates during load transients. HSBP's purpose is to eliminate current imbalance that can result from a load current oscillating near the switching frequency. The phase pulse widths are compared and the largest pulse is skipped if its pulse width exceeds an internally set threshold relative to the smallest phase. This ensures that the phases remain balanced during high frequency load transients.

High speed phase balancing (HSPB) and regular (low-speed) phase balancing can be activated/disabled independently.

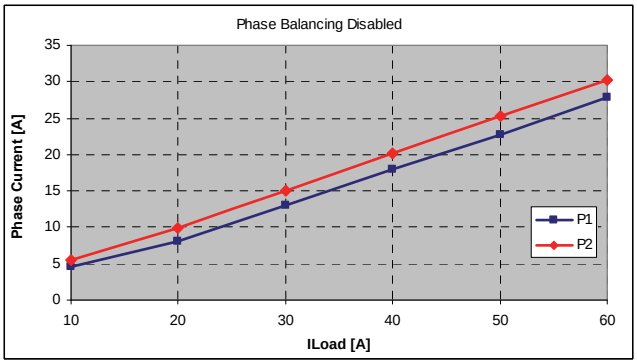


Figure 21: Phase Currents for a tested sample when phase balancing is disabled. The current in phase 2 is a little more than phase 1. The currents values are the reported GUI values.

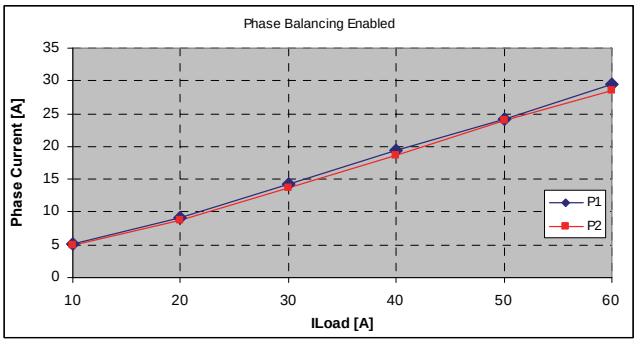


Figure 22: Phase Currents measured when phase-balancing is activated for the same tested sample used for Figure 21 . The currents in two phases are almost equal.

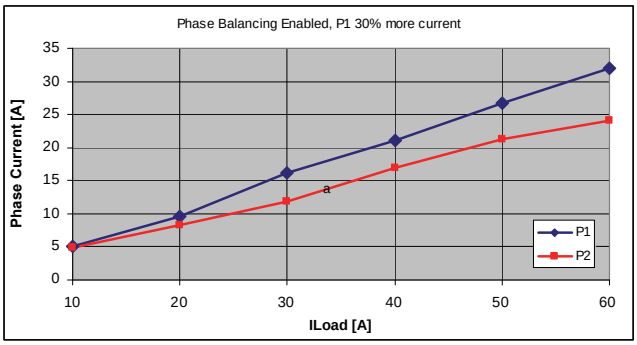


Figure 23: Phase Currents measured when phase-balancing is activated and the current in phase 1 is programmed to be about 30% more than the current in phase 2 (same tested sample).

CURRENT CALIBRATION

For optimizing the current measurement accuracy of a design or even individual boards, the IR36021 contains a register in MTP which can store a user-programmed Total Current Offset to zero the no-load current reading. Refer to Table 27 for output current calibration registers.

LOAD LINE

The IR36021 enables the implementation of accurate, temperature compensated load lines on both loops. The load line is set by an external resistor R_{CS}, as shown in Figure 24 and the nominal value must also be stored in MTP. The stored load line, scaling and gain values provides the IR36021 with the scaling factor for the digital computation of the total current to determine the OCP threshold and I2C current and output voltage reporting.

The load line ranges for IR36021 are shown in Table 7.

TABLE 7: LOAD LINE SETTINGS

	Loop #1	Loop #2
Minimum	0.0 mΩ	0.0 mΩ
Maximum	6.375 mΩ	12.75 mΩ
Resolution	0.025 mΩ	0.050 mΩ

Figure 24 shows a typical 1.3mΩ loadline measurement with minimum and maximum error ranges. The controller accuracy lies well within common processor requirements.

For each loop, the sensed current from all the active phases is summed and applied to a resistor network across the RSCP and RCSM pins. This generates a precise proportional voltage which is summed with the sensed output voltage and VID DAC reference to form the error voltage. Also part of the network shown in Figure 32 is thermistor, R_{Th}. For proper loadline temperature compensation, the thermistor is placed near the phase one inductor to accurately sense the inductor temperature.

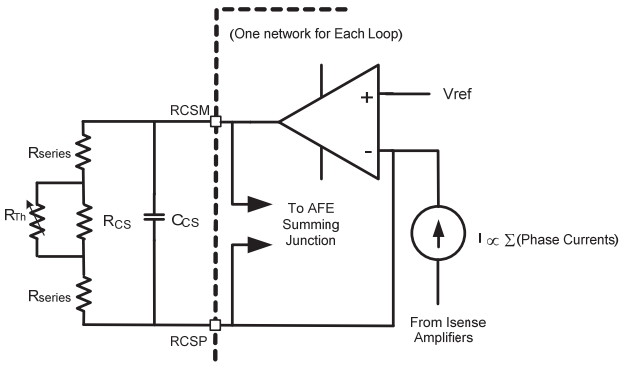


Figure 24: Load Line & Thermal Compensation

The resistor R_{CS} is calculated using the following procedure:

First the designer calculates the $R_{CSeffective}$ or the total effective parallel resistance across the RSCP and RCSM pins. It is defined by:

$$R_{CS\,effective} = 8 \times R\_ISEN \times \frac{R_{LL}}{DCR}$$

Where R_{LL} is the desired loadline, typically 1.0mΩ, DCR is DC resistance of the phase inductor, and R_ISEN is the series resistor across the inductor sense circuit. The required value for R_ISEN is a 301Ω, 1% tolerance. Then the designer chooses a suitable NTC thermistor. Thermistor R_{th} is typically selected to have the lowest thermal coefficient and tightest tolerance in a standard available package. A typical value for the NTC will be 10kΩ, 1% tolerance. Recommended thermistors are shown in Table 8.

TABLE 8: 10K 1% NTC THERMISTORS

Murata	NCP18XH103F03RB
Panasonic	ERTJ1VG103FA
TDK	NTCG163JF103F

Then the designer calculates R_{CS} using the following equation:

$$R_{CS} = \frac{1}{\frac{1}{R_{CSeffective} - 2 \times R_{series}} - \frac{1}{R_{Th}}}$$

R_{series} is selected to achieve minimum loadline error over temperature. The IR DPDC (GUI) provides a graphical tool that allows the user to easily calculate the resistor values for minimum error.

The capacitor C_{CS} is defined by the following equation:

$$C_{CS} = \frac{1}{2 \times \pi \times RCSeffective \times f_{AVP}}$$

where, f_{AVP} is the user selectable current sense AVP bandwidth. The best bandwidth is typically in the range of 200kHz to 300kHz.

Setting 0mΩ Loadline

The load line is turned off by setting a digital bit in the IR36021 register map. This is a separate bit from the load line settings for each loop.

Even though the loadline is disabled digitally, the resistors and loadline and scaling registers should be set such that the load line is at least 3 times the value of low ohmic DCR inductors (<0.5mΩ) or 1 times the DCR value for high ohmic inductors (>0.5mΩ), e.g. if the inductor(s) DCR is 0.3mΩ, a notional 0.9 mΩ load line should be set. For accurate current measurement and OCP threshold with the loadline disabled, the output current gain and scaling registers must be set to the same value as the loadline set with the external resistor network. With loadline disabled, the thermistor and Css capacitor must still be installed to insure accuracy of the current measurement.

DIGITAL FEEDBACK LOOP & PWM

The IR36021 uses a digital feedback loop to minimize the requirement for output decoupling and maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized. This error voltage is then passed through a low pass filter to smooth ripple and then passed through a PID (Proportional Integral Derivative) compensator followed by an additional single pole filter. The loop compensation parameters K_P (proportional coefficient), K_I (integral coefficient), and K_D (derivative coefficient) and low-pass filter pole locations are user configurable to optimize the VR design for the chosen external components.

The IR36021 significantly reduces design time because the loop coefficients need to be calculated only once. Simply enable any number of phases (1 or 2 for loop1) and design the compensation coefficients. The IR36021 will intelligently scale the coefficients and low-pass filters automatically as one phase is dynamically added and dropped to maintain optimum stability. In other words, the loop-band-width does not change significantly (decreases a little) as the loop switches from 2-phase to 1-phase operation.

Each of the proportional, integral and derivative terms is a 6-bit value stored in MTP that is decoded by the IC's digital code. This allows the designer to set the converter bandwidth and phase margin to the desired values.

The compensator transfer function is defined as

$$(Kp + \frac{Ki}{s} + Kd \bullet s) \bullet \left(\frac{1}{1 + \frac{s}{\omega p_1}} \right) \bullet \left(\frac{1}{1 + \frac{s}{\omega p_2}} \right)$$

where ωp_1 and ωp_2 are configurable poles typically positioned to filter noise and ripple and roll off the high-frequency gain that the K_D term creates.

The outputs of the compensator and the phase current balance block are fed into a digital PWM pulse generator to generate the PWM pulses for the active phases. The digital PWM generator has a native time resolution of 625ps which is combined with digital dithering to provide an effective PWM resolution of 156.25ps. This ensures that there is no limit cycling when operating at the highest switching frequency.

ADAPTIVE TRANSIENT ALGORITHM (ATA)

The IR36021 Adaptive Transient Algorithm (ATA) is a high speed non-linear control technique that speeds up the controller response to loading transients and reduces the required output bulk capacitance for reduced system cost. ATA is not very effective for single-phase rails (loop2). In addition, it is more effective when used in conjunction with the load-line.

A high-speed digitizer measures both the magnitude and slope of the error signal to predict the load current transient. If the magnitude and slope of the error signal exceed predefined thresholds, the ATA is activated. When activated, the ATA bypasses the PID control momentarily during load transients to achieve very wideband closed loop control and smoothly transitions back to PID control during steady state load conditions. During ATA operation, the width of the PWM pulses is not changed. However, the positions of the pulses are changed. For example, in a loading transient when ATA is activated, the PWM pulses come closer in all active phases to compensate for the undershoot caused by the transient. Figure 25 illustrates the transient performance improvement provided by the ATA showing the clear reduction in undershoot and overshoot and recovery time. Figure 26 is a close up of a loadstep illustrating the fast reaction time of ATA and how the algorithm changes the pulse phase relationships. ATA settings/thresholds can be modified in the GUI. In addition, it can be disabled if desired. The ATA settings are stored in MTP memory.

During a load transient overshoot, the ATA can also be programmed to turn off the low-side MOSFETS instead of holding them on. This forces the load current to flow through the larger forward voltage of the FET body diode and helps to reduce the overshoot created during a load release (Figure 27). This is not recommended when there is no load-line and there is no steady state load. This is because unloading creates a Vout overshoot and without

load (and with low-side MOSFETs being off) it can take a relatively long time for the output voltage to decay down to the steady state value.

Note that ATA is more effective on multi-phase rails (e.g. loop1) and when used in conjunction with the load-line.

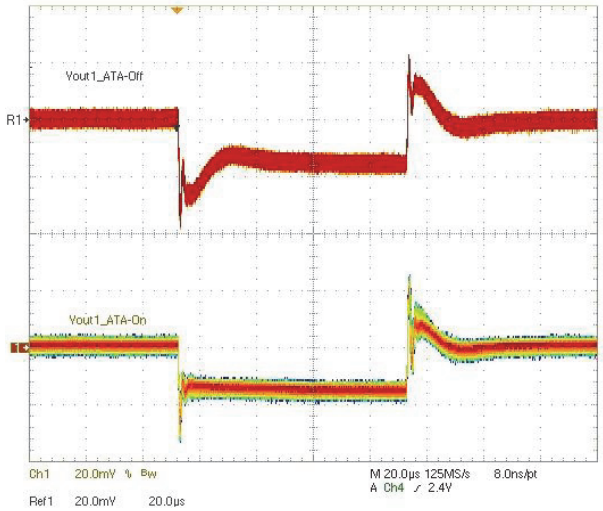


Figure 25: Vout1 (2phase) response to a transient. ATA Enable/Disable Comparison, load-line is enabled.

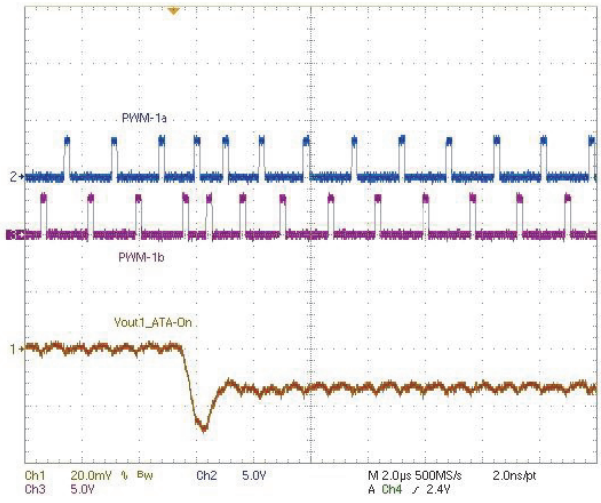


Figure 26: ATA close up when a load is applied.

DYNAMIC VID SLEW RATE

VID refers to the code inside a register which corresponds to a specific output voltage. This code can be changed in the GUI by changing the manual_VID registers (through I2C communication) or by corresponding commands (for example margining commands) sent through PMBus. The IR36021 provides the VR designer with up to 8 slew rates by selecting a slew rate setting as shown in the fast-rate column in Table 2.

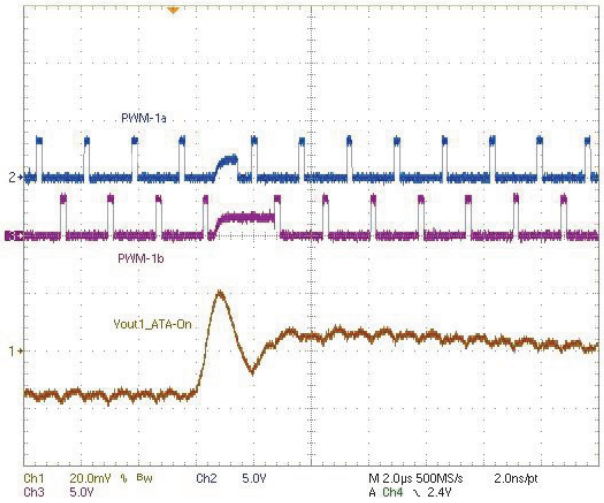


Figure 27: Diode Emulation (ATA is on) during a load release

EFFICIENCY SHAPING

IR36021 features Efficiency Shaping Technology that enables VR designers to cost-effectively maximize system efficiency. Efficiency Shaping Technology consists of phase-shedding (sometimes referred to as 'Dynamic Phase Control', DPC) and diode-emulation to achieve the best VR efficiency at a given cost point.

POWER-SAVING STATES

The IR36021 can be programmed to do phase shedding for loop1 and/or go into diode emulation at light load for both loops. Both of these mechanisms improve efficiency at light loads at the expense of more output voltage ripple. Phase-shedding and diode-emulation can be enabled/disabled independently from each other and independently for each loop. To improve efficiency for loop1 at light loads when there is no transient, it is recommended to program the device to do phase shedding at about 20A and as the current decreases to about 3-5A the diode-emulation should be activated for the running phase (phase-1a). This sequence can be explained using Power States as summarized in Table 9. For loop2, since it is 1phase, PS1 and PS0 are identical.

When there are transients, it is recommended to use either phase shedding or diode emulation since using both mechanisms can further increase the output voltage ripple in some conditions.

TABLE 9: POWER STATES

Power State	Mode	Recommended Current
PS0	Full Power, 2Φ(loop1)	Maximum
PS1	Light Load 1Φ	<20A
PS2	Light Load, 1Φ with Diode Emulation	<5A

The Power States may be commanded through I2C/PMBus, or the IR36021 can automatically step through the Power States based upon the regulator conditions as summarized in Table 10. Auto Mode is ensued when diode-emulation is enabled by setting a flag. It should be noted that to use the commands (I2C/PMBus), Auto Mode should be disabled. Furthermore, it is recommended to use the Auto Mode or phase-shedding option as much as possible instead or using the commands.

TABLE 10: POWER STATE ENTRY/EXIT

	Auto Mode disabled	Auto Mode
PS1 Entry	a) based on current level if phase-shed is enabled b) via command c) based on current level if commanded to PS2	based on the current level if phase-shed is enabled
PS1 Exit	a) Command to PS0 b) Command to PS2 if current level is low c) Current level to PS0 d) current limit To PS0 fe To PS0 if Vout drops below a threshold (fc_hth)	a) Current level to PS0 b) Current level to PS2 c) to PS0 if Vout drops below a threshold (fc_hth)
PS2 Entry	a) Command (if current is lower than threshold)	Current level in phase-1a
PS2 Exit	a) Command to PS1 b) Command to PS0 c) Current level To PS1 d) Current limit to PS0 e) To PS0 if Vout drops below a threshold (le_th)	a) to PS0 if Vout drops below a threshold (le_th) b) To PS0 or PS1 based on current

PHASE SHEDDING / DYNAMIC PHASE CONTROL (DPC)

The designer can configure the VR to dynamically add or shed one phase as the load current varies. Phase shedding (or DPC) reduces the number of phases (Figures 28-30) based upon monitoring both filtered total current and error voltage over the DPC filter window. Monitoring the error voltage insures that the VR will not drop a phase during large load oscillations.

Figure 28 shows that at startup, if the load current is below the 2-phase current threshold, one phase is dropped shortly after PGood1 goes high.

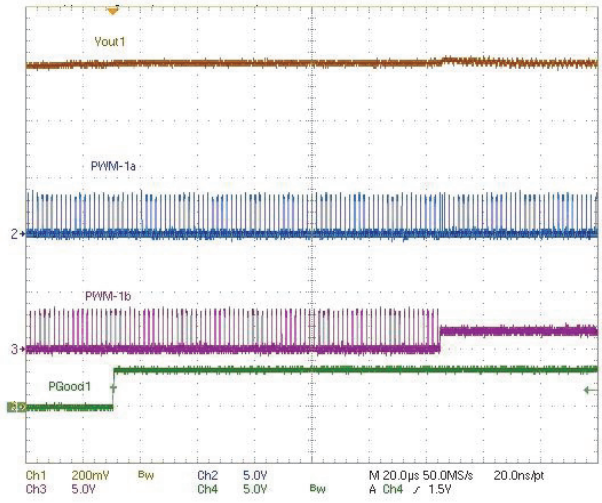


Figure 28: Phase Shed 2Φ à 1Φ at startup

During a large load step for loop1 and based upon the error voltage, the controller instantly goes to 2-phase operation and will remain there for the DPC filter delay (BW≈40kHz) after which a phase will be dropped depending on the load current (Figure 29). The error-threshold, which should be exceeded, is called 'L1_fc_hth'. This threshold is among the ATA settings. The ATA circuitry ensures that the idle phase is activated with optimum timing during a load step (this is still valid even if ATA is disabled).

Figure 30 shows that how adding/dropping a phase is automatically done based on the current level. For this figure, the slew-rate of the load step is not high enough to make a Vout drop larger than the threshold. Therefore, phase dropping/adding is delayed because it is based on the measured load current which is low-pass filtered.

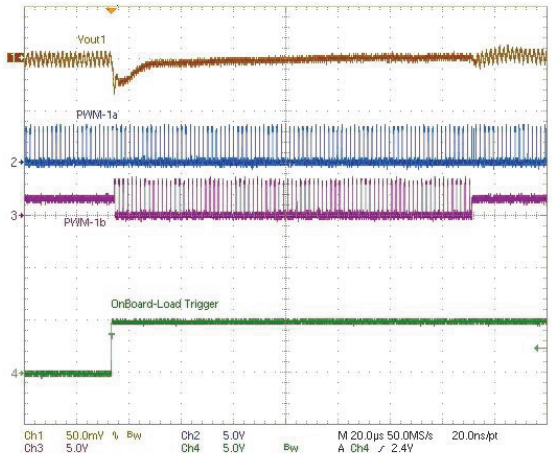


Figure 29: loop1 going from 1Φ to 2Φ operation due to a heavy load transient which causes Vout drop, 1Φ operation is resumed with a delay after Vout1 recoveres.

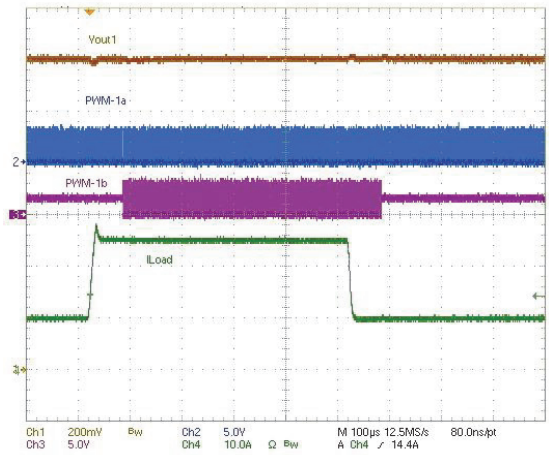


Figure 30: Wide View of Phase Shed/Add

Current limit and current balancing circuits remain active during ATA events to prevent inductor saturation and maintain even distribution of current across the active phases.

As mentioned before, loop coefficients are automatically scaled to the number of active phases to insure stability at all load currents.

The add/drop points for phase-1b can be set in 2A increments from 0 to 30A with a fixed 4A hysteresis. Setting the threshold to 0A will disable phase shedding.

As shown in Figure 31, with phase-shedding enabled, IR36021 provides light and medium load efficiency improvements. To generate the graphs shown in Figure 31, the inductor, the PCB and the controller loses have been taken into account in measurements.

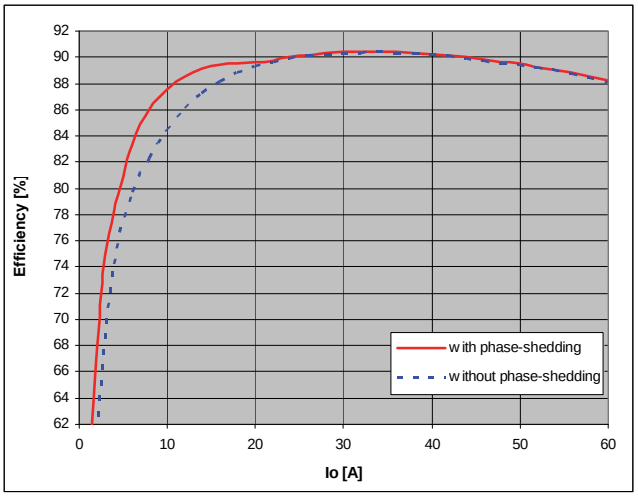


Figure 31: Typical Efficiency with phase-shedding for loop1, Vo1=1.2V, 600kHz/phase, 2 x IR3550 used as power-stages

DIODE EMULATION / DISCONTINUOUS MODE OPERATION

Under very light loads, efficiency can become dominated by MOSFET switching losses. In PS2 mode, the IR36021 operates as a constant on-time controller where the user sets the desired peak-to-peak ripple by programming an error threshold and an on-time duration (Table 11).

TABLE 11: PS2 MODE, CONSTANT ON-TIME CONTROL, PARAMETERS

MTP Register	Function
de_thresh	Sets the error voltage at which an on-time pulse is started in 2mV steps
Pulse_width_de	Sets the duration of the on-time pulse in 40ns steps. Note that this also sets the off-time in 160ns steps
Off-time_adjust	Reduces the calculated low-side FET on-time in 60ns steps. Useful for compensating for DrMOS or other drivers' tri-state delay for a better prediction of the zero-crossing
Le_th	error threshold to go from PS1/PS2 mode to full phase count. 4 mV resolution. If Vout drops by this amount, the control will be changed to full-phase count and diode-emulation is ended.
Ni_thresh	Total current threshold below which it is assumed that the inductor current has a negative component.

In PS2 mode (Constant-On-Time Mode), internal circuitry determines when the inductor current declines to zero on a cycle by cycle basis and shuts off the low-side MOSFET at the appropriate time in each cycle (Figure 32). This reduces conduction losses and also lowers the switching frequency resulting in improved efficiency because the inductor and low-side MOSFET are not sinking power from the output capacitors at light loads.

When diode-emulation is activated if phase-1b is active (i.e. phase-shedding is not active), PWM-1b becomes tri-state and phase-1a goes into constant-on-time mode simultaneously.

In diode-emulation mode, if Vout drops below a certain threshold (le_th) due to applying a load, the operation is switched to PWM instantly.

Industry standard tri-state drivers typically have slow tri-state entry times, typically which allows negative current to build up reducing efficiency and causing ringing. The *off_time_adjust* variable allows the designer to compensate for the tri-state delay by reducing the low-side FET on-time by an equivalent amount.

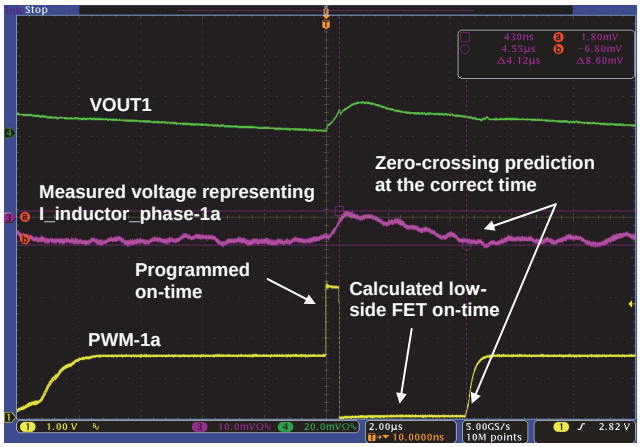


Figure 32: PS2 Active Diode Emulation Mode

FAULTS & PROTECTION

The comprehensive fault coverage of the IR36021 protects the VR against a variety of fault conditions. Faults are user configurable through the GUI which also displays the fault status. There are two types of fault monitoring registers. In addition to real-time fault registers, there are "sticky" fault registers that can only be cleared with an I2C command or 3.3V power cycle. These will indicate if any fault has occurred since the last power cycle, even if the fault has cleared itself and the VR has resumed normal operation. Table 12 lists the available faults.

TABLE 12: STICKY & NON-STICKY FAULTS

Register Type	Faults
Sticky	OTP, OCP, OVP, UVP, VIN UVLO, 3.3V UVLO, phase-fault, slow-OCP
Non-Sticky	

The controller has two programmable modes for determining how the controller responds to faults on the two loops. In combined mode, an over-current or under-voltage fault on either loop will trigger the programmed response on both loops (Figure 35). In individual mode, a loop will respond only to its own over-current or under-voltage fault independent from the other loop. Input under-voltage on 3.3V or VIN supplies, over-voltage on either loop or an over-temperature fault on controllers with single temperature sense will always shut down both loops.

Output Over-voltage Protection (OVP)

If the output voltage exceeds a user-programmable threshold (Table 15) above the set-point, the IR36021 detects an output over-voltage fault and latches on the low-side MOSFETS to limit the output voltage rise based on the settings in Table 13.

TABLE 13: OVP ACTION

OVP Action
Low-side MOSFET latched on
Low-side MOSFET on until Output<0.248V

Under OVP conditions, the low-side MOSFETs can be configured to remain latched indefinitely (Figure 33) or remain latched on until the output voltage falls below the threshold at which time the low-side MOSFETs are released (Figure 34). This release mode can reduce or prevent undershoot of the output voltage. In the release mode, if the output voltage rises above the OVP level the low side MOSFET's will again be turned on until Vout drops below the release threshold level.

During soft-start, OVP is triggered at the fixed soft-start level. This level can be chosen from three different values of 1.275V, 1.2V or 1.35V. Optionally, the OVP may be allowed to remain active while the IR36021 is disabled to prevent system leakage from over-voltaging the output (Table 14).

Note that when EN is pulled low, the device ramps down Vout. During this time OVP level is equal to the reference voltage (which is ramping down) plus the selected threshold (Table 15). When the soft-stop is done, the level is switched to fixed OVP level.

OVP is disabled whenever Vout is ramped down using I2C or PMBus commands.

TABLE 14: OVP OPTIONS

OVP_when-disabled setting	When active
On	IC disabled & IC enabled
Off	IC enabled

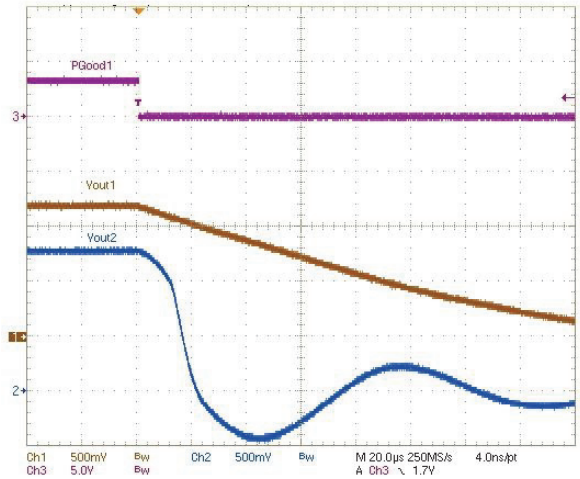


Figure 33: External bias caused OVP2, which shuts down both loops (EN2=low), Low-side MOSFET latched ON for loop2

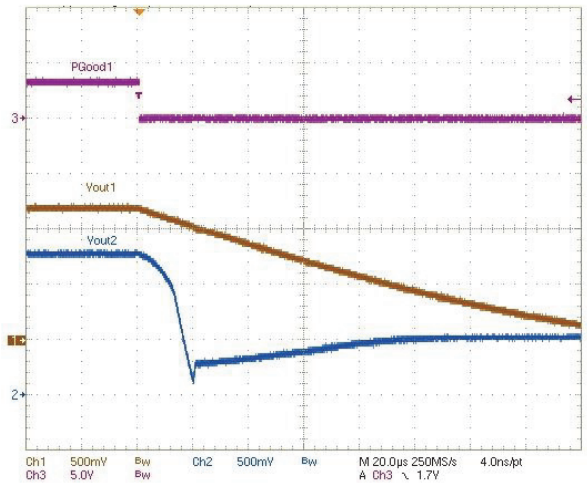


Figure 34: External bias caused OVP2, which shuts down both loops (EN2=low), MOSFET released when output<0.3V for loop2

Output Under-voltage Protection (UVP)

The IR36021 detects an output under-voltage condition if the sensed voltage at the CPU is below the user-programmable UVP threshold (Table 15) or a fixed 248mV as defined by the VID setting and with or without the load line (Using the fixed or programmable threshold, and the load line term is user selectable). Upon detecting an output under-voltage condition, the IR36021 responds in the same manner as the OCP, according to the setting selected in Table 16.

TABLE 15: OVP/UVP THRESHOLDS

Value	Threshold
0	150mV
1	200mV
2	250mV
3	325mV
4	350mV
5	375mV
6	400mV
7	500mV

Over-current Protection (OCP)

The IR36021 provides a user defined output over-current protection limit up to a maximum value of 62A per phase per loop. For example, with 2 phases, the OCP maximum would be 62A*2 phases = 124A. To set the OCP current threshold, the current handeling capability of the power stages, the inductor and the input supply should be considered.

The controller action in OCP is configurable as shown in Table 16.

TABLE 16: OCP & UVP MODE SELECTION

OCP/UVP Behavior Mode
Per phase OCP Threshold (0 to 62A)
Shutdown immediately (cycle power or enable to restart)
Hiccup 2X before Shutdown
Hiccup indefinitely

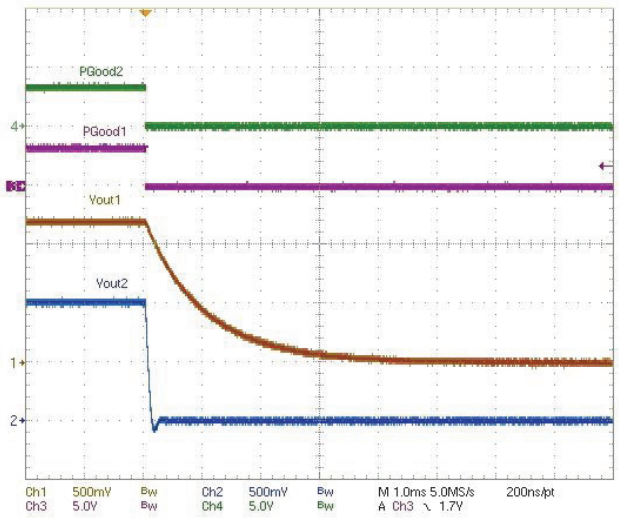


Figure 35: OCP on Loop #2 shuts down both loops

Slow Current Limit

In addition to the (fast) OCP, a Slow Current Limit can be programmed to monitor and protect against the long-term average current (Table 17). This allows the system designer to operate closer to the TDP level (thermal design power) of the system.

TABLE 17: SLOW OCP

MTP Register	Function
Slow_Imax = 0	Disabled
Slow_Imax = non-zero	Slow OCP range 2A to 62A per phase in 2A steps

The fast OCP threshold should be set reasonabely above the slow OCP threshold to prevent the instantaneous current spikes from tripping OCP. The fast OCP comparator has a 60kHz low-pass filter and the slow OCP comparator has a LPF with a programable band-width of 52Hz or 3.2Hz.

When the slow OCP is tripped, the VR will shut down based upon the OCP behavior set in Table 16.

Note that the slow OCP protection is disabled during start up and during VID transitions. In addition, depending on the revision of the the GUI, the current thresholds for OCP might be set per phase or per rail.

VR_HOT and Over Temperature Protection (OTP)

The IR36021 provides a temperature measurement capability at the TSEN pin that is used for over temperature protection, VR_HOT flag and temperature monitoring on loop one. The temperature is measured with an NTC network that can be positioned close to thermal hot spot. The thresholds are programmable in 1°C increments as shown in Table 18. If the measured temperature exceeds the OTP threshold, the IR36021 will latch off the VR (cycle system power or ENABLE to restart).

TABLE 18: VR_HOT & OTP

Function
VR_HOT polarity
VR_HOT threshold (64°C to 127°C)
OTP threshold (VR_HOT + 0°C to 32°C) max 134°C

The IR36021 includes a pre-programmed look-up table that is optimized for the recommended NTC options shown in Table 19. The NTC network is connected to the TSEN pin as shown in Figure 36. A 0.01uF capacitor is recommended to filter noise.

TABLE 19: NTC TEMPERATURE SENSE RANGE

NTC	Value	$R_{parallel}$
Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J	47KΩ	13KΩ

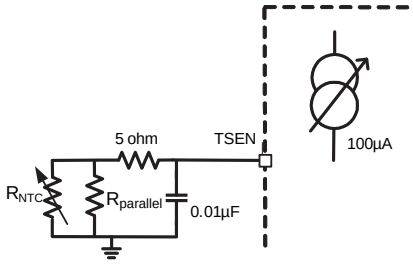


Figure 36: Temperature Sense NTC Network

Icritical Flag

The IR36021 VR_HOT_ICRIT pin can be optionally programmed to assert when a user programmable output current level is exceeded. The assertion is not a fault and the VR continues to regulate. I_CRITICAL monitors a long term averaged output current which is a useful indicator of average operating current and thermal operation. The user can select between two I_CRITICAL filters bandwidths, which is called telemetry-BW. Telemetry-BW affects other readings/measurements like: slow-OCP, Vin/Vout reading, and temperature measurement. (Table 20).

TABLE 20: TELEMETRY BAND-WIDTH

52Hz / Slow
3.2Hz / Very Slow

Refer to electrical table for Iout filter values

I_CRITICAL has a 5% hysteresis level and the VR_HOT_ICRIT pin will de-assert when the average output current level drops below 95% of the programmed current level threshold.

Pin Critical Flag

Additionally the IR36021 can be programmed to assert VR_HOT_ICRIT pin when a user programmable input power level is exceeded. The assertion is not a fault and the VR continues to regulate. PIN_CRITICAL monitors a long term average input power as calculated from the output current. The equation below shows the calculation performed by the IC to determine the average input power.

$$P_{IN} = \frac{Iout \cdot D}{\eta} V_{IN}$$

Where D is the duty cycle and η is the efficiency (fixed at 85%).

The PIN_CRITICAL power level can be programmed in MTP in 4W steps up to 252W, and if set (must be >4W), is wired OR'd into the VR_HOT_ICRIT pin. PIN_CRITICAL has a fixed 4W hysteresis level and the VR_HOT_ICRIT pin will de-assert when the power level drops 4W below the programmed input power level threshold.

VR_HOT_ICRIT Pin Functionality Options

The functionality of the VR_HOT_ICRIT pin can be set to assert when levels of Temp_max, Icc_max, and/or OCP levels are exceeded. Table 21 shows the multiple configurations of the VR_HOT_ICRIT pin.

TABLE 21: VR_HOT_ICRIT PIN OPTIONS

Temp_max Only
Temp_max or Icc_max
Temp_max or OCP
Icc_max Only

Input Over-voltage Protection

IR36021 monitors the input voltage (12V main power supply) via VINSEN pin. If input under-voltage protections is enabled, the VINSEN pin is compared to a fixed threshold and the IC will shut down if the threshold is exceeded(Table 22).

TABLE 22: INPUT OVER-VOLTAGE OPTIONS

	Threshold with 14:1 divider	Threshold with 22:1 divider
disabled	-	-
enabled	14.5V	23.5V

I2C/PMBUS COMMUNICATION

The IR36021 simultaneously supports I2C and PMBus through the use of exclusive addressing. The I2C and PMBus address for the IR36021 is programmed by MTP bits (I2C_Addr<6:0>) in Table 23, and (PMBus_Addr<3:0>) in Table 24. This means that a motherboard PMBus master may communicate with typically up to 8 dual loops, or if used as single loop controllers, as many as 16 IR36021-based VRs. Optionally, a resistor offset can be enabled as shown in Tables 25 and 26 (note that a 0.01uF capacitor is required across the resistor per Figure 37). As an example, setting a base I2C address of 28h with a resistor offset of +15 sets the I2C address to 37h. Similarly setting a base PMBus address of 40h with a resistor offset of +15 sets the PMBus address to 77h. Note that a single I2C address operates both loops whereas Table 24 sets the PMBus address of Loop 1, while Loop 2 is offset higher by the *Chip_Addr_Offset* register which is defaulted to 1.

$$PMaddress_{Loop\ 2} = PMaddress_{Loop\ 1} + Chip\_Addr\_Offset$$

The IR36021 can also set the I2C address independently from the PMBus address. By using a 7-bit address the user can configure the device to any one of 127 different I2C addresses. Note that I2C address 00h is not allowed. This is an I2C broadcast address. Setting the I2C address to 00h forces the I2C address to follow the PMBus address per Table 24.

Once the address of the IR36021 is set, it is locked to protect it from being overridden.

For unprogrammed devices, the I2C/PMBus address can be temporarily forced to address 0Ah for I2C and 0Dh for PMBus by setting EN=VR_HOT=low.

TABLE 23: I2C ADDRESSING

Register Setting I2C_Addr<6:0>	Controller I2C 7-bit Address
I2C_Addr<6:0> is non-zero*	I2C_addr<6:0>
Test mode (EN=VR_HOT=low)	0A hex

** Note Address 00h is not allowed. This is the I2C Broadcast Address.*

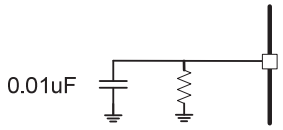


Figure 37: ADDR_PROT Pin Components

TABLE 24: PMBUS ADDRESSING

Register Setting PM_Addr<3:0>	Calculated 8-bit address code	PMBus 7-bit Address (Loop1)	I2C 7-bit address when tied to PMBus[1]
1111	1110 1110	77 hex	37 hex
1110	1110 1100	76 hex	36 hex
1101	1110 1010	75 hex	35 hex
1100	1110 1000	74 hex	34 hex
1011	1110 0110	73 hex	33 hex
1010	1110 0100	72 hex	32 hex
1001	1110 0010	71 hex	31 hex
1000	1110 0000	70 hex	30 hex
0111	1000 1110	47 hex	2F hex
0110	1000 1100	46 hex	2E hex
0101	1000 1010	45 hex	2D hex
0100	1000 1000	44 hex	2C hex
0011	1000 0110	43 hex	2B hex
0010	1000 0100	42 hex	2A hex
0001	1000 0010	41 hex	29 hex
0000	1000 0000	40 hex	28 hex
EN=VR_HOT=low	0001 1010	0D hex	0A hex

[1]: This I2C address only takes effect if Register 0x12[6:0] =0000000

TABLE 25: I2C OFFSET OPTIONS

Enable_I2C Addr_Offset MTP bit	I2C Address Offset
0	disabled
1	enabled

REAL-TIME I2C MONITORING FUNCTIONS

IR36021 provides real-time accurate measurement of input voltage, input current, output voltage, output current and temperature over the I2C interface. Output voltage is calculated based upon the VID setting and loadline and the result is reported through the I2C.

TABLE 26: ADDR_PROT RESISTOR OFFSET

ADDR_PROT Resistor	I2C Address Offset
0.845kΩ	+0
1.30kΩ	+1
1.78kΩ	+2
2.32kΩ	+3
2.87kΩ	+4
3.48kΩ	+5
4.12kΩ	+6
4.75kΩ	+7
5.49kΩ	+8
6.19kΩ	+9
6.98kΩ	+10
7.87kΩ	+11
8.87kΩ	+12
10.00kΩ	+13
11.00kΩ	+14
12.10kΩ	+15

**Note: Extends the range of PMBus addresses.*

Accuracy Optimization Registers

The IR36021 provides excellent factory-trimmed chip accuracy. In addition, the designer has calibration capability that can be used to optimize accuracy for a given design with minimum component changes. Once a design has been optimized the IR36021 will provide excellent repeatability from board to board. The IR36021 also provides the capability for individual board calibration and programming in production for the best accuracy. Table 27 shows the MTP registers used to fine tune the accuracy of the reported measurements. Figures 38 to 40 show the typical accuracy of the output current, input voltage and output voltage measurements using the IR36021.

TABLE 27: ACCURACY OPTIMIZATION REGISTERS

NVM Register	Function
IIN Fixed Offset	Offsets the input current in 1/32A steps e.g. driver Icc which can be 5-8mA per driver
IIN Per Phase Offset	Offsets the input current dependent upon the number of active phases in 1/128A steps e.g. the drive current for the MOSFET"s. This current increases every time a new phase is added
IOUT Current Offset	Offsets the output current from -8A to +7.5A in 0.5A steps (loop 1) and -4A to +3.75A 0.25A steps (loop 2)
Vout Offset	Offsets the output voltage +40mV to -35mV in 5mV steps.
Temperature Offset	Offsets the temperature in 1°C steps e.g. to compensate for offset between the hottest component and the NTC sensing location.

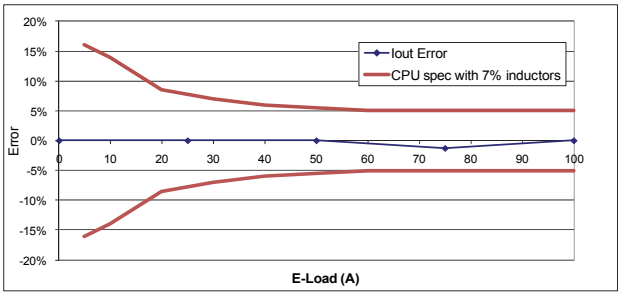


Figure 38: I2C I_{OUT} Error using 10% DCR inductors

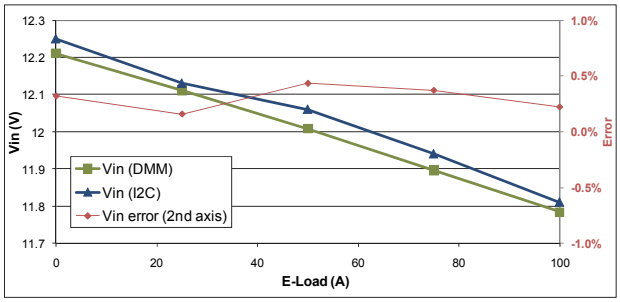


Figure 39: I2C Input Voltage Measurements

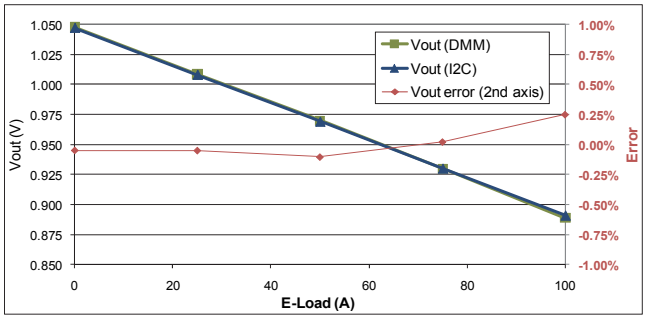


Figure 40: I2C Output Voltage Measurements

I2C SECURITY

The IR36021 provides robust and flexible security options to meet a wide variety of customer applications. A combination of hardware pin and software password prevents accidental overwrites, discourages hackers, and secures custom configurations and operating data. The Read and Write Security Zones can be in set in MTP (Tables 28 and 29) with the protection methods shown in Table 30.

TABLE 28: READ SECURITY ZONES

Zone	Access when	
	Locked	Unlocked
Open	All	All
Configuration	Control & Telemetry	All
Telemetry	Telemetry	All
Secure	None	All

TABLE 29: WRITE SECURITY ZONES

Zone	Access when	
	Locked	Unlocked
Open	All	All
Configuration	Control & Telemetry	All
Secure	None	All

TABLE 30: READ OR WRITE UNLOCK OPTIONS

Password Only
Pin Only
Pin & Password
Lock Forever

Password Protection

The system designer can set any 16-bit password (other than 00h) and this is stored in MTP (Table 31). To unlock, a user must write the correct password into the "Password Try" register which is a volatile read/write register. To lock, write an incorrect password into the "Password Try" register. After a certain number of incorrect tries, the IC will lock up to prevent unauthorized access.

TABLE 31: PASSWORD REGISTERS

Register	Length	Location
Password	16 bit (2 bytes)	MTP
Try	16 bit (2 bytes)	R/W

The following pseudo-code illustrates how to change a password:

 # first unlock the IC
Write old password high Byte to R/W high Byte Try register
Write old password low Byte to R/W low Byte Try register
 # now write new password into MTP
Write new password high Byte to high Byte MTP register
 # password has changed! Must unlock to change the low byte
Write new password high Byte to R/W high Byte Try register
Write new password low Byte to low Byte MTP register
 # password change complete, status is locked
#Need to write new low byte to Try register to unlock

Pin Protection

The ADDR_PROT pin is a dual function pin. When the IC is enabled, the resistor value is latched and stored for use in the I2C address offset function. Thereafter, the pin acts entirely as a PROTECT pin. If enabled, the PROTECT pin must be driven high to unlock and low to lock. Note, if the resistor address offset function is being used, care must be taken to allow the IC to read the resistor value before driving the pin high or low to set the security state otherwise an erroneous address offset value may be latched in. The user should wait until at least the completion of the auto-trim time t_4 in Figure 8.

GAMER MODE & MARGINING

IR36021 supports a PMBus gamer command for flexible over-clocking over an extended VID range. System firmware can use this command to enable and disable "Gamer Mode". When Gamer mode is enabled, the output voltage transitions from the current value to the value specified by the Gamer command .

The Gamer VID is represented as a 9-bit word given by the formula:

$$V_{Gamer} = (VID + 1) \times Stepsize \quad for\ VID = 1\ to\ 460$$
$$V_{Gamer}MAX = 2.3V$$
$$where\ Stepsize = 5mV$$

The designer may also configure a maximum Vout (Table 32) to protect the VR from exceeding the programmed voltage regardless of the commanded VID and offset. The Gamer command may be used to set the controller to either override or track the current VID (set by manual_VID registers). In Override mode, the IR36021 sets the output voltage defined by the Gamer VID and ignores the manual_VID registers. In Track mode, the output voltage is initially set to the Gamer VID and any subsequent changes to the manual_VID registers cause the same offset changes in the Gamer VID.

The IR36021 Gamer command also provides overclockers the ability to minimize droop by digitally scaling the loadline to 80%, 60% or 0% (disable) of the nominal value. A summary of the PMBus Gamer command is shown in Table 33.

Note that sending a Gamer command does not change the output voltage when the device is in margining mode. The command will take effect when the device comes out of margining mode.

TABLE 32: OVERCLOCK VMAX

Register Value	Vmax
0	0.645
1	0.765
2	0.885
3	1.005
4	1.125
5	1.245
6	1.365
7	1.485
8	1.605
9	1.725
10	1.845
11	1.965
12	2.085
13	2.205
14	2.325
15	2.445

TABLE 33: GAMER COMMAND FORMAT

Bits	Function
15-13	Reserved. Always set to “001”b
12	Gamer Mode Enable/Disable
11	VID Follow or VID Override Mode
10:9	Loadline scale 100%, 80%, 60%, 0%
8:0	Gamer VID[8:0]

Overclock Mode Recovery

Raising the CPU voltage to achieve higher performance or lowering the CPU voltage to save power can result in a system crash. The IR36021 contains a safety mechanism whereby the Overclock Mode is immediately disabled any time the ENABLE pin is driven low (typically by a system restart). This ensures that the CPU starts at the proper boot VID.

I2C PROTOCOLS

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 41 shows the I2C format employed by the IR36021.

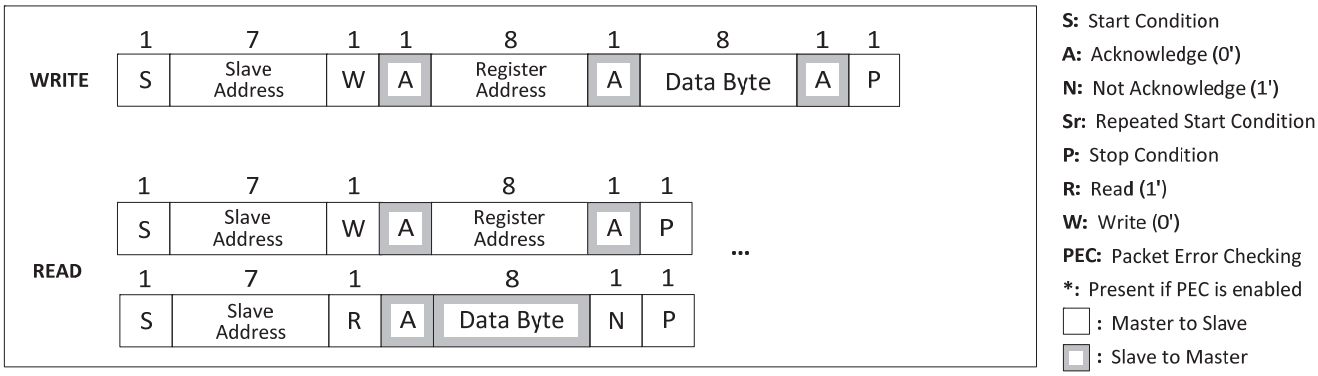


Figure 41: I2C Format

SMBUS/PMBUS PROTOCOLS

To access IR's configuration and monitoring registers, 4 different protocols are required:

- the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the SMBus Block Read protocol for accessing Model and Revision information
- the SMBus Process call (for accessing Configuration Registers)

An explanation of which command codes and protocols are required to access them is given in Table 34.
In addition, the IR36021 supports:

- Alert Response Address (ARA)
- Bus timeout (10ms)
- Group Command for writing to many VRs within one command

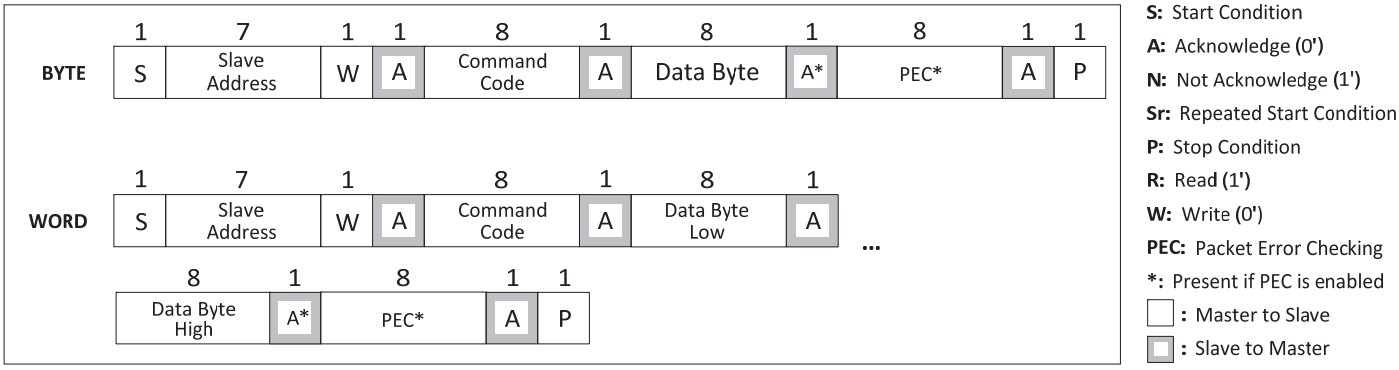


Figure 42: SMBus Write Byte/Word

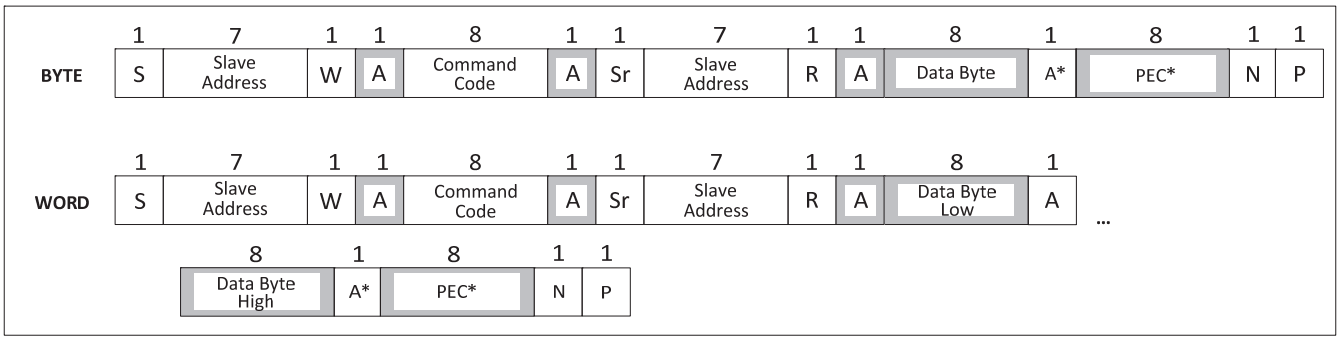


Figure 43: SMBus Read Byte/Word

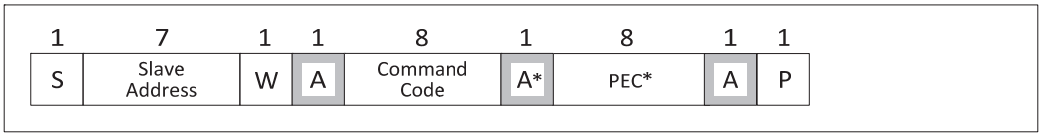


Figure 44: SMBus Send Byte

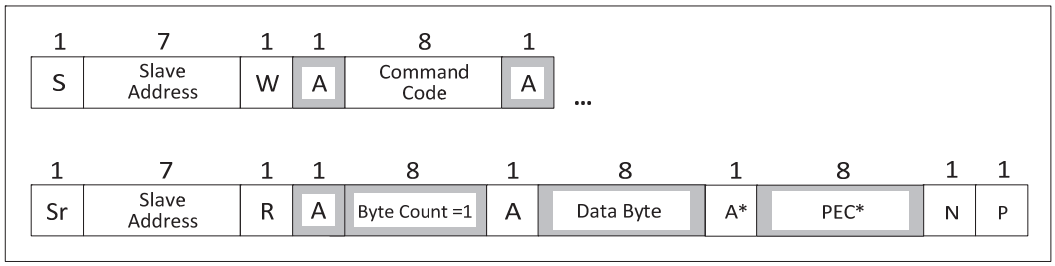


Figure 45: SMBus Block Read with Byte Count=1

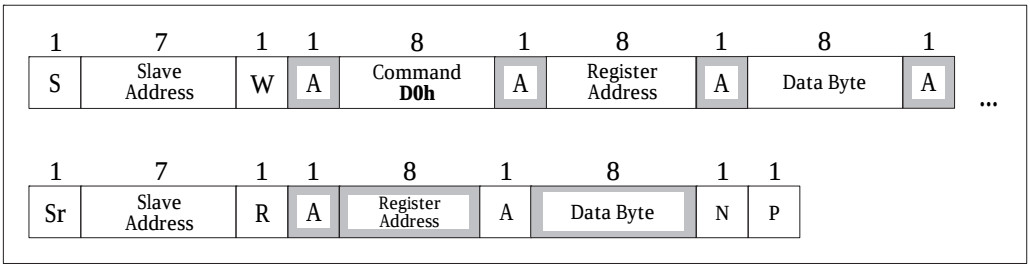


Figure 46: SMBus Process Call to Write an IR Register

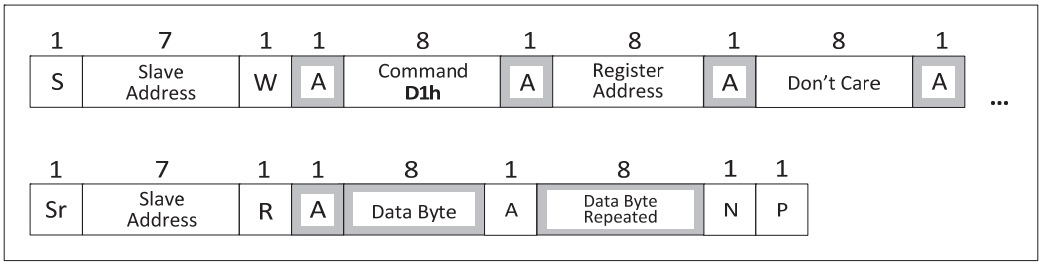


Figure 47: SMBus Process Call to Read an IR Register

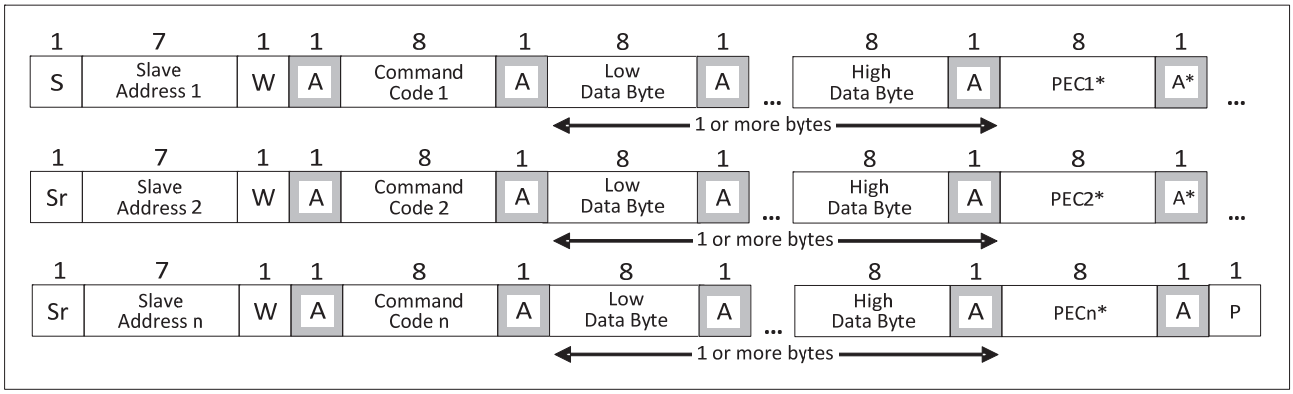


Figure 48: Group Command

TABLE 34: PMBUS COMMANDS

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
OPERATION	Read/Write Byte	01h	Enables or disables IR36021 output and controls margining
CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers
CAPABILITY	Read Byte	19h	Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz
VOUT_MODE	Read/Write Byte	20h	Sets the VOUT format to Linear Mode for the READ_VOUT, VOUT_MARGIN_LOW, VOUT_MARGIN_HIGH commands The default is LINEAR mode with exponent -9. LINEAR Mode: exponent of 1 to -16 is supported
VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the high voltage when commanded by OPERATION. Works in conjunction with VOUT_MODE.
VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the low voltage when commanded by OPERATION. Works in conjunction with VOUT_MODE.
STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> device busy fault Bit <6> output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: Reserved
STATUS_WORD	Read Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are:

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> Reserved Bit <3> Loop is not ready Bit <2:0> Reserved
STATUS_TEMPERATURE	Read/Write Byte	7Dh	Returns Over Temperature warning (VR_HOT level) and Over Temperature fault (OTP level). Does not report under temperature warning/fault. The bit meanings are: Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5> Under Temperature Warning Bit <4> Under Temperature Fault Bit <3:0> Reserved
STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Command not Supported Bit <6> Reserved Bit <5> PEC fault Bit <4:0> Reserved
STATUS_MFR_SPECIFIC	Read/Write Byte	80h	Returns 1 byte where the bit meanings are: Bit <7:1> Reserved Bit <0> Phase Fault
READ_VIN	Read Word	88h	Returns the input voltage in Volts1
READ_IIN	Read Word	89h	Returns the input current in Amperes1
READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
READ_IOUT	Read Word	8Ch	Returns the output current in Amperes 1
READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop NTC temperature in degrees Celsius 1
READ_TEMPERATURE_2	Read Word	8Eh	Returns the other loop NTC temperature in degrees Celsius 1
READ_POUT	Read Word	96h	Returns the output power in Watts1
READ_PIN	Read Word	97h	Returns the input power in Watts1
PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft)
MFR_MODEL	Block Read, byte count = 2	9Ah	Returns a 2 byte code with the following values: Low Byte always = 01h High Byte is: 2Dh = IR36021

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
MFR_REVISION	Block Read, byte count = 2	9Bh	Returns a 2 byte code with the following values: Low Byte always = 01h High Byte is the revision number in hex.
WRITE_REGISTER_PROCESS_CALL	Process Call	D0h	Write to configuration registers
READ_REGISTER_PROCESS_CALL	Process Call	D1h	Read from configuration & status registers
GAMER COMMAND	Write Word	D2h	Enables/disables Gamer Mode and associated options
SET_POINTER	Write Byte	D3h	Sets the register address for reading/writing
GET_POINTER	Read Byte	D4h	Reads 1 byte from the previously set register address
WRITE_REGISTER	Write Word	D5h	Writes 1 byte to the previously set register address
SET_I2C	Read/Write Byte	D6h	Sets the 7-bit I2C address according to the bit meanings: Bit <7> Enable I2C Bus (0 – Disable, 1 – Enable) Bit<6:0> 7-bit I2C address
READ_EFFICIENCY	Read Word	D7h	Reports the efficiency in %1
MASK_STATUS_WORD	Read/Write Word	D8h	Masks STATUS_WORD bits.
MASK_TEMPERATURE	Read/Write Byte	D9h	Masks STATUS_TEMPERATURE
MASK_CML	Read/Write Byte	Dah	Masks STATUS_CML
MASK_MANUFACTURER	Read/Write Byte	DBh	Masks STATUS_MFR_SPECIFIC

Note[1] – PMBus: Linear Data Format is used

11-BIT LINEAR DATA FORMAT

Monitored parameters use the Linear Data Format (Figure 49) encoding into 1 Word (2 bytes), where:

$$Value = Y \times 2^{N}$$

Note N and Y are "signed" values. If, VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

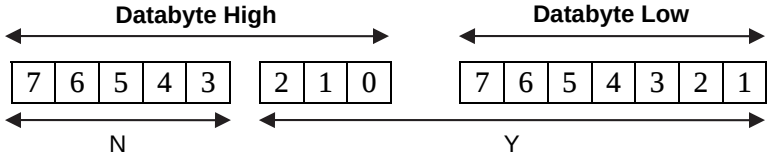


Figure 49: 11-bit Linear Data Format

16-BIT LINEAR DATA FORMAT

This format is only used for VOUT related commands (READ_VOUT, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW):

$$Value = Y \times 2^{N}$$

Note N and Y are "signed" values. If, VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

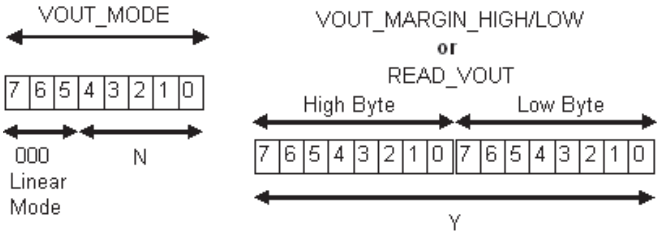
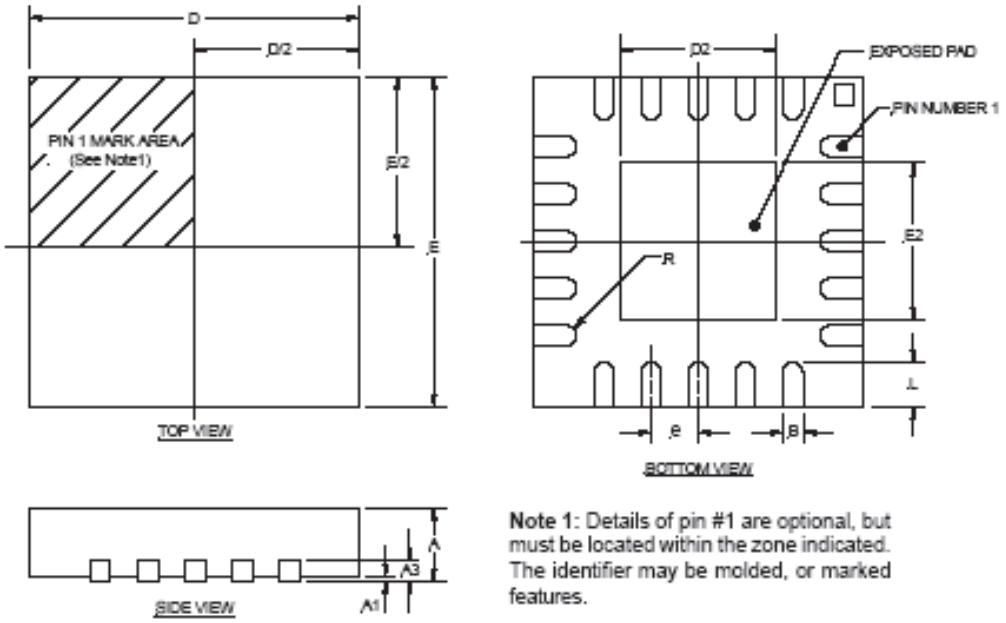


Figure 50: 16-bit Linear Data Format

QFN Package; 5x5-32 Lead



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	32-PIN 5x5		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		5.00 BSC	
D2	3.30	3.45	3.55
E		5.00 BSC	
E2	3.30	3.45	3.55
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

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