

ON Semiconductor®

NC7SZ175 TinyLogic® UHS D-Type Flip-Flop with Asynchronous Clear

General Description

The NC7SZ175 is a single positive edge-triggered D-type CMOS Flip-Flop with Asynchronous Clear from ON Semiconductor's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power

dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. This single flip-flop will store the state of the D input that meets the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. A LOW input to Clear sets the Q output to LOW level. The Clear input is independent of clock.

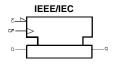
Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- \blacksquare Matches the performance of LCX when operated at 3.3V $\rm V_{CC}$
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Proprietary noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ175P6X	MAA06A	Z75	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ175L6X	MAC06A	C4	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol



Function Table

	Output		
СР	D	Q	
\	L	Н	L
~	Н	Н	Н
~	Χ	Н	Qn
X	Х	L	L

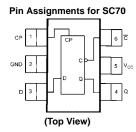
H = HIGH Logic Level L = LOW Logic Level

Qn = No change in data X = Immaterial

Pin Descriptions

Pin Names	Description
D	Data Input
CP	Clock Pulse Input
C	Clear Input
Q	Flip-Flop Output

Connection Diagrams



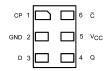
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings(Note 1)

DC Input Diode Current (I_{IK})

V_{IN} < 0V

DC Output Diode Current (I_{OK})

V_{OUT} < 0V

DC Output (I_{OUT}) Source/Sink Current ± 50 mA DC V_{CC}/GND Current (I_{CC}/I_{GND}) ± 50 mA Storage Temperature Range (T_{STG}) -65° C to +150 $^{\circ}$ C Junction Temperature under Bias (T_{J}) 150° C

Junction Lead Temperature (T_L)

 $\begin{tabular}{ll} \mbox{(Soldering, 10 seconds)} & 260^{\circ}\mbox{C} \\ \mbox{Power Dissipation (P_D) @+85°$C} & 180 \mbox{ mW} \\ \end{tabular}$

Recommended Operating Conditions (Note 2)

Power Supply

for actual device operation.

-50 mA

-50 mA

 $\begin{array}{lll} \text{Operating (V}_{\text{CC}}) & 1.65\text{V to } 5.5\text{V} \\ \text{Data Retention} & 1.5\text{V to } 5.5\text{V} \\ \text{Input Voltage (V}_{\text{IN}}) & 0\text{V to } 5.5\text{V} \\ \text{Output Voltage (V}_{\text{OUT}}) & 0\text{V to V}_{\text{CC}} \\ \text{Input Rise and Fall Time (t}_{\text{r}}, \, t_{\text{f}}) & \end{array}$

 $\begin{array}{lll} V_{CC} = 1.8 \text{V, } 2.5 \text{V} \pm 0.2 \text{V} & 0 \text{ to } 20 \text{ ns/V} \\ V_{CC} = 3.3 \text{V} \pm 0.3 \text{V} & 0 \text{ to } 10 \text{ ns/V} \\ V_{CC} = 5.5 \text{V} \pm 0.5 \text{V} & 0 \text{ to } 5 \text{ ns/V} \\ \text{Operating Temperature (T}_{A}) & -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C} \\ \text{Thermal Resistance (}\theta_{JA}\text{)} & 350 ^{\circ}\text{ C/W} \end{array}$

Note 1: The "Absolute Maximum Ratings": are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}		T _A = +25°)	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Unit	Conditions	
Syllibol	Parameter	(V)	Min	Тур	Max	Min	Max	Onn	Co	nuttions
V _{IH}	HIGH Level Control	1.65 to 1.95	0.75 V _{CC}			0.75 V _{CC}		V		
	Input Voltage	2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		V		
V _{IL}	LOW Level Control	1.65 to 1.95			0.25 V _{CC}		0.25 V _{CC}	V		
	Input Voltage	2.3 to 5.5			$0.3\mathrm{V}_{\mathrm{CC}}$		$0.3\mathrm{V}_{\mathrm{CC}}$	V		
V _{OH}	HIGH Level Control	1.65	1.55	1.65		1.55				
	Output Voltage	1.8	1.7	1.8		1.7				
		2.3	2.2	2.3		2.2				$I_{OH} = -100 \ \mu A$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V	$V_{IN} = V_{IH}$	
		1.65	1.24	1.52		1.29		v	or V_{IL}	$I_{OH} = -4 \text{ mA}$
		2.3	1.9	2.15		1.9				$I_{OH} = -8 \text{ mA}$
		3.0	2.4	2.8		2.4				$I_{OH} = -16 \text{ mA}$
		3.0	2.3	2.68		2.3				$I_{OH} = -24 \text{ mA}$
		4.5	3.8	4.2		3.8				$I_{OH} = -32 \text{ mA}$
V _{OL}	LOW Level Control	1.65		0.0	0.1		0.1			
	Output Voltage	1.8		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1			$I_{OL} = 100 \mu A$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IL}$	
		1.65		0.08	0.24		0.24	ľ	or V _{IH}	I _{OL} = 4 mA
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4			$I_{OL} = 16 \text{ mA}$
		3.0		0.22	0.55		0.55			$I_{OL} = 24 \text{ mA}$
		4.5		0.22	0.55		0.55			$I_{OL} = 32 \text{ mA}$
I _{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5$	5.5V
I _{OFF}	Power Off Leakage Current	0.0			1.0		10	μΑ	V _{IN} or V _{OL}	_{JT} = 5.5V
Icc	Quiescent Supply Current	1.65 to 5.5			1.0		10.0	μΑ	$V_{IN} = 5.5V$, GND

AC Electrical Characteristics

Symbol	Parameter	V _{CC}		T _A = +25°	С	T _A = -40°	C to +85°C	Units	Conditions	Figure Number
Symbol	Farameter	(V)	Min	Тур	Max	Min	Max	Oilles		
f _{MAX}	Maximum Clock	1.65				100				
	Frequency	1.8				100				
		2.5 ± 0.2				125		MHz	C _L = 50 pF	Figures 1, 4
		3.3 ± 0.3				150			$R_L = 500 \Omega$., .
		5.0 ± 0.5				175				
t _{PLH}	Propagation Delay	1.65	2.5	9.8	15.0	2.5	16.5			
t _{PHL}	CP to Q	1.8	2.5	6.5	10.0	2.5	11.0			
		2.5 ± 0.2	2.0	3.8	6.5	2.0	7.0		C _L = 15 pF	Figures 1, 3
		3.3 ± 0.3	1.5	2.8	4.5	1.4	5.0	ns	$R_L = 1 \ M\Omega$	1,0
		5.0 ± 0.5	1.0	2.2	3.5	1.0	3.8			
		3.3 ± 0.3	2.0	3.4	5.5	1.6	6.2		C _L = 50 pF	Figures
		5.0 ± 0.5	1.5	2.6	4.0	1.4	4.7		$R_L = 500 \Omega$	1, 3
t _{PHL}	Propagation Delay	1.65	2.5	9.8	13.5	2.5	15.0			
	C to Q	1.8	2.5	6.5	9.0	2.5	10.0			
		2.5 ± 0.2	2.0	3.8	6.0	2.0	6.4		C _L = 15 pF	Figures 1, 3
		3.3 ± 0.3	1.5	2.8	4.3	1.2	4.6	ns	$R_L = 1 M\Omega$	1, 5
		5.0 ± 0.5	1.5	2.2	3.2	1.0	3.5			
		3.3 ± 0.3	1.5	3.4	5.3	1.5	5.8		C _L = 50 pF	Figures
		5.0 ± 0.5	1.0	2.7	4.0	1.2	4.5		$R_L = 500 \Omega$	1, 3
t _S	Setup Time	2.5 ± 0.2				2.5			C _L = 50 pF	
	CP to D	3.3 ± 0.3				2.0		ns	$R_L = 500 \Omega$	Figures 1, 4
		5.0 ± 0.5				1.5				1, 4
t _H	Hold Time,	2.5 ± 0.2				1.5			C _L = 50 pF	
	CP to D	3.3 ± 0.3				1.5		ns	$R_L = 500 \Omega$	Figures 1, 4
		5.0 ± 0.5				1.5				1, 4
t _W	Pulse Width, CP	2.5 ± 0.2				3.0			C _L = 50 pF	
		3.3 ± 0.3				2.8		ns	$R_L = 500 \Omega$	Figures 1, 4
		5.0 ± 0.5				2.5				1, 4
	Pulse Width, C	2.5 ± 0.2				3.0			Clock HIGH or LOW	
	,	3.3 ± 0.3				2.8		ns	C _I = 50 pF	Figures
		5.0 ± 0.5				2.5			$R_1 = 500 \Omega$	1, 4
t _{rec}	Recovery Time,	2.5 ± 0.2				1.0			C _L = 50 pF	1
. 50	C to CP	3.3 ± 0.3				1.0		ns	$R_L = 500 \Omega$	Figures
		5.0 ± 0.5				1.0		ĺ	-	1, 4

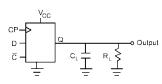
Capacitance (Note 3)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Input Capacitance	3		pF	V _{CC} = Open, V _{IN} = 0V or V _{CC}
C _{OUT}	Output Capacitance	4		pF	$V_{CC} = 3.3V$, $V_{IN} = 0V$ or V_{CC}
C _{PD}	Power Dissipation Capacitance	10		pF	V _{CC} = 3.3V
	(Note 4)	12		Pi	V _{CC} = 5.0V

Note 3: T_A = +25C, f = 1MHz.

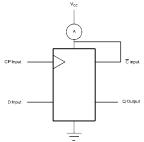
Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}$ static).

AC Loading and Waveforms



 ${
m C_L}$ includes load and stray capacitance Input PRR = 1.0 MHz, ${
m t_W}$ = 500 ns

FIGURE 1. AC Test Circuit



CP Input = AC Waveform; $t_r = t_f = 1.8$ ns; CP Input PRR = 10 MHz; Duty Cycle = 50% D Input PRR = 5MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

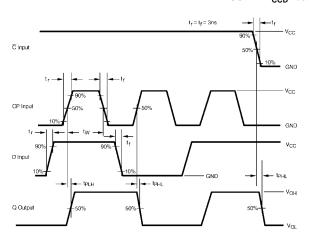


FIGURE 3. AC Waveforms

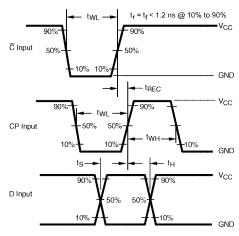


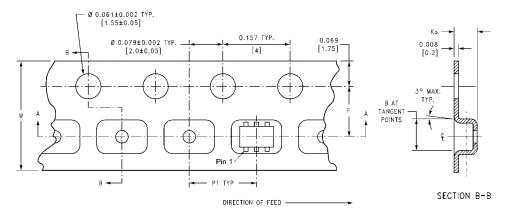
FIGURE 4. AC Waveforms

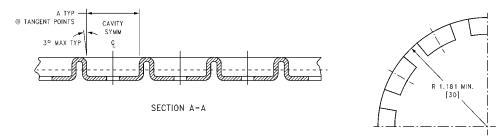
Tape and Reel Specification

TAPE FORMAT for SC70

AFE FORMAL IOLS	C/0			
Package	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
P6X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

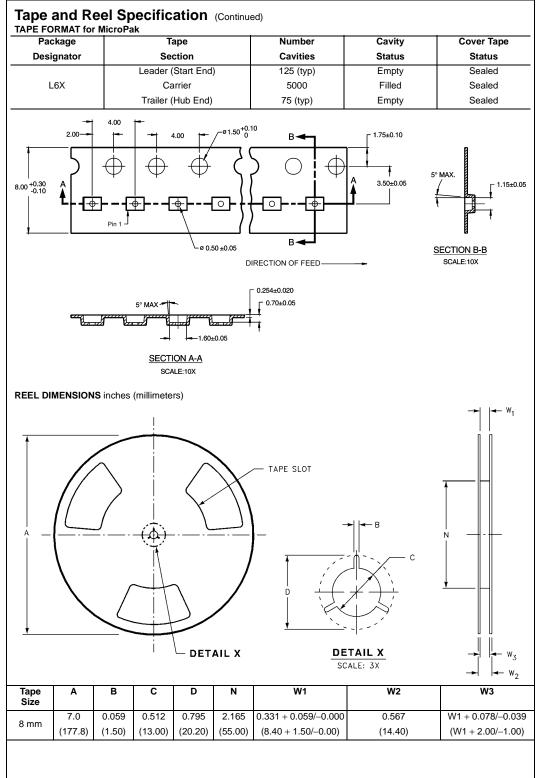
TAPE DIMENSIONS inches (millimeters)





BEND RADIUS NOT TO SCALE

Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
		(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)

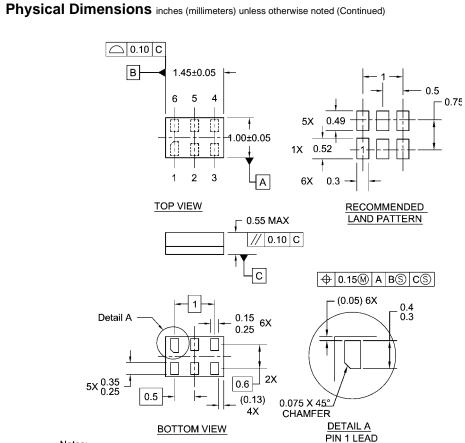


Physical Dimensions inches (millimeters) unless otherwise noted 0.65 B 1.25±0.10 2.10±0.10 0.20 +0.10 LAND PATTERN RECOMMENDATION ◆ max 0.1 **②** SEE DETAIL A 0.9±.10 0.95±0.15 max 0.1 R0.14 GAGE PLANE R0.10 0.20 0.45 0.10 -- 0.425 NOMINAL DETAIL A NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

6-Lead SC70, EIAJ SC88, 1.25mm Wide Package Number MAA06A

MAA06ARevC



Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
- DIMENSIONS ARE IN MILLIMETERS
 DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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