

MC74HC540A

Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

The MC74HC540A is identical in pinout to the LS540. The device inputs are compatible with Standard CMOS outputs. External pull-up resistors make them compatible with LSTTL outputs.

The HC540A is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC540A is similar in function to the HC541A, which has noninverting outputs.

Features

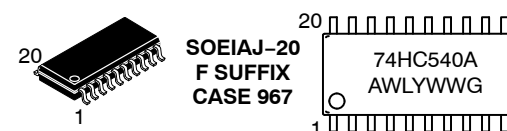
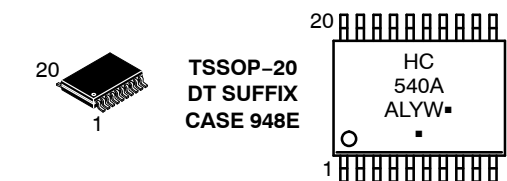
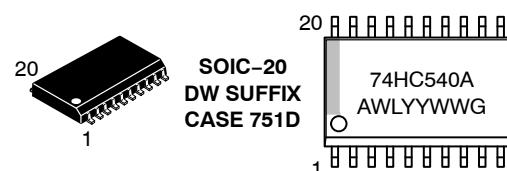
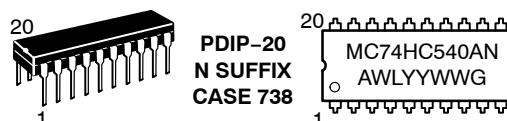
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC540A

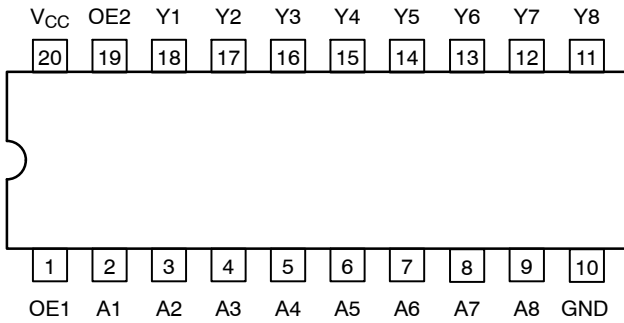


Figure 1. Pinout: 20-Lead Packages (Top View)

FUNCTION TABLE

| Inputs | | | Output Y |
|--------|-----|---|----------|
| OE1 | OE2 | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

Z = High Impedance

X = Don't Care

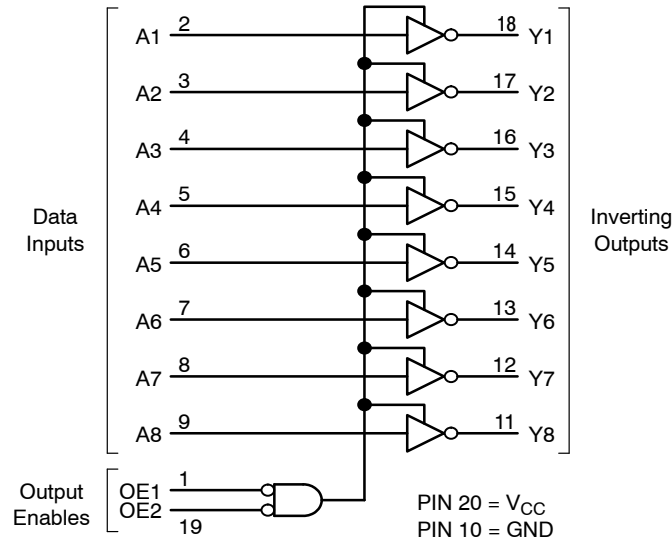


Figure 2. Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|---------------------------|------------------|
| MC74HC540ANG | PDIP-20 (Pb-Free) | 18 Units / Rail |
| MC74HC540ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC540ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC540ADTR2G | TSSOP-20* | 2500 Tape & Reel |
| MC74HC540AFG | SOEIAJ-20 (Pb-Free) | 40 Units / Rail |
| MC74HC540AFELG | SOEIAJ-20 (Pb-Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74HC540A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|---|--|------------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _I | DC Input Voltage | -0.5 to V _{CC} +0.5 | V |
| V _O | DC Output Voltage (Note 1) | -0.5 ≤ V _O ≤ V _{CC} +0.5 | V |
| I _{IK} | DC Input Diode Current | ±20 | mA |
| I _{OK} | DC Output Diode Current | ±35 | mA |
| I _O | DC Output Sink Current | ±35 | mA |
| I _{CC} | DC Supply Current per Supply Pin | ±75 | mA |
| I _{GND} | DC Ground Current per Ground Pin | ±75 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | +150 | °C |
| θ _{JA} | Thermal Resistance | PDIP SOIC TSSOP 67 96 128 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C | PDIP SOIC TSSOP 750 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating | Oxygen Index: 30% - 35% UL 94 V0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) >2000 >200 >1000 | V |
| I _{LATCHUP} | Latchup Performance | Above V _{CC} and Below GND at 85°C (Note 5) | ±300 mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|--|--------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 3) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V 0 0 0 | 1000 500 400 | ns |

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

MC74HC540A

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IL} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4 | 40 | 160 | μA |

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|--|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 3 and 5) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 18 | 23 | 28 | |
| | | 6.0 | 15 | 20 | 25 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 3 and 5) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 22 | 28 | 34 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| C _{out} | Maximum 3-State Output Capacitance (Output in High Impedance State) | | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Buffer) (Note 7) | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | | | pF | |
| | | 35 | | | | |

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC540A

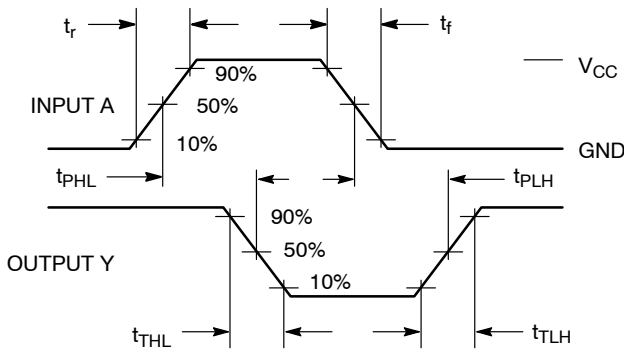


Figure 3. Switching Waveform

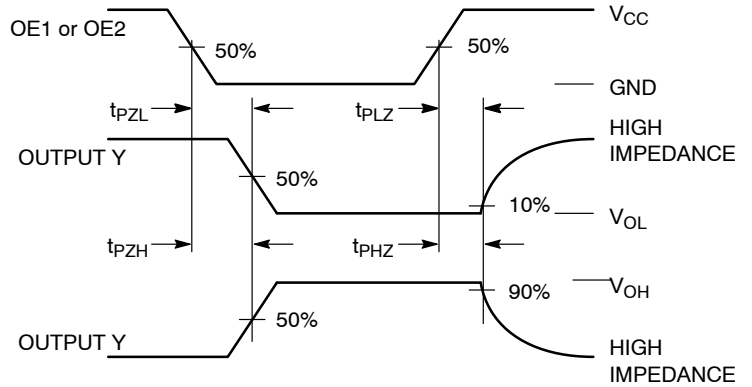
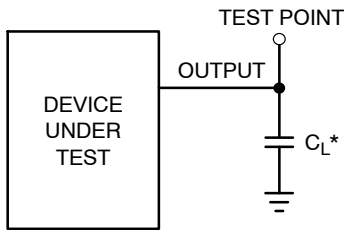
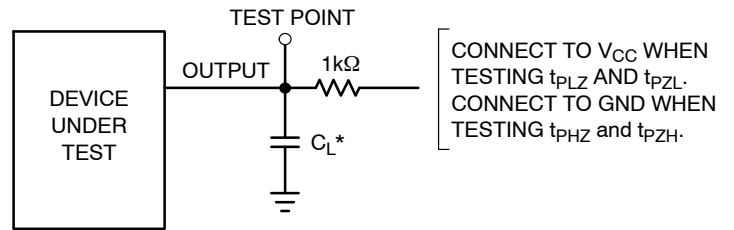


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

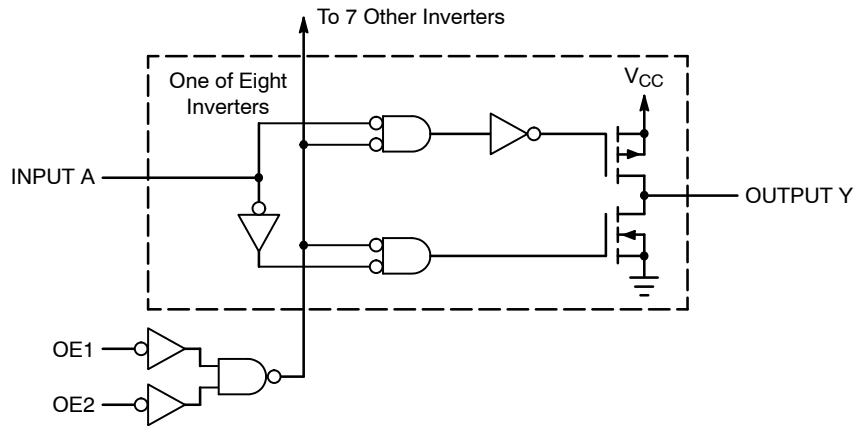


Figure 7. Logic Detail

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)

Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

OE1, OE2 (PINS 1, 19)

Output enables (active-low). When a low voltage is applied to both of these pins, the outputs are enabled and the

device functions as an inverter. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

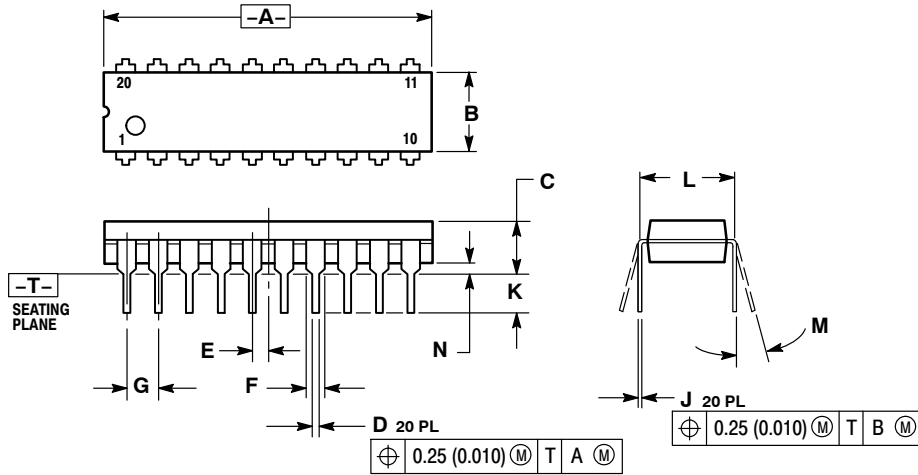
Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)

Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high-impedance outputs.

MC74HC540A

PACKAGE DIMENSIONS

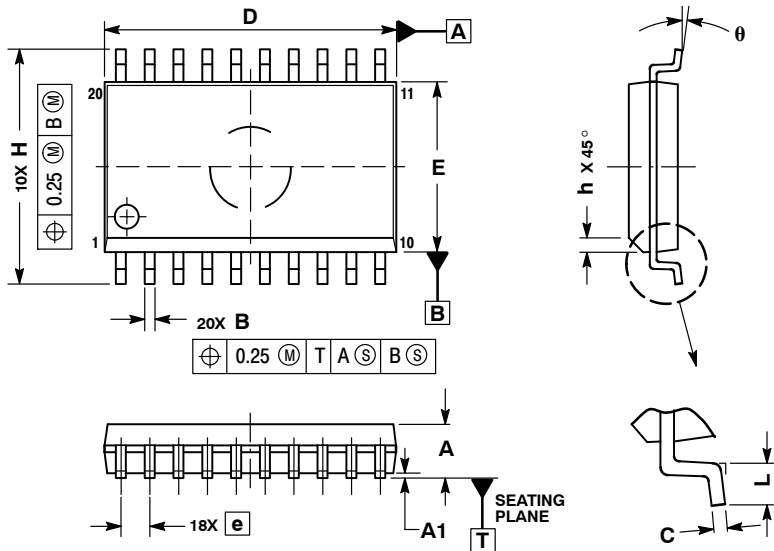
PDIP-20
N SUFFIX
 PLASTIC DIP PACKAGE
 CASE 738-03
 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-20
DW SUFFIX
 CASE 751D-05
 ISSUE G



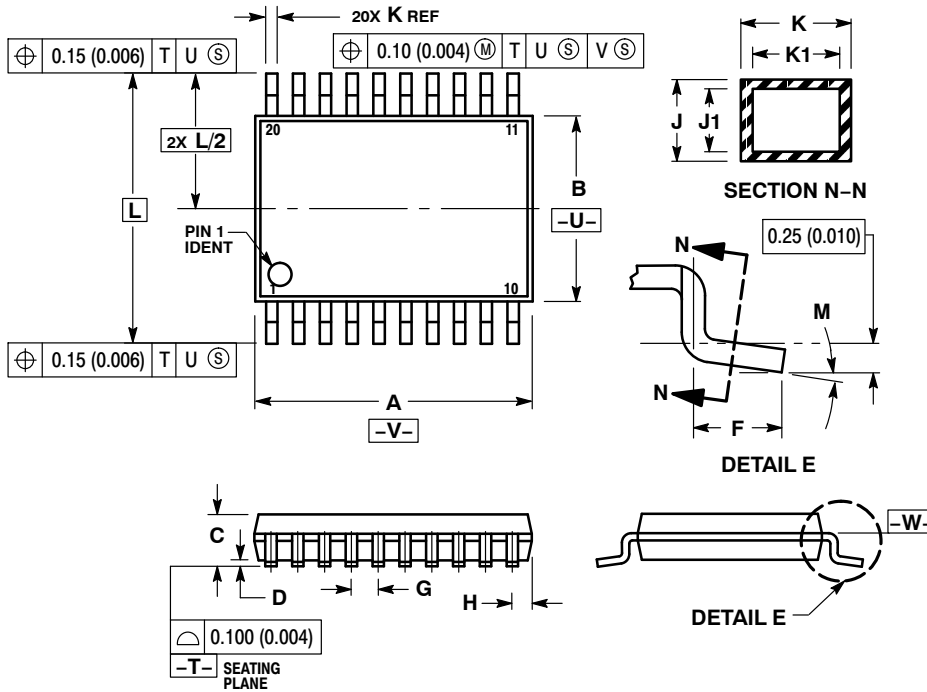
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

MC74HC540A

PACKAGE DIMENSIONS

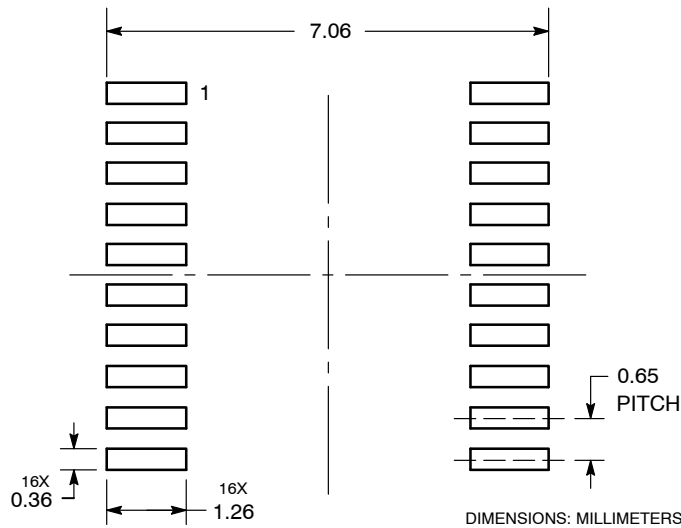
TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

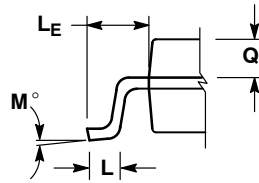
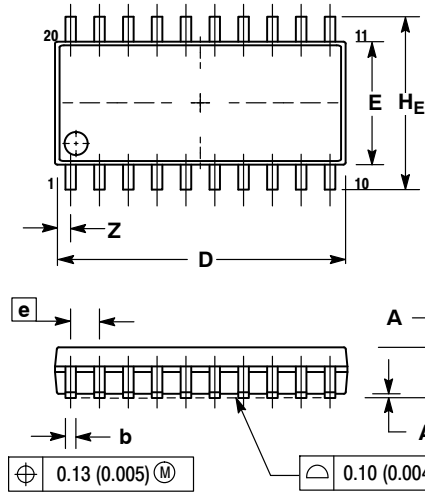
SOLDERING FOOTPRINT



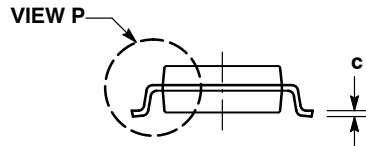
MC74HC540A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967-01
ISSUE A



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[MC74HC540ADTR2](#) [MC74HC540ADW](#) [MC74HC540ADWR2](#) [MC74HC540AF](#) [MC74HC540AFEL](#) [MC74HC540AN](#)
[MC74HC540ANG](#)