1.5K-Bit Serial EPROM with SDQ Interface

1 Features

- 1536 Bits of One-Time Programmable (OTP) EPROM For Storage Of User-Programmable Configuration Data
- Factory-Programmed Unique 64-Bit Identification Number
- Single-Wire Interface to Reduce Circuit Board Routing
- Synchronous Communication Reduces Host Interrupt Overhead
- 6KV IEC 61000-4-2 ESD Compliance on Data Pin
- No Standby Power Required
- Available in a 3-Pin SOT-23 and TO-92 Packages

2 Applications

- Security Encoding
- Inventory Tracking
- Product-Revision Maintenance
- Battery-Pack Identification

3 Description

The bq2026 is a 1.5K-bit serial EPROM containing a factory-programmed, unique 48-bit identification number, 8-bit family code, and a 64-bit status register.

The bq2026 SDQ™ interface requires only a single connection and a ground return. The SDQ pin is also the sole power source for the bq2026.

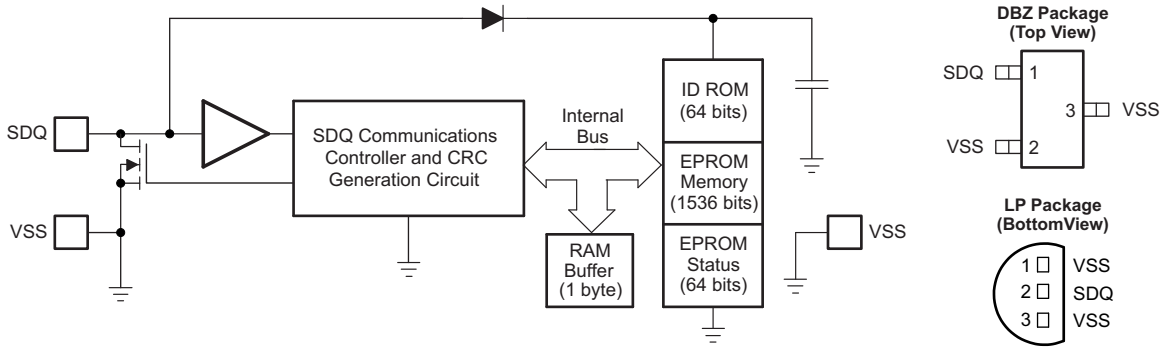
The small surface-mount package options saves printed-circuit-board space, while the low cost makes it ideal for applications such as battery-pack configuration parameters, record maintenance, asset tracking, product-revision status, and access-code security.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2026	SOT-23 (3)	4.30 mm × 4.30 mm
	TO-92 (3)	2.92 mm × 1.30 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Block Diagram



NOTE: Pin 3 for LP package can be ground or left unconnected.

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4 Revision History

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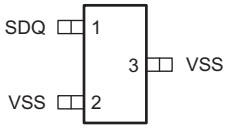
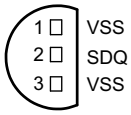
- Changed document format to latest data sheet standards ... 1
- Added Handling Rating table, Feature Description, Device Functional Modes, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections ... 1
- Added note to front page diagram ... 1
- Changed pin 3 (VSS) description for LP package ... 3

5 Pin Configuration and Functions

DBZ Package
SOT-23-3
(Top View)



LP Package
TO-92-3
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBZ	LP		
SDQ	1	2	I/O	Data
VSS	2, 3	1	—	Ground
VSS	—	3	—	Can be ground or left unconnected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
DC voltage applied to V_{PU} See Figure 1		–0.3	12.5	V
Low-level output current, I_{OL}			5	mA
ESD IEC 61000-4-2 Air discharge	SDQ to V_{SS}, V_{SS} to SDQ		6	kV
Operating free-air temperature range, T_A		–20	70	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–55	125	°C

6.3 Electrical Characteristics: DC

At T_A = –20°C to 70°C; $V_{PU(min)}$ = 2.65 V_{DC} to 5.5 V_{DC}, all voltages relative to VSS.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{SDQ}	Supply current	V_{PU} = 5.5 V			20	µA
V_{OL}	Low-level output voltage	Logic 0, V_{PU} = 5.5 V, I_{OL} = 4 mA, SDQ pin			0.4	V
		Logic 0, V_{PU} = 2.65 V, I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	Logic 1		V_{PU}	5.5	V
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V, SDQ pin			4	mA
V_{IL}	Low-level input voltage	Logic 0			0.8	V
V_{IH}	High-level input voltage	Logic 1	2.2			V
V_{PP}	Programming voltage		11.5		12	V
I_{lkg}	Input leakage			1.4		µA
C_I	Input capacitance			1.2		nF

6.4 Switching Characteristcs: AC

T_A = –20°C to 70°C; $V_{PU(min)}$ = 2.65 V_{DC} to 5.5 V_{DC}, all voltages relative to VSS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_c	Bit cycle time (1)		60		120	µs
t_{WSTRB}	Write start cycle (1)		1		15	µs
t_{WDSU}	Write data setup (1)		t_{WSTRB}		15	µs
t_{WDH}	Write data hold (1) (2)		60		t_c	µs
t_{rec}	Recovery time (1)		1			µs
t_{RSTRB}	Read start cycle (1)		1		13	µs
t_{ODD}	Output data delay (1)		t_{RSTRB}		13	µs
t_{ODHO}	Output data hold (1)		17		60	µs
t_{RST}	Reset time (1)		480			µs
t_{PPD}	Presence pulse delay (1)		15		64	µs
t_{PP}	Presence pulse (1)		60		240	µs
t_{EPROG}	EPROM programming time		480			µs
t_{PSU}	Program setup time		5			µs
t_{PREC}	Program recovery time		5			µs
t_{PRE}	Program rising-edge time				5	µs
t_{PFE}	Program falling-edge time				5	µs
t_{RSTREC}			480			µs

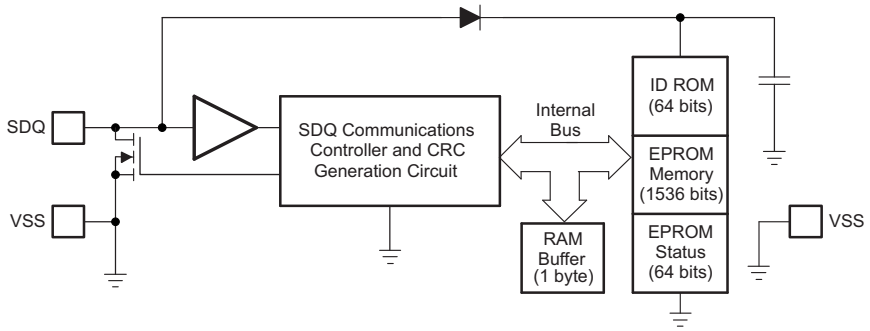
(1) 5-kΩ series resistor between SDQ pin and V_{PU}. (See Figure 1)
(2) t_{WDH} must be less than t_c to account for recovery.

7 Detailed Description

7.1 Overview

The block diagram shows the relationships among the major control and memory sections of the bq2026. The bq2026 has three main data components: a 64-bit factory-programmed ROM, including 8-bit family code, 48-bit identification number and 8-bit CRC value, 1536-bit EPROM, and EPROM Status bytes. Power for read and write operations is derived from the SDQ pin. An internal capacitor stores energy while the signal line is high, and releases energy during the low times of the SDQ pin until the pin returns high to replenish the charge on the capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EPROM

Table 1 is a memory map of the 1536-bit EPROM section of the bq2026, configured as six pages of 32 bytes each. The 1-byte RAM buffer is an additional register used when programming the memory. Data are first written to the RAM buffer and then verified by reading a 16-bit CRC from the bq2026 that confirms proper receipt of the data. If the buffer contents are correct, a programming pulse is issued and a 1-byte segment of data is written into the selected address in memory. This process ensures data integrity when programming the memory. The details for reading and programming the 1536-bit EPROM portion of the bq2026 are in the *Memory and Status Function Commands* section of this data sheet.

Table 1. 1536-Bit EPROM Data Memory Map

ADDRESS (HEX)	PAGE
00A0-00BF	Page 5
0080-009F	Page 4
0060-007F	Page 3
0040-005F	Page 2
0020-003F	Page 1
0000-001F	Page 0

7.3.2 EPROM Status Memory

In addition to the programmable 1536-bits of memory are eight bytes of status information, the first seven bytes are available to the user, contained in the EPROM status memory. The status memory is accessible with separate commands. The status bytes are EPROM and are read or programmed to indicate various conditions to the software interrogating the bq2026. These general-purpose bytes can be used by the customer to store various information.

Table 2. EPROM Status Bytes

ADDRESS (HEX)	PAGE
100h-107h	General-purpose OTP status memory

7.3.3 Error Checking

Implement error checking by comparing the 16-bit CRC values transmitted by the bq2026. If the two CRC values match, the transmission is error-free. Details are found in the CRC Generation section.

7.4 Device Functional Modes

7.4.1 Customizing the bq2026

The 64-bit ID identifies each bq2026 device. The 48-bit serial number is unique and programmed by Texas Instruments. The default 8-bit family code is 09h; however, a different value can be reserved on an individual customer basis. Contact your Texas Instruments sales representative for more information.

7.4.2 Bus Termination

Because the drive output of the bq2026 is an open-drain, N-channel MOSFET, the host must provide a source current or a 5-kΩ external pullup, as shown in the typical application circuit in Figure 1.

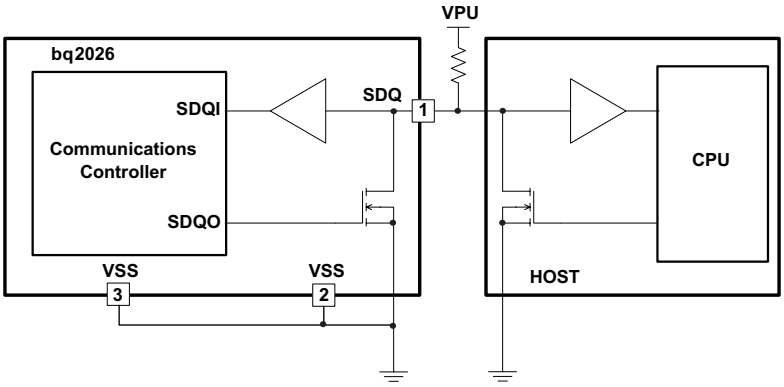


Figure 1. Bus Termination Example for SOT-23 Package

7.4.3 Serial Communication

A host reads, programs, or checks the status of the bq2026 through the hierarchical command structure of the SDQ interface. Figure 2 shows that the host must first issue a ROM command before the EPROM memory or status can be read or modified.

Initialization	ROM Command Sequence	Memory and Status Command Sequence

Figure 2. General Command Sequence

7.4.4 Initialization

Initialization consists of two pulses, the reset and the presence pulses. The host generates the reset pulse, while the bq2026 responds with the presence pulse. The host resets the bq2026 by driving the DATA bus low for at least 480 µs. For more details, see the *Reset and Presence Pulse* section.

7.4.5 ROM Commands

7.4.5.1 Read ROM

The Read ROM command sequence is the fastest sequence that allows the host to read the 8-bit family code and 48-bit identification number. The Read ROM sequence starts with the host generating the reset pulse of at least 480 µs. The bq2026 responds with a presence pulse. Next, the host continues by issuing the Read ROM command, 33h, and then reads the ROM and CRC byte using the read signaling (see the *Write* and *Read* sections) during the data frame.

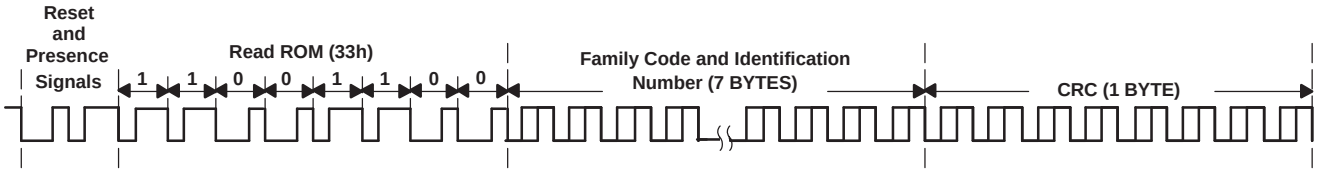


Figure 3. Read ROM Sequence

7.4.5.2 Match ROM

The Match ROM command, 55h, is used by the host to select a specific SDQ device when the family code and identification number is known. The host issues the Match ROM command followed by the family code, ROM number, and the CRC byte. The device that matches the 64-bit ROM sequence is selected and available to perform subsequent memory and status function commands.

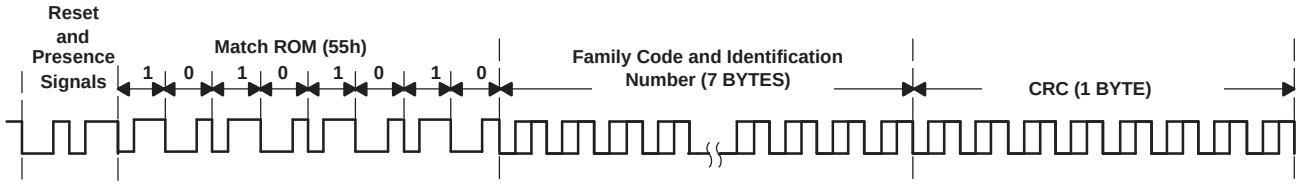


Figure 4. Match ROM Sequence

7.4.5.3 Skip ROM

This Skip ROM command, CCh, allows the host to access the memory and status functions without issuing the 64-bit ROM code sequence. The Skip ROM command is directly followed by a memory or status functions command.

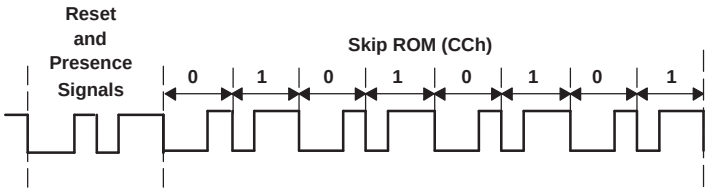


Figure 5. Skip ROM Sequence

7.4.6 Memory and Status Function Commands

Four memory and status function commands allow read and modification of the 1536-bit EPROM data memory or the 7-byte EPROM status memory. There is a Read Memory and Field CRC command, plus the Write Memory, Read Status, and Write Status commands. The bq2026 responds to memory and status function commands only after a device is selected by a ROM command.

7.4.7 Read Memory and Field CRC

To read the memory, the ROM command is followed by the Read Memory command, F0h, followed by the address low byte and then the address high byte.

The host then issues read time slots and receives data from the bq2026, starting at the initial address and continuing until the end of the 1536-bit data field is reached, or until a reset pulse is issued. If reading occurs through the end of memory space, the host may issue sixteen additional read time slots and the bq2026 responds with a 16-bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the host, any subsequent read time slots appears as logical 1s until a reset pulse is issued. Any reads ended by a reset pulse prior to reaching the end of memory do not have the 16-bit CRC available.

Initialization and ROM Command Sequence	Read Memory Command F0h	Address Low Byte A0 A7	Address High Byte A8 A15	Read EPROM Memory Until End of EPROM Memory	Read and Verify 16-bit CRC

(1) Individual bytes of address and data are transmitted LSB first.

Figure 6. Read Memory and Field CRC

7.4.8 Read Status

The Read Status command is used to read data from the EPROM status data field. After issuing a ROM command, the host issues the Read Status command, AAh, followed by the address low byte and then the address high byte.

NOTE

An 16-bit CRC of the command byte and address bytes is computed by the bq2026 and read back by the host to confirm that the correct command word and starting address were received.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the bq2026 starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point, the host receives a 16-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final byte.

This feature is provided because the EPROM status information may change over time making it impossible to program the data once and include an accompanying CRC that is always valid. Therefore, the Read Status command supplies a 16-bit CRC that is based on (and always is consistent with) the current data stored in the EPROM status data field.

After the 16-bit CRC is read, the host receives logical 1s from the bq2026 until a reset pulse is issued. The Read Status command sequence can be ended at any point by issuing a reset pulse.

Initialization and ROM CommandSequence	Read Memory Command AAh	Address Low Byte A0 A7	Address High Byte A8 A15	Read Status Memory Until End of Page	Read and Verify 16-bit CRC of command, address and data

Figure 7. READ STATUS Command

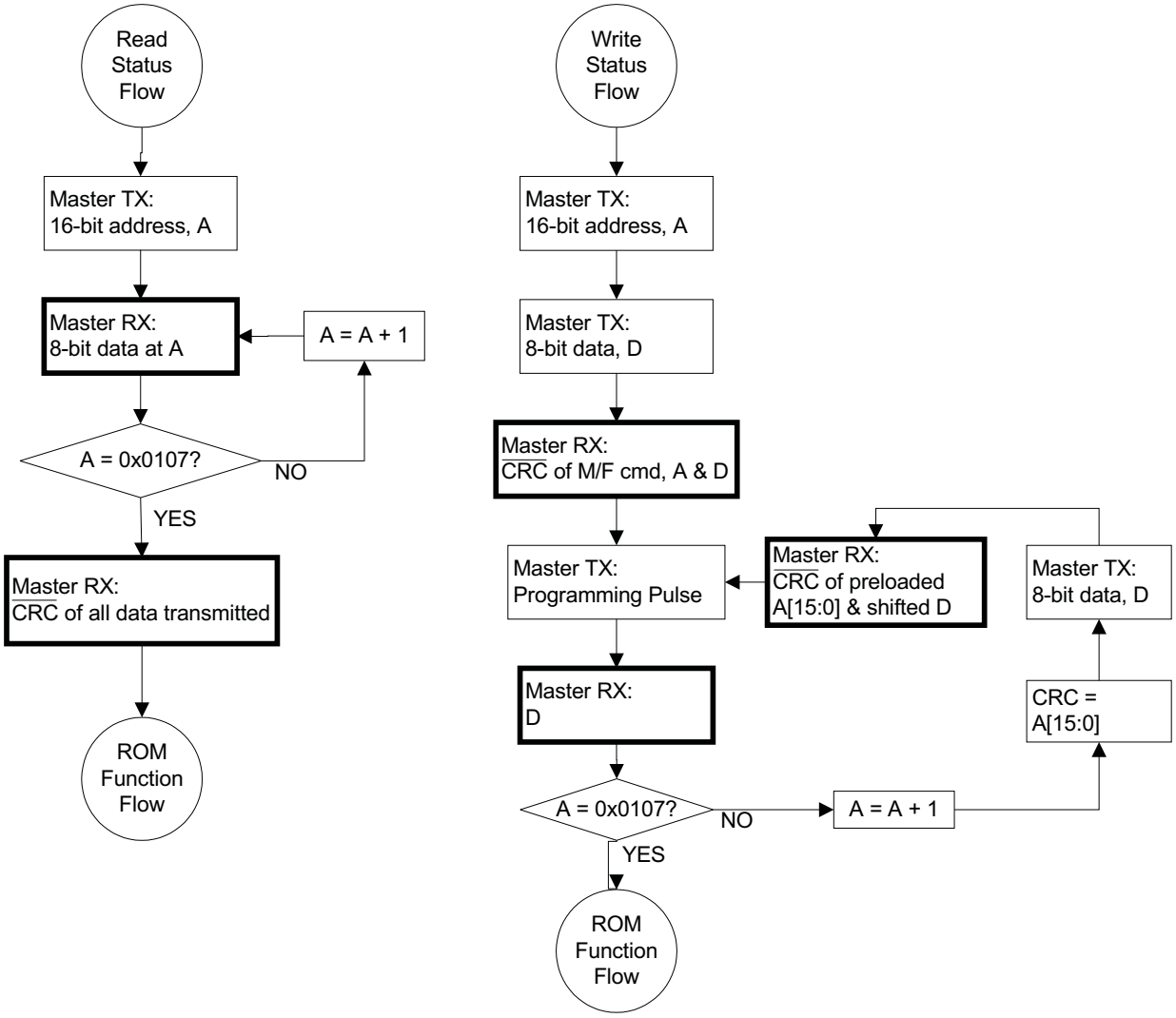


Figure 8. Status Memory Read and Write Flowchart

7.4.9 Write Memory

The Write Memory command is used to program the 1536-bit EPROM memory field. The 1536-bit memory field is programmed in 1-byte segments. Data is first written into an 1-byte RAM buffer. The contents of the RAM buffer is then ANDed with the contents of the EPROM memory field when the programming command is issued.

Figure 9 illustrates the sequence of events for programming the EPROM memory field. After issuing a ROM command, the host issues the Write Memory command, 0Fh, followed by the low byte and then the high byte of the starting address. The host then transmits 1 byte of data to the bq2026.

a 16-bit CRC is calculated and transmitted based on the command, address and data. If this CRC agrees with the CRC calculated by the host, the host applies the programming voltage for at least 480 µs or t_{EPROG}.

If at any time during the Write Memory process, the CRC read by the host is incorrect, a reset pulse must be issued, and the entire sequence must be repeated.

The Write Data Memory command sequence can be terminated at any point by issuing a reset pulse except during the program pulse period t_{PROG}.

NOTE

The bq2026 responds with the data from the selected EPROM address sent least significant-bit first. This response should be checked to verify the programmed byte. If the programmed byte is incorrect, then the host must reset the part and begin the write sequence again.

For both of these cases, the decision to continue programming is made entirely by the host, because the bq2026 is not able to determine if the 16-bit CRC calculated by the host agrees with the 16-bit CRC calculated by the bq2026.

Prior to programming, bits in the 1536-bit EPROM data field appear as logical 1s.

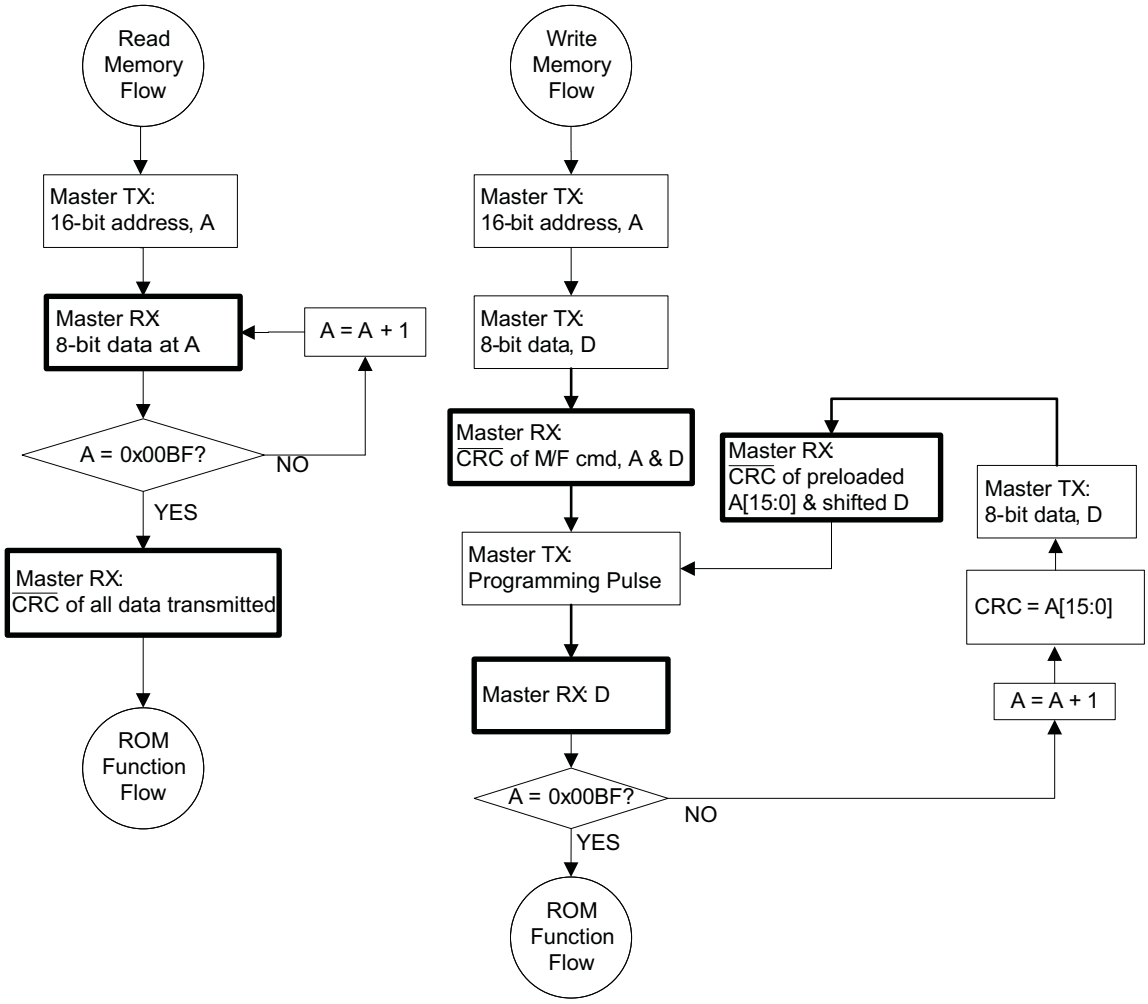


Figure 9. General Use OTP Memory Read and Write Flowchart

7.4.10 Write Status

The Write Status command is used to program the EPROM Status data field after the bq2026 has been selected by a ROM command

The flow chart in Figure 9 illustrates that the host issues the Write Status command, 55h, followed by the address low byte and then the address high byte followed by the byte of data to be programmed.

NOTE

Individual bytes of address and data are transmitted LSB first. a 16-bit CRC of the command byte, address bytes, and data byte is computed by the bq2026 and read back by the host to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the programming voltage, V_{PP} is applied to the SDQ pin for period t_{PROG}. Prior to programming, the first 7 bytes of the EPROM STATUS data field appear as logical 1s. For each bit in the data byte provided by the host that is set to a logical 0, the corresponding bit in the selected byte of the EPROM STATUS data field is programmed to a logical 0 after the programming pulse has been applied at the byte location.

After the programming pulse is applied and the data line returns to V_{PU}, the host issues eight read time slots to verify that the appropriate bits have been programmed. The bq2026 responds with the data from the selected EPROM STATUS address sent least significant bit first. This response should be checked to verify the programmed byte. If the programmed byte is incorrect, then the host must reset the device and begin the write sequence again. If the bq2026 EPROM data byte programming was successful, the bq2026 automatically increments its address counter to select the next byte in the STATUS MEMORY data field. The least significant byte of the new two-byte address is also loaded into the 16-bit CRC generator as a starting value. The host issues the next byte of data using eight write time slots.

As the bq2026 receives this byte of data into the RAM buffer, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is a 16-bit CRC of the new data byte and the new address. After supplying the data byte, the host reads this 16-bit CRC from the bq2026 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the host issues a programming pulse and the selected byte in memory is programmed.

NOTE

The initial write of the Write Status command, generates a 16-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two-address bytes, and finally the data byte. Subsequent writes within this Write Status command due to the bq2026 automatically incrementing its address counter generates a 16-bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue programming the EPROM Status registers is made entirely by the host, because the bq2026 is not able to determine if the 16-bit CRC calculated by the host agrees with the 16-bit CRC calculated by the bq2026. If an incorrect CRC is ignored and a program pulse is applied by the host, incorrect programming could occur within the bq2026. Also note that the bq2026 always increments its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the host, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the bq2026. The Write Status command sequence can be ended at any point by issuing a reset pulse.

Table 3. Command Code Summary

COMMAND (HEX)	DESCRIPTION	CATEGORY
33h	Read serialization ROM and CRC	ROM Commands Available in Command Level I
55h	Match serialization ROM	
CCh	Skip serialization ROM	
F0h	Read memory and field CRC	Memory Function Commands Available in Command Level II
AAh	Read EPROM status	
0Fh	Write memory	
55h	Write EPROM status	

7.4.11 SDQ Signaling

All SDQ signaling begins with initializing the device, followed by the host driving the bus low to write a 1 or 0, or to begin the start frame for a bit read. Figure 10 shows the initialization timing, whereas Figure 11 and Figure 12 show that the host initiates each bit by driving the data bus low for the start period, t_{WSTRB} / t_{RSTRB}. After the bit is initiated, either the host continues controlling the bus during a write, or the bq2026 responds during a read.

7.4.12 Reset and Presence Pulse

If the data bus is driven low for more than 120 µs, the bq2026 may be reset. Figure 10 shows that if the data bus is driven low for more than 480 µs, the bq2026 resets and indicates that it is ready by responding with a presence pulse.

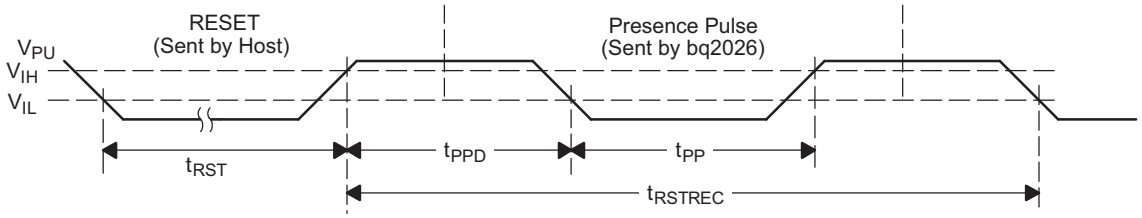


Figure 10. Reset Timing Diagram

7.4.13 Write

The Write bit timing diagram in Figure 11 shows that the host initiates the transmission by issuing the t_{WSTRB} portion of the bit and then either driving the data bus low for a write 0, or releasing the data bus for a write 1.

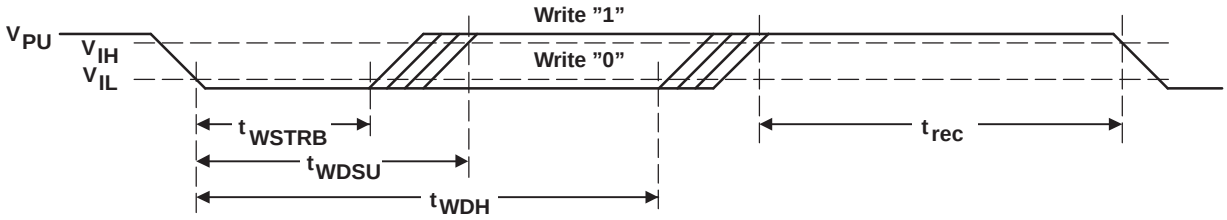


Figure 11. Write Bit Timing Diagram

7.4.14 Read

The Read bit timing diagram in Figure 12 shows that the host initiates the transmission of the bit by issuing the t_{RSTRB} portion of the bit. The bq2026 then responds by either driving the data bus low to transmit a read 0, or releasing the data bus to transmit a read 1.

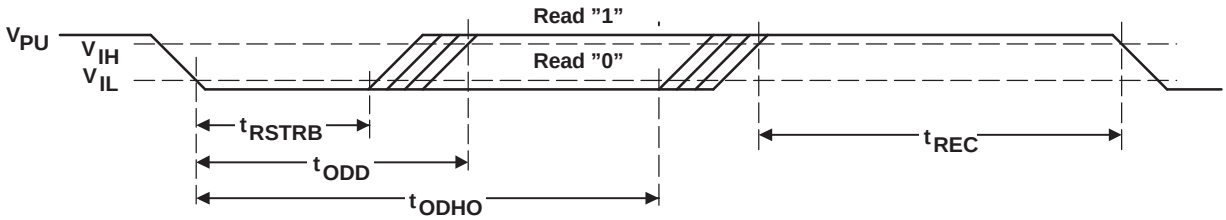


Figure 12. Read Bit Timing Diagram

7.4.15 Program Pulse

Figure 13 shows the program pulse timing.

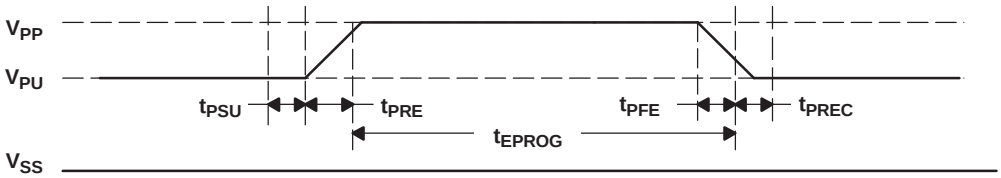


Figure 13. Program Pulse Timing Diagram

7.4.16 Idle

If the bus is high, the bus is in the idle state. Bus transactions can be suspended by leaving the data bus in idle. Bus transactions can resume at any time from the idle state.

7.4.17 CRC Generation

The bq2026 has a 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master computes a CRC value from the first 56 bits of the 64-bit ROM and compares it to the value stored within the bq2026 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is shown in Figure 14.

Under certain conditions, the bq2026 also generates a 16-bit CRC value using the polynomial function is shown in Figure 15 and provides this value to the bus master which validates the transfer of command, address, and data bytes from the bus master to the bq2026. The bq2026 computes a 16-bit CRC for the command, address, and data bytes received for the Write Memory and the Write Status commands, and then outputs this value to the bus master which confirms proper transfer. Similarly, the bq2026 computes a 16-bit CRC for the command and address bytes received from the bus master for the Read Memory, and Read Status commands to confirm that these bytes have been received correctly.

In each case, where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function in Figure 14 or Figure 15 and compares the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the bq2026 (for ROM reads) or the 16-bit CRC value computed within the bq2026. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. No circuitry on the bq2026 prevents a command sequence from proceeding if the CRC stored in or calculated by the bq2026 does not match the value generated by the bus master. Proper use of the CRC can result in a communication channel with a high level of integrity.

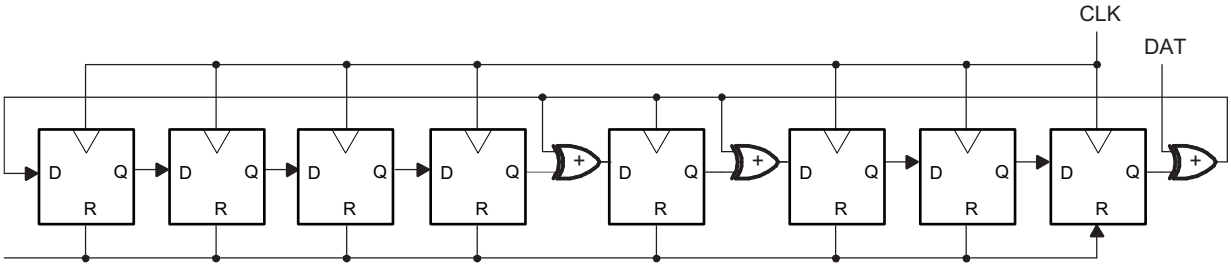


Figure 14. 8-bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$) for Serial Number Read

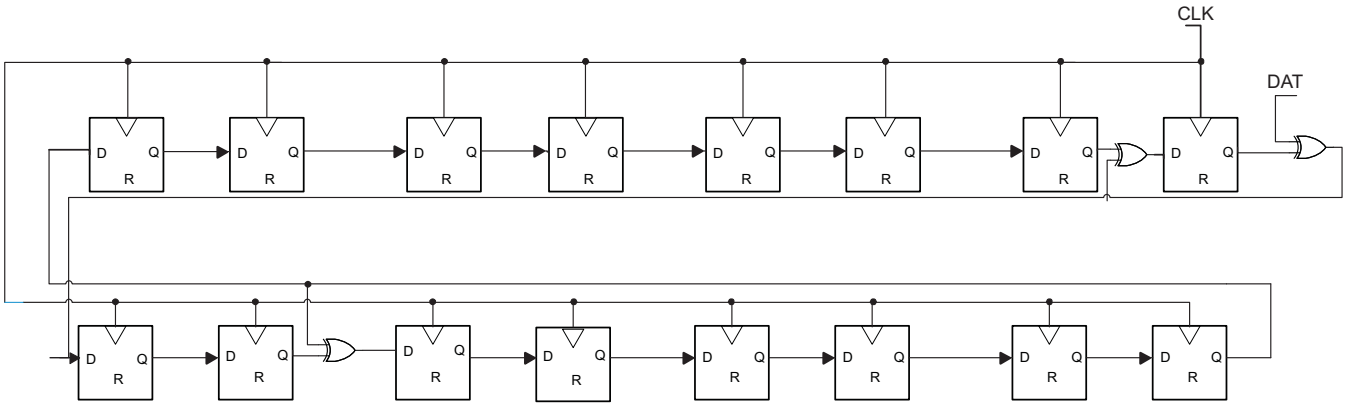


Figure 15. 16-bit CRC Generator Circuit ($X^{16} + X^{15} + X^2 + 1$) for Memory Interface

8 Device and Documentation Support

8.1 Trademarks

SDQ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2026DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 70	WAIS	Samples
BQ2026LPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	SN	N / A for Pkg Type	-20 to 70	BQ2026	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

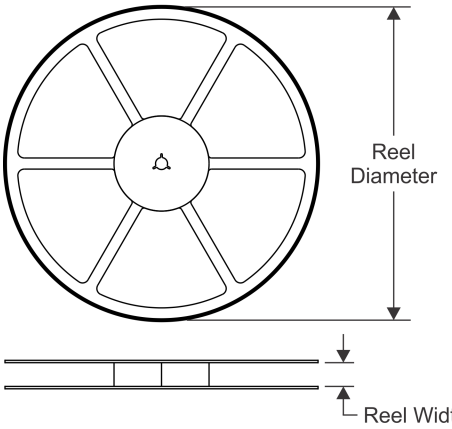
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

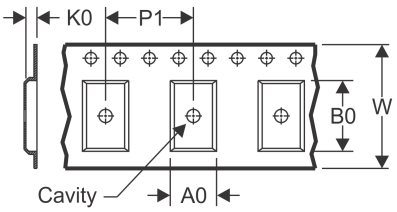
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

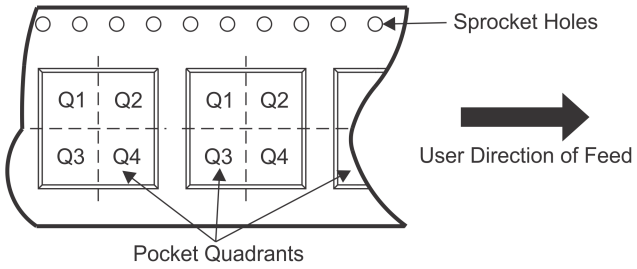


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

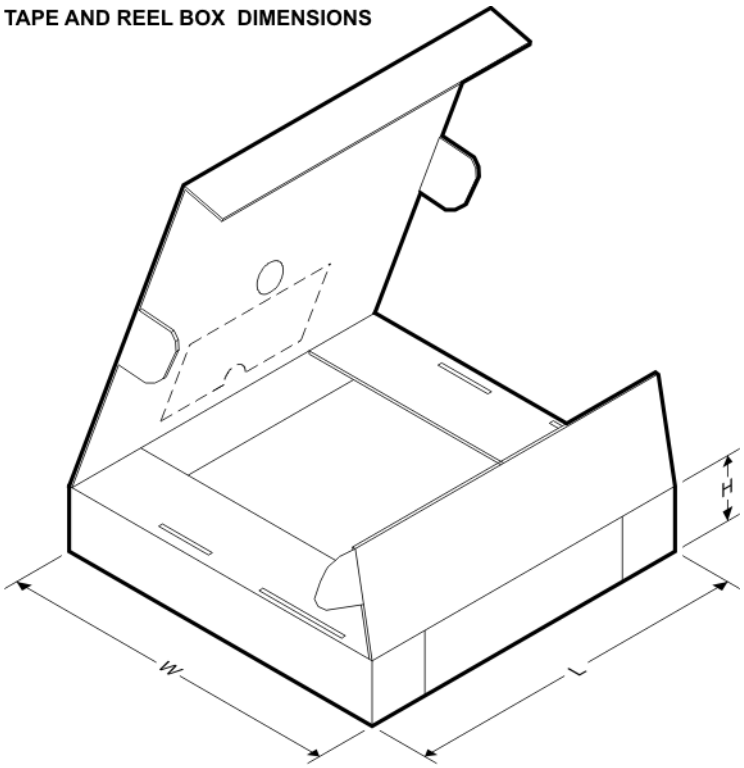
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2026DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2026DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

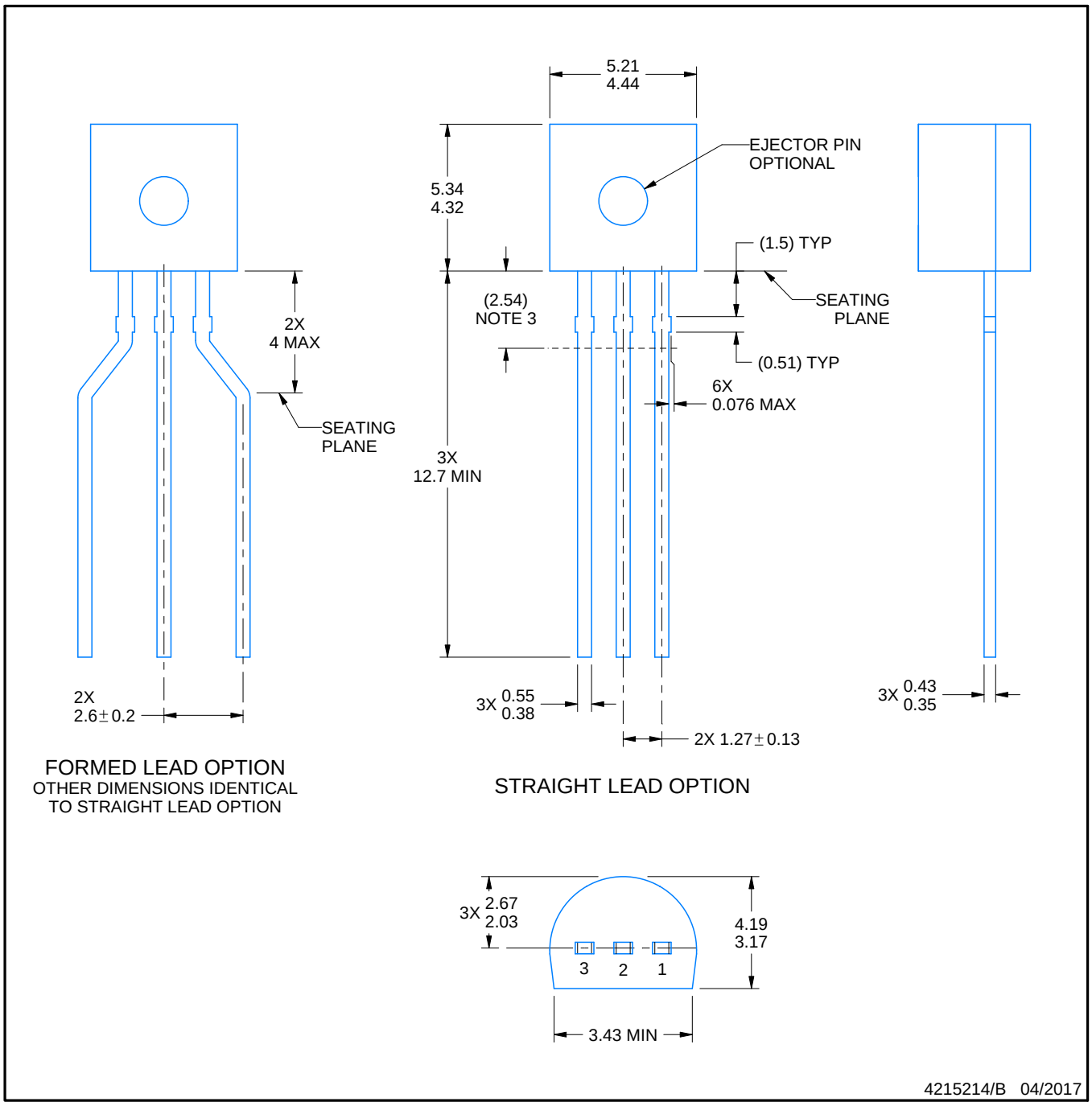
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

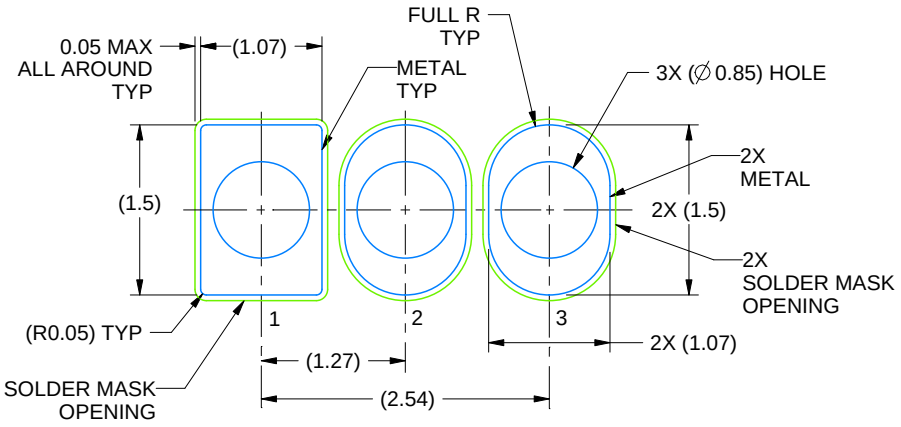
TO-92 - 5.34 mm max height

TO-92

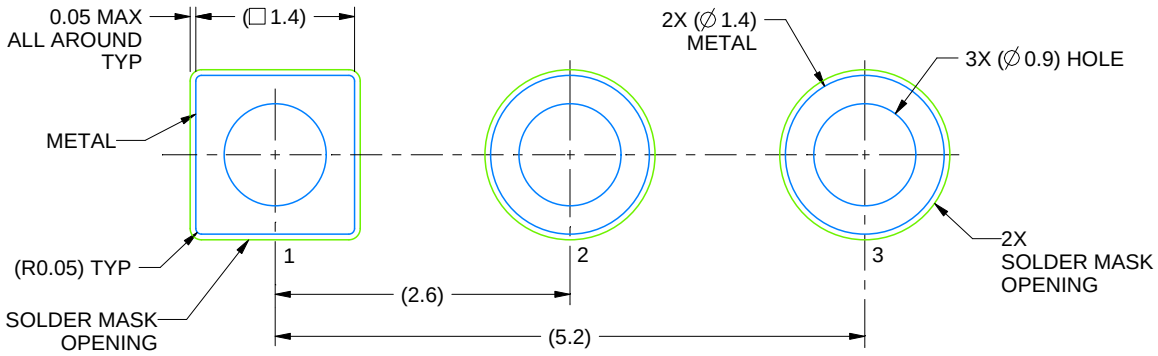


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



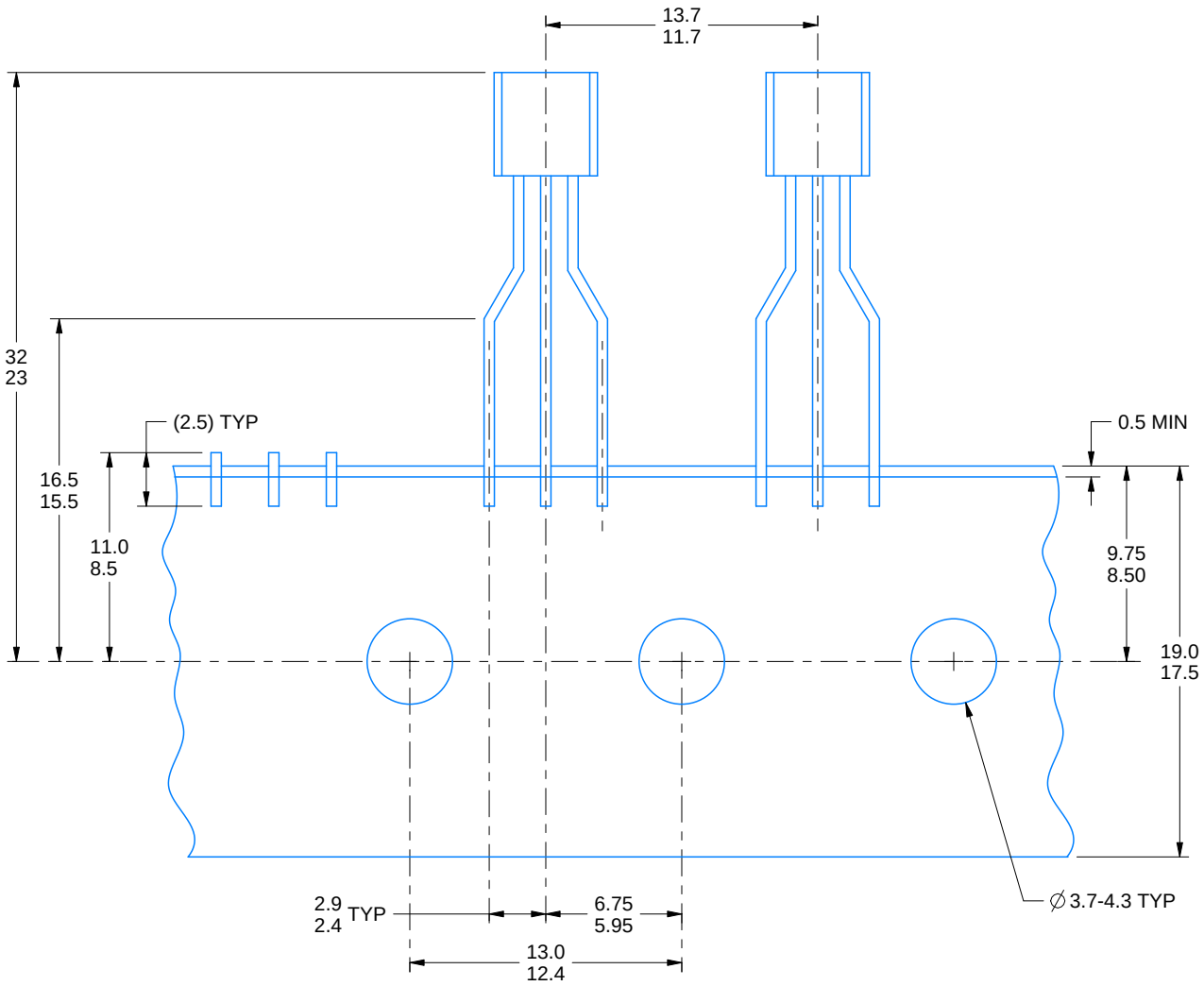
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



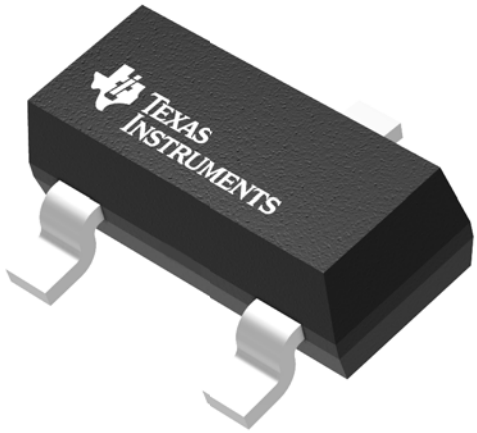
FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



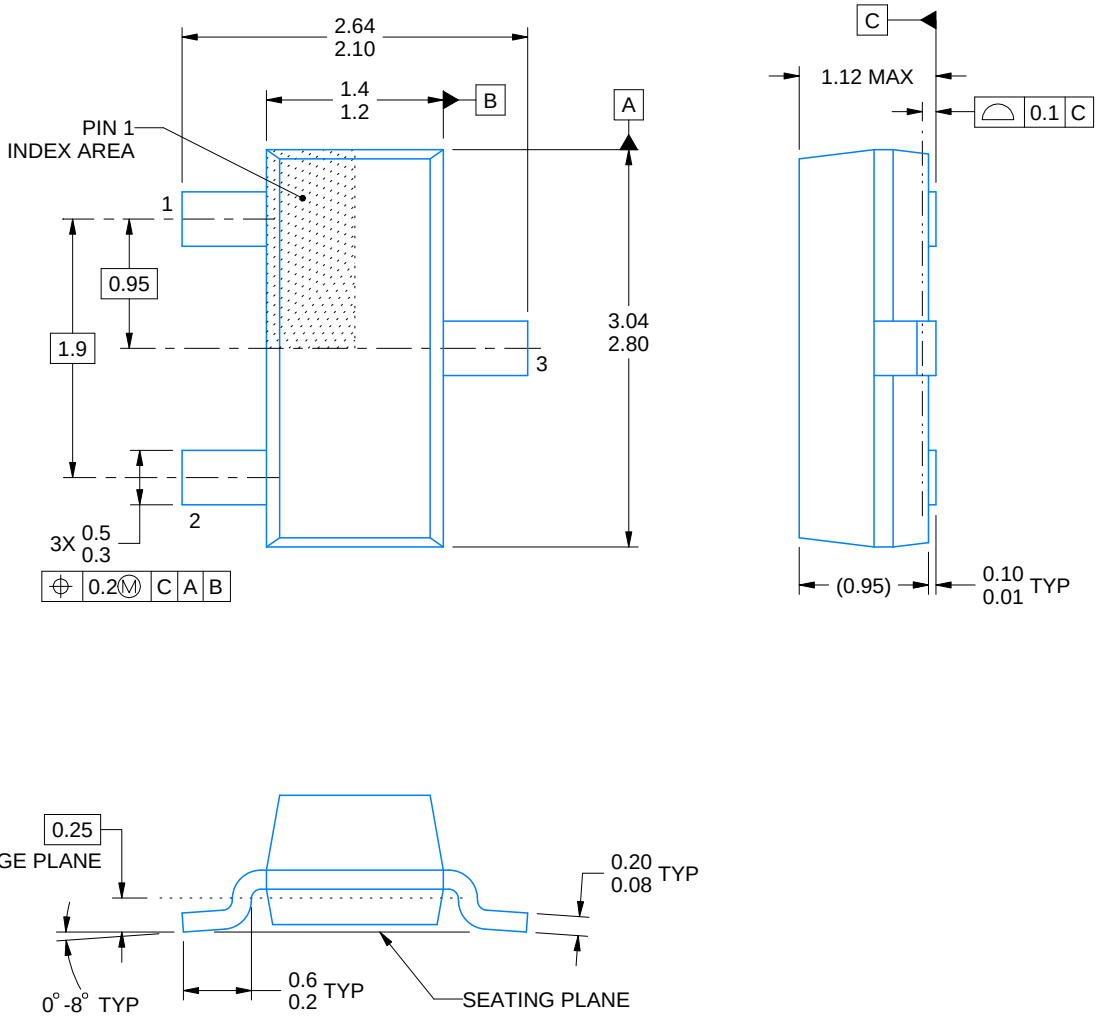
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

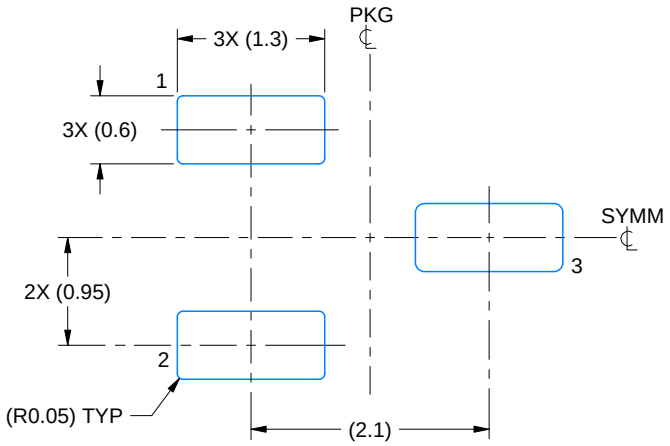
SMALL OUTLINE TRANSISTOR



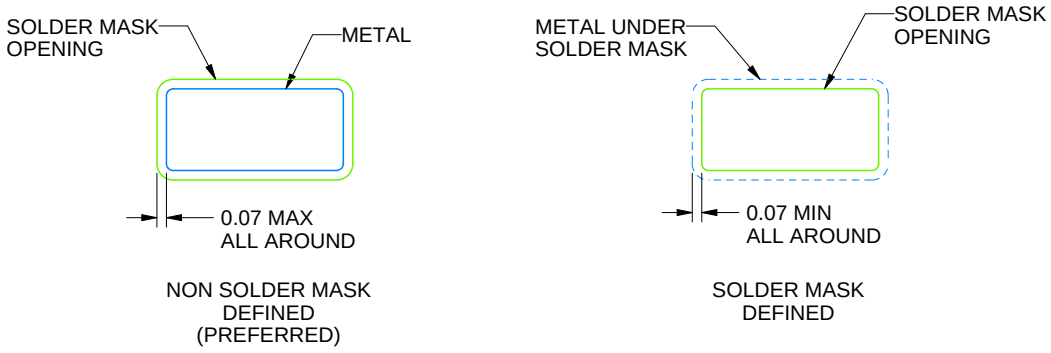
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

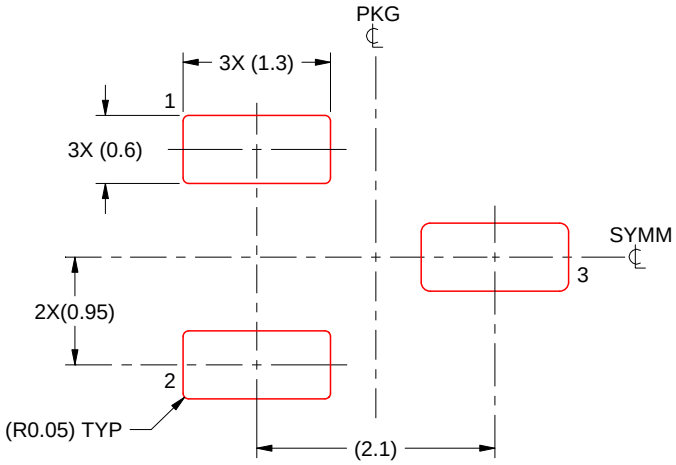


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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