TEXAS INSTRUMENTS

ISO7240CF, ISO7240C, ISO7240M
ISO7241C, ISO7241M, ISO7242C, ISO7242M

SLLS868T – SEPTEMBER 2007 – REVISED APRIL 2017

ISO724x High-Speed, Quad-Channel Digital Isolators

1 Features

- 25 and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns Maximum
  - Low Pulse-Width Distortion (PWD); 2 ns Maximum
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Selectable Default Output (ISO7240CF)
- > 25-Year Life at Rated Working Voltage (see *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* and Isolation Capacitor Lifetime Projection)
- 4-kV ESD Protection
- Operates With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see *ISO72x Digital Isolator Magnetic-Field Immunity*)
- –40°C to +125°C Operating Temperature Range
- Safety-Related Certifications:
  - VDE 4000 V_{PK} Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 2.5 kV_{RMS} Insulation for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A and IEC 60950-1 End Equipment Standard

2 Applications

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7240x, ISO7241x, and ISO7242x devices are quad-channel digital isolators with multiple channel configurations and output-enable functions. These devices have logic-input and logic-output buffers separated by Texas Instrument's silicon-dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices help block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

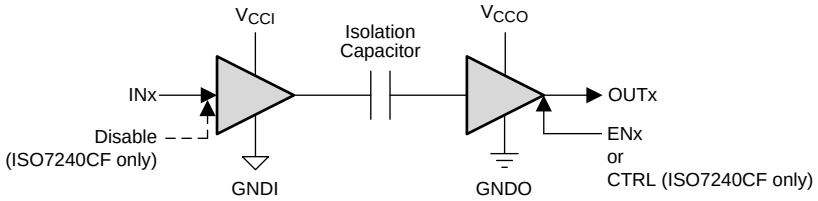
The ISO7240x family of devices has all four channels in the same direction. The ISO7241x family of devices has three channels in the same direction and one channel in the opposition direction. The ISO7242x family of devices has two channels in each direction.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7240CF	SOIC (16)	10.30 mm × 7.50 mm
ISO7240C		
ISO7240M		
ISO7241C		
ISO7241M		
ISO7242C		
ISO7242M		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (April 2016) to Revision T **Page**

- Added isolation resistance for 100°C ≤ T_A ≤ 125°C in the *Insulation Specifications* table ... 11
- Deleted the maximum transient overvoltage from VDE in the *Safety-Related Certifications* table ... 11
- Added the *Receiving Notification of Documentation Updates* and the *Community Resources* section ... 33

Changes from Revision R (September 2015) to Revision S **Page**

- Changed the HBM value from ±4 V to ±4000 V and the CDM value from ±1 V to ±1000 V in the *ESD Ratings* table ... 9
- Moved the device power dissipation parameter from the *Thermal Information* table to the *Power Dissipation Characteristics* table ... 10

Changes from Revision Q (January 2015) to Revision R **Page**

- Changed *Features* From: "Basic Isolation per DIN EN 60747-5-5 (VDE 0884-5) & DIN EN 61010-1" To:"Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" ... 1
- Changed V_{CC1} To V_{CCI}, V_{CC2} To V_{CCO}, GND1 To GNDI, and GND2 To GNDO, and added Notes 1 and 2 to the

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Changes from Revision P (August 2014) to Revision Q **Page**

Changes from Revision O (November 2012) to Revision P **Page**

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Changes from Revision N (January 2012) to Revision O **Page**

- Added the *Safety Limiting Values* section 12

Changes from Revision M (January 2011) to Revision N **Page**

- Changed Feature From: Operates 3.3-V or 5-V Supplies To: Operates With 2.8-V (ISO7241C), 3.3-V or 5-V Supplies 1
- Added device options to V_{CC} in the RECOMMENDED OPERATING CONDITIONS table 9
- Changed Table Note (1) 9
- Changed the CTI MIN value From: ≥175 V To:≥400 V 11
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- Changed Table Note (1) 12
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- Changed Table Note (1) 13
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 5-V, V_{CC2} at 3.3-V *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* table 13
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- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} and V_{CC2} at 3.3 V table 15
- Changed *V_{CC} Undervoltage Threshold vs Free-Air Temperature* From V_{CC1} Failsafe Threshold To: V_{CC} Undervoltage Threshold 19

Changes from Revision L (January 2010) to Revision M **Page**

- Changed the CSA File Number From: 1698195 To: 220991 11
- Changed Switching Characteristic Test Circuit and Voltage Waveforms, Failsafe Delay Time Test Circuit and Voltage Waveforms, and Wake Time From Input Disable Test Circuit and Voltage Waveforms 21

Changes from Revision K (Decemberl 2009) to Revision L **Page**

- Added CTI - Tracking resistance (comparative tracking index to the *Package Characteristics* table 11
- Added the IEC 60664-1 RATINGS TABLE 11
- Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table 11

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- Changed the Input circuit in the DEVICE I/O SCHEMATICS illustration 1
- Added Note 1 to LI01), and changed the MIN value From: 8.34 To 8 mm in the *Package Characteristics* table 11
- Added Note 1 to LI02), and changed the MIN value From: 8.1 To 8 mm in the *Package Characteristics* table 11

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- Changed I_{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA 12
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- Added Features Bullet: Selectable Failsafe Output (ISO7240CF) ... 1
- Changed description paragraph 4 text. ... 7
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- Added t_{wake}, Wake time from input disable ... 16
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- Changed Title From: QUAD DIGITAL ISOLATORS To: HIGH SPEED QUAD DIGITAL ISOLATORS ... 1
- Changed Feature Low Jitter Content - From: 1, 25, and 150-Mbps Signaling Rate Options To: 25, and 150-Mbps Signaling Rate Options ... 1
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5 Description (Continued)

The devices with the C suffix (C option) have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The devices with the M suffix (M option) have CMOS $V_{CC}/2$ input thresholds and do not have the input noise filter or the additional propagation delay.

The ISO7240CF device has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe output is a logic high when a logic high is placed on the CTRL pin or it is left unconnected. If a logic low signal is applied to the CTRL pin, the failsafe output becomes a logic-low output state. The input disable function of the ISO7240CF device prevents data from being passed across the isolation barrier to the output. When the inputs are disabled or V_{CC1} is powered down, the outputs are set by the CTRL pin.

These devices can be powered from 3.3-V or 5-V supplies on either side, in any combination. The signal input pins are 5-V tolerant regardless of the voltage supply level that is used.

These devices are characterized for operation over the ambient temperature range of –40°C to +125°C.

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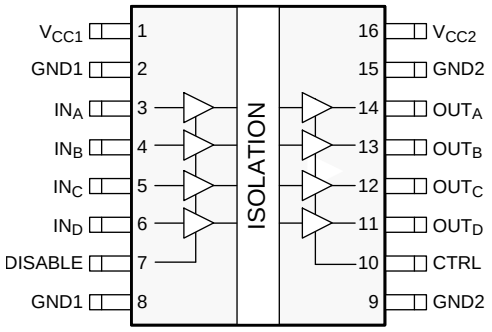
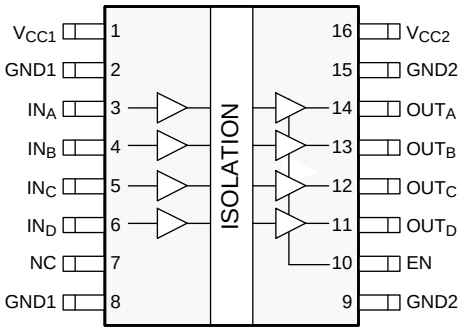
6 Pin Configurations and Functions

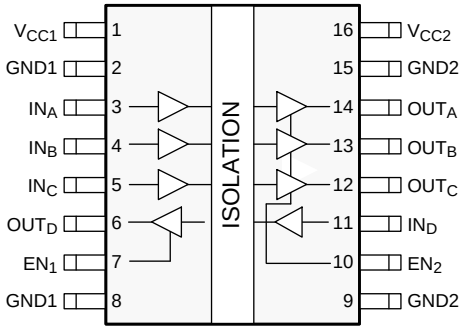
ISO7240CF DW Package
16-Pin SOIC
Top View



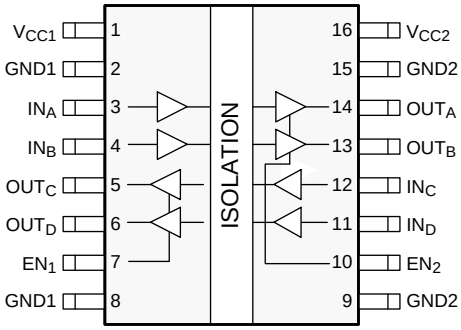
ISO7240C and ISO7240M DW Package
16-Pin SOIC
Top View



ISO7241C and ISO7241M DW Package
16-Pin SOIC
Top View



ISO7242C and ISO7242M DW Package
16-Pin SOIC
Top View



Pin Functions

PIN					I/O	DESCRIPTION3
NAME	NO.					
	ISO7240CF	ISO7240C ISO7240M	ISO7241C ISO7241M	ISO7242C ISO7242M		
CTRL	10	—	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V_{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	10	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN_1	—	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN_1 is high or open and disabled when EN_1 is low.
EN_2	—	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN_2 is high or open and disabled when EN_2 is low.
GND1	2, 8	2, 8	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	9, 15	9, 15	—	Ground connection for V_{CC2}
IN_A	3	3	3	3	I	Input, channel A
IN_B	4	4	4	4	I	Input, channel B
IN_C	5	5	5	12	I	Input, channel C
IN_D	6	6	11	11	I	Input, channel D
NC	—	7	—	—	—	No Connect pins are floating with no internal connection
OUT_A	14	14	14	14	O	Output, channel A
OUT_B	13	13	13	13	O	Output, channel B
OUT_C	12	12	12	5	O	Output, channel C
OUT_D	11	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	16	—	Power supply, V_{CC2}

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7 Specifications

7.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT, EN, DISABLE, CTRL	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM), per ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width	ISO724xC	40			ns
		ISO724xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO724xC	0	30(2)	25	Mbps
		ISO724xM	0	200(2)	150	
V_{IH}	High-level input voltage (IN)	ISO724xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	V
V_{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	ISO724xC	2		5.5	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)		0		0.8	V
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
(2) Typical value at room temperature and well-regulated power supply.

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7.4 Thermal Information

THERMAL METRIC[1]			ISO724xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K board	168	°C/W
		High-K board	77.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter		41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation				220	mW

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7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 400	V
	Material group		II	
	Overvoltage Category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3. V_{ini} = VIOTM, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s,	≤5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = VIOTM, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s,	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = VIOTM, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s,	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_I = 0.4 sin (4E6πt)	2	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		V_{IO} = 500 V at T_S = 150°C	>10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

7.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Isolation Voltage, 4000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 560 V_{PK}	4000 V_{PK} maximum isolation rating; Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 366 V_{RMS} maximum working voltage,	Single protection, 2500 V_{RMS}
Certificate Number: 40016131	Master Contract Number: 220991	File Number: E181974

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7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 168°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Figure 2			156	mA
		$R_{\theta JA}$ = 168°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Figure 2			239	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel		0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 11	V_{CCO} – 0.8			V
		I_{OH} = –20 µA, See Figure 11	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 11			0.4	V
		I_{OL} = 20 µA, See Figure 11			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN at V_{CCI}			10	µA
I_{IL}	Low-level input current	IN at 0 V	–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15	25	50		kV/µs

7.10 Supply Current Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	Quiescent, All channels, no load, EN at 3 V, V_I = V_{CC} or 0 V			1	3	mA
		25 Mbps, All channels, no load, EN at 3 V, 12.5-MHz input-clock signal			7	10.5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		15	22	mA
			25 Mbps, 12.5-MHz input-clock signal		17	25	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6.5	11	mA
			25 Mbps, 12.5-MHz input-clock signal		12	18	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		13	20	mA
			25 Mbps, 12.5-MHz input-clock signal		18	28	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	

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7.11 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 11	3.3-V side	V_{CCO} – 0.4			V
			5-V side	V_{CCO} – 0.8			
		I_{OH} = –20 μA, See Figure 11		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 11				0.4	V
		I_{OL} = 20 μA, See Figure 11				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN at V_{CCI}				10	μA
I_{IL}	Low-level input current	IN at 0 V		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15		25	50		kV/μs

7.12 Supply Current Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		1	3	mA
			25 Mbps, 12.5-MHz input-clock signal		7	10.5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		9.5	15	mA
			25 Mbps, 12.5-MHz input-clock signal		10.5	17	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6.5	11	mA
			12.5-MHz input-clock signal		12	18	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		8	13	mA
			25 Mbps, 12.5-MHz input-clock signal		11.5	18	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			12.5-MHz input-clock signal		15	24	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	

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7.13 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 11	3.3-V side	V_{CCO} – 0.4			V
			5-V side	V_{CCO} – 0.8			
		I_{OH} = –20 μA, See Figure 11		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 11				0.4	V
		I_{OL} = 20 μA, See Figure 11				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN at V_{CCI}				10	μA
I_{IL}	Low-level input current	IN at 0 V		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15		25	50		kV/μs

7.14 Supply Current Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		0.5	1	mA
			25 Mbps, 12.5-MHz input-clock signal		3	5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		15	22	mA
			25 Mbps, 12.5-MHz input-clock signal		17	25	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		4	7	mA
			25 Mbps, 12.5-MHz input-clock signal		6.5	11	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		13	20	mA
			25 Mbps, 12.5-MHz input-clock signal		18	28	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	

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7.15 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, single channel		0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 11	V_{CCO} – 0.4			V
		I_{OH} = –20 μA, See Figure 11	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 11			0.4	V
		I_{OL} = 20 μA, See Figure 11			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN at V_{CCI}			10	μA
I_{IL}	Low-level input current	IN at 0 V	–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 15	25	50		kV/μs

7.16 Supply Current Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		0.5	1	mA
			25 Mbps, 12.5-MHz input-clock signal		3	5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		9.5	15	mA
			25 Mbps, 12.5-MHz input-clock signal		10.5	17	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		4	7	mA
			25 Mbps, 12.5-MHz input-clock signal		6.5	11	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		8	13	mA
			25 Mbps, 12.5-MHz input-clock signal		11.5	18	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	

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7.17 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 11	18		42	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xC	See Figure 11			2.5	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 11	10		23	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xM	See Figure 11		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				8	ns
		ISO724xM			0	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				2	ns
		ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 11		2		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 12		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 12		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		12		µs
t_{wake}	Wake time from input disable		See Figure 14		15		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 16		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.18 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 11	20		50	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xC	See Figure 11			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 11	12		29	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xM	See Figure 11		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
		ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				3	ns
		ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 11		2		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 12		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 12		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		18		µs
t_{wake}	Wake time from input disable		See Figure 14		15		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 16		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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7.19 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 11	22		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xC	See Figure 11			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 11	12		30	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xM	See Figure 11		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
		ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				2.5	ns
		ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 11		2		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 12		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 12		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		12		µs
t_{wake}	Wake time from input disable		See Figure 14		15		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 16		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.20 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 11	25		56	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$(1)	ISO724xC	See Figure 11			4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 11	12		34	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$(1)	ISO724xM	See Figure 11		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
		ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				3.5	ns
		ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 11		2		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 12		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 12		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 12		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		18		µs
t_{wake}	Wake time from input disable		See Figure 14		15		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 16		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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7.21 Insulation Characteristics Curves

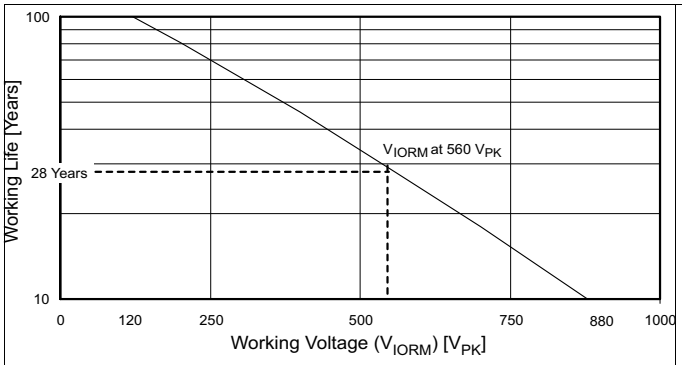

Figure 1. Isolation Capacitor Lifetime Projection

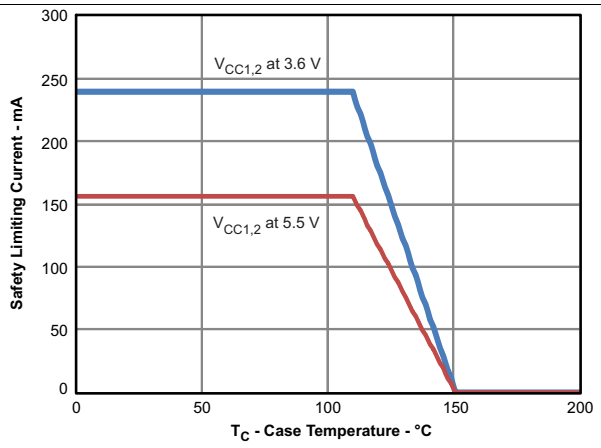

Figure 2. Thermal Derating Curve for Limiting Current per VDE

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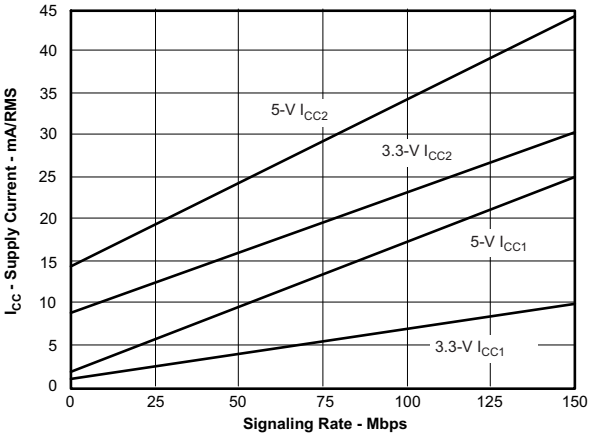
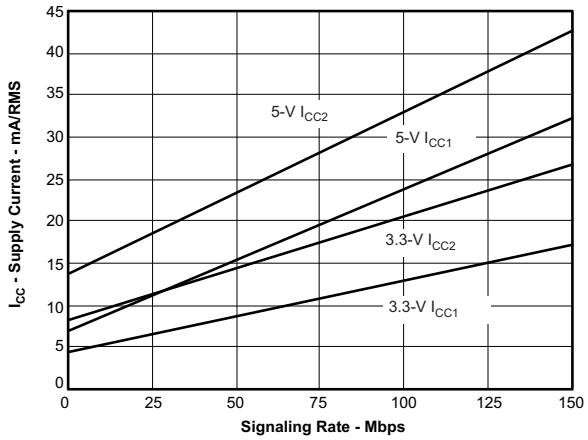
7.22 Typical Characteristics



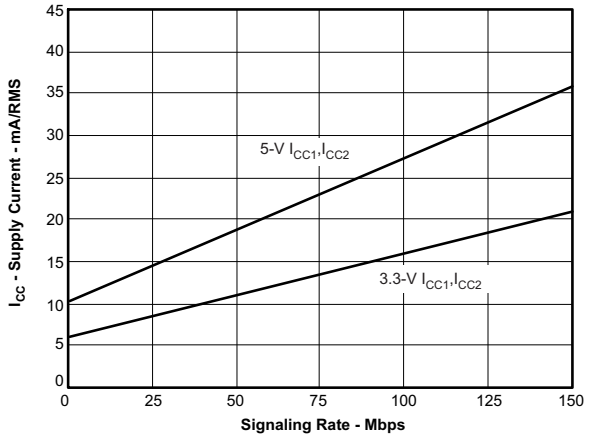
T_A = 25°C Load = 15 pF All Channels

Figure 3. ISO7240C/M RMS Supply Current vs Signaling Rate



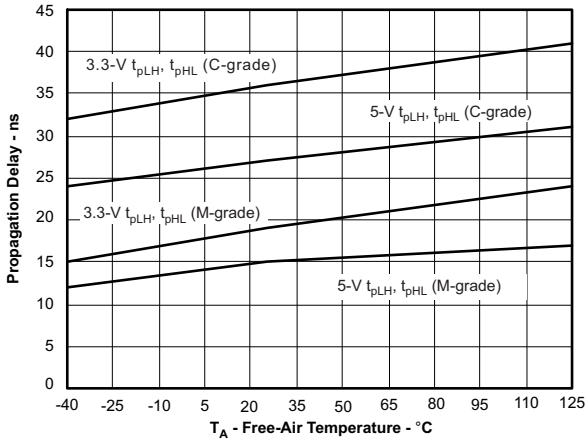
T_A = 25°C Load = 15 pF All Channels

Figure 4. ISO7241C/M RMS Supply Current vs Signaling Rate



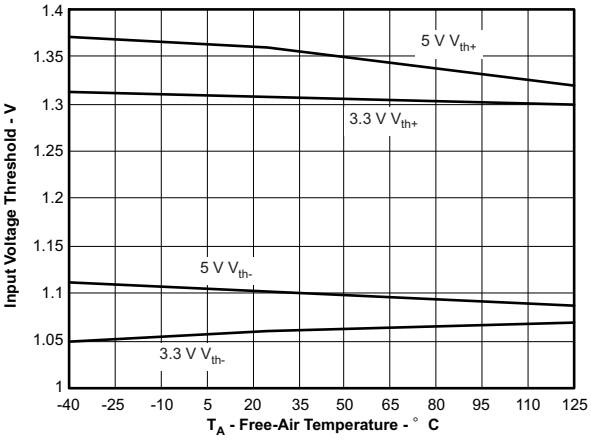
T_A = 25°C Load = 15 pF All Channels

Figure 5. ISO7242C/M RMS Supply Current vs Signaling Rate



T_A = 25°C Load = 15 pF All Channels

Figure 6. Propagation Delay vs Free-Air Temperature



Air Flow at 7 cf/m Low_K Board

Figure 7. Input Voltage Threshold vs Free-Air Temperature

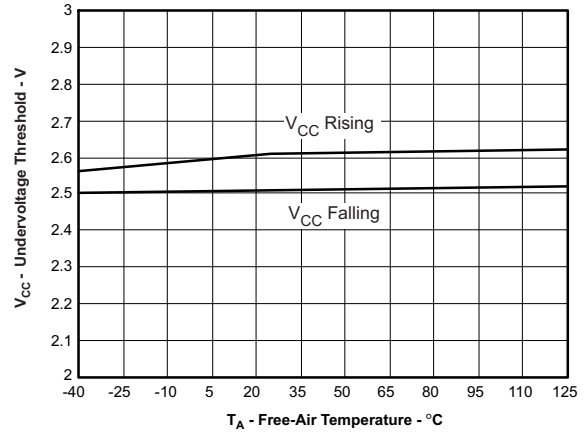
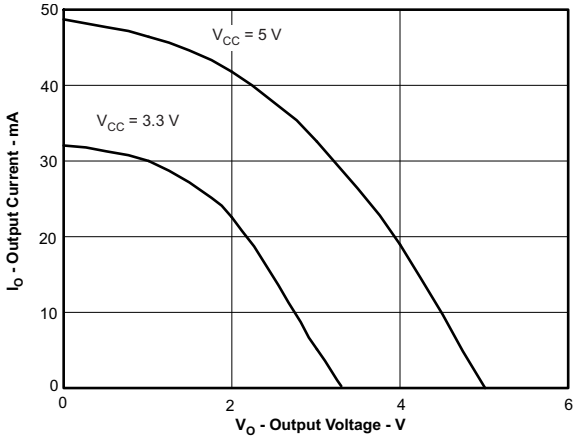


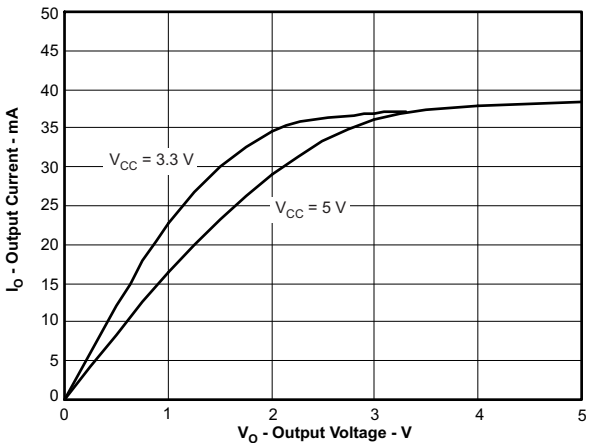
Figure 8. V_{CC} Undervoltage Threshold vs Free-Air Temperature

Typical Characteristics (continued)



T_A = 25°C Load = 15 pF

Figure 9. High-Level Output Current vs High-Level Output Voltage



T_A = 25°C Load = 15 pF

Figure 10. Low-Level Output Current vs Low-Level Output Voltage

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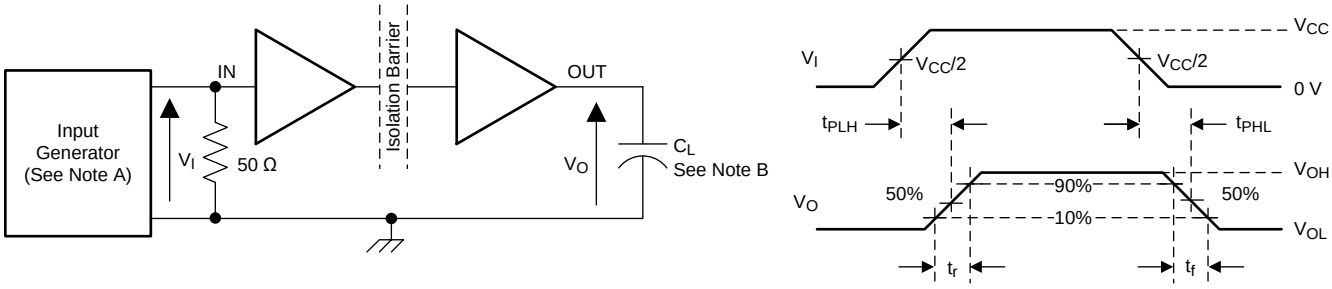
8 Parameter Measurement Information



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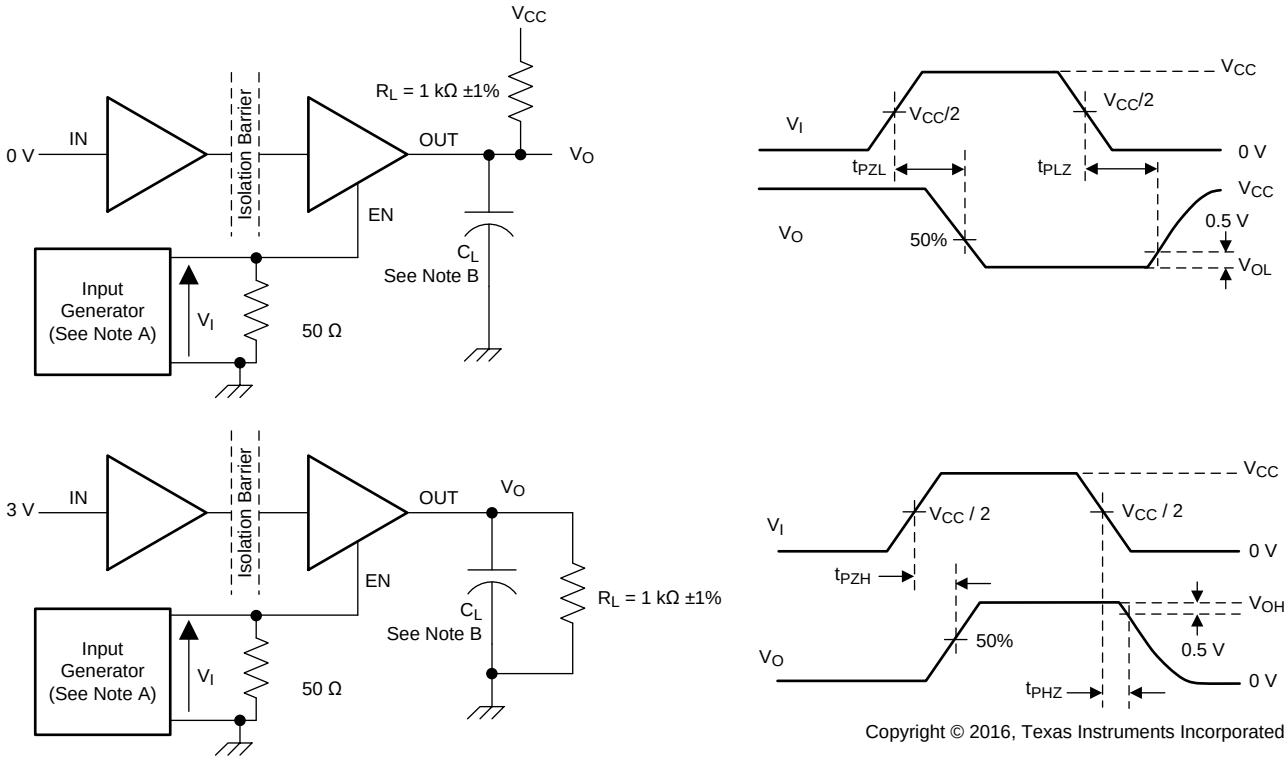
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms



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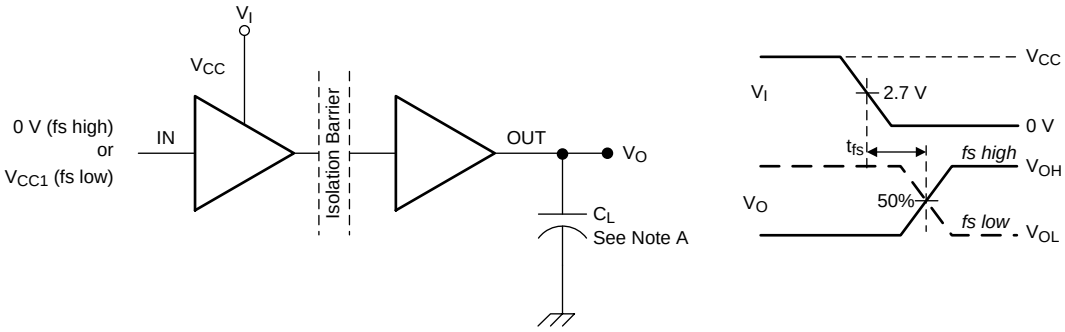
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

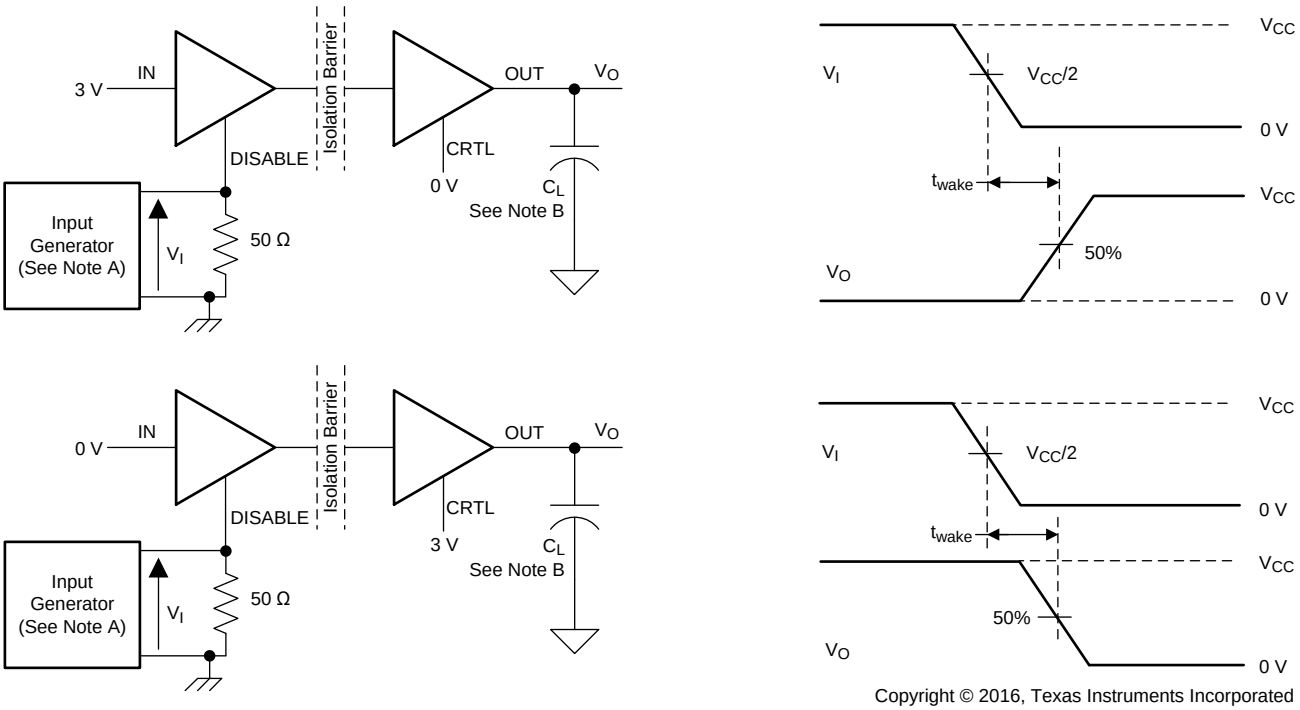
Figure 12. Enable or Disable Propagation-Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Failsafe Delay Time Test Circuit and Voltage Waveforms



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NOTE: The test that yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Wake Time From Input Disable Test Circuit and Voltage Waveforms

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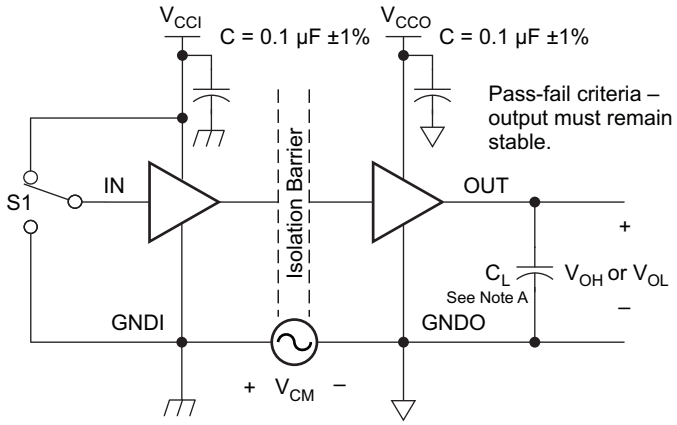
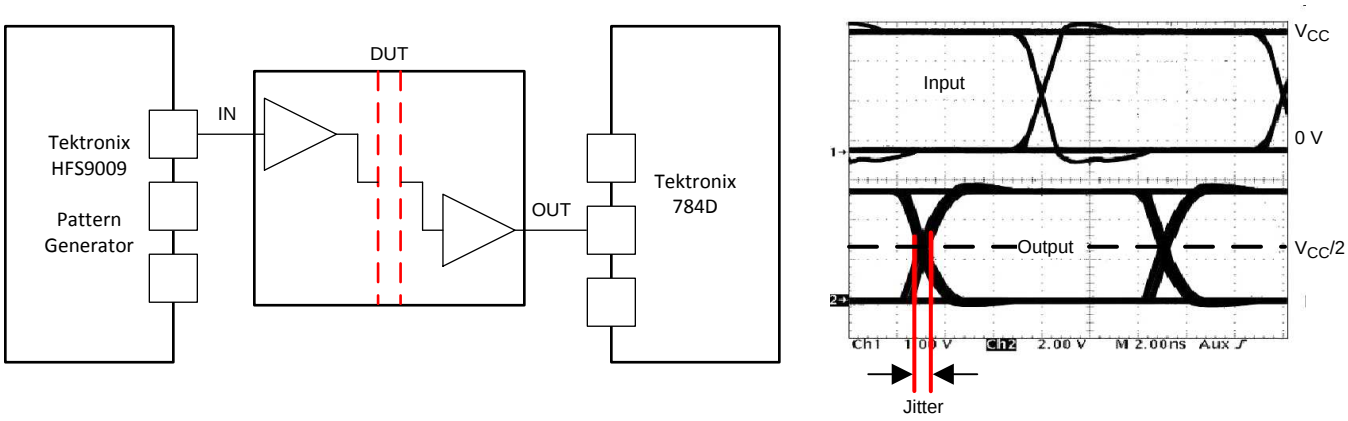
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

Figure 15. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



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NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 16. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

9 Detailed Description

9.1 Overview

The isolator in Figure 17 is based on a capacitive isolation-barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop the output of which feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, as in the case of a low-frequency signal, the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is required to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

9.2 Functional Block Diagram

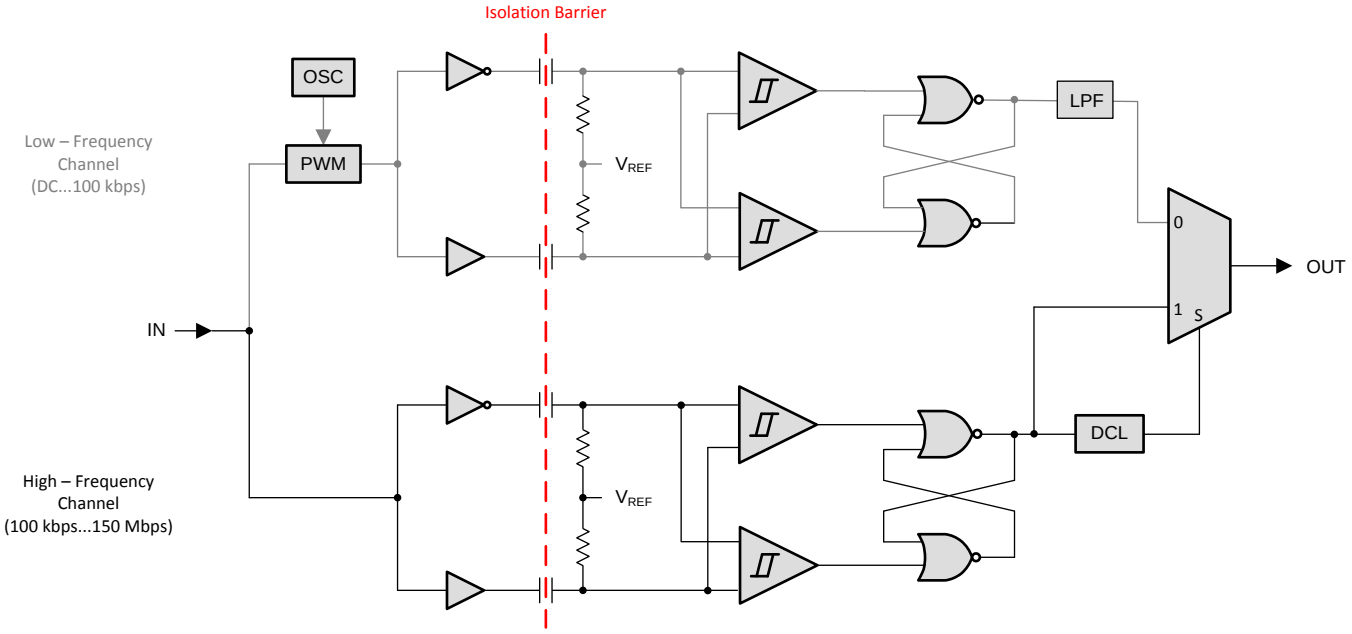

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Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

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9.3 Feature Description

The ISO724xx family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. Table 1 lists these device features.

Table 1. Device Features

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240C	25 Mbps	~1.5 V (TTL)	4/0
ISO7240CF	25 Mbps	~1.5 V (TTL)	
ISO7240M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7241C	25 Mbps	~1.5 V (TTL)	3/1
ISO7241M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7242C	25 Mbps	~1.5 V (TTL)	2/2
ISO7242M	150 Mbps	V_{CC}/ 2 (CMOS)	

9.4 Device Functional Modes

Table 2 lists the ISO724xx functional modes. Table 3 lists the ISO7240CF functional modes.

Table 2. Device Function Table ISO724x(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

Table 3. ISO7240CF Functions Table(1)

V_{CC1}	V_{CC2}	DATA INPUT (IN)	DISABLE INPUT (DISABLE)	FAILSAFE CONTROL (CTRL)	DATA OUTPUT (OUT)
PU	PU	H	L or Open	X	H
PU	PU	L	L or Open	X	L
X	PU	X	H	H or Open	H
X	PU	X	H	L	L
PD	PU	X	X	H or Open	H
PD	PU	X	X	L	L
X	PD	X	X	X	Undetermined

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

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9.4.1 Device I/O Schematics

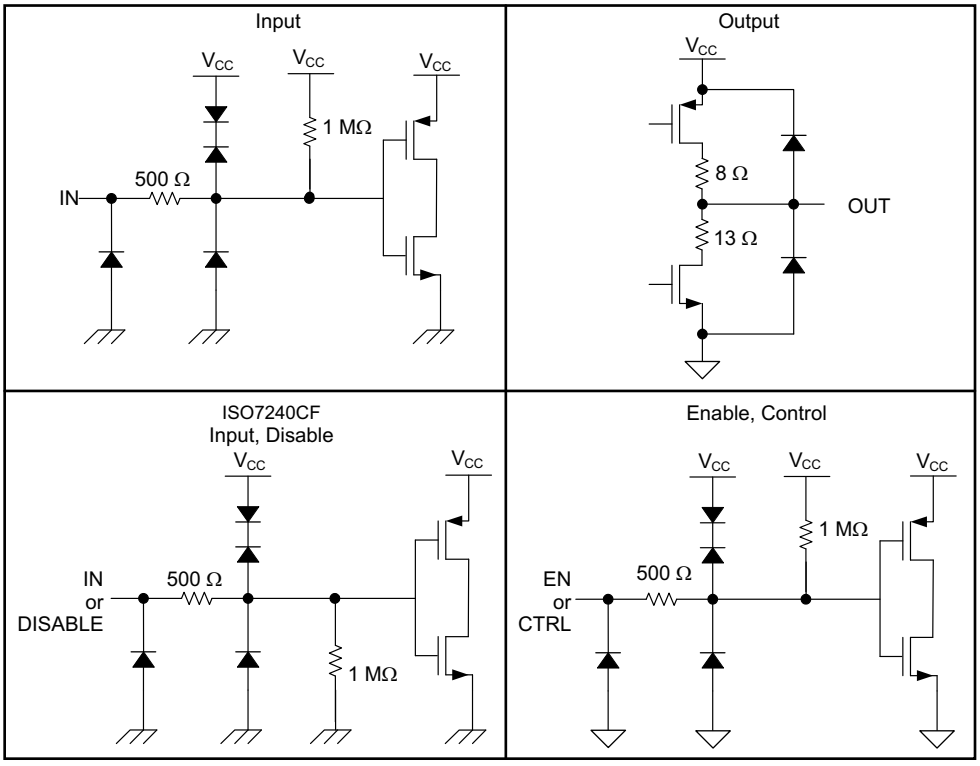

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Figure 18. Device I/O Schematics

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO724xx family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

10.2.1 Isolated Data Acquisition System for Process Control

The ISO724xx family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in Figure 19.

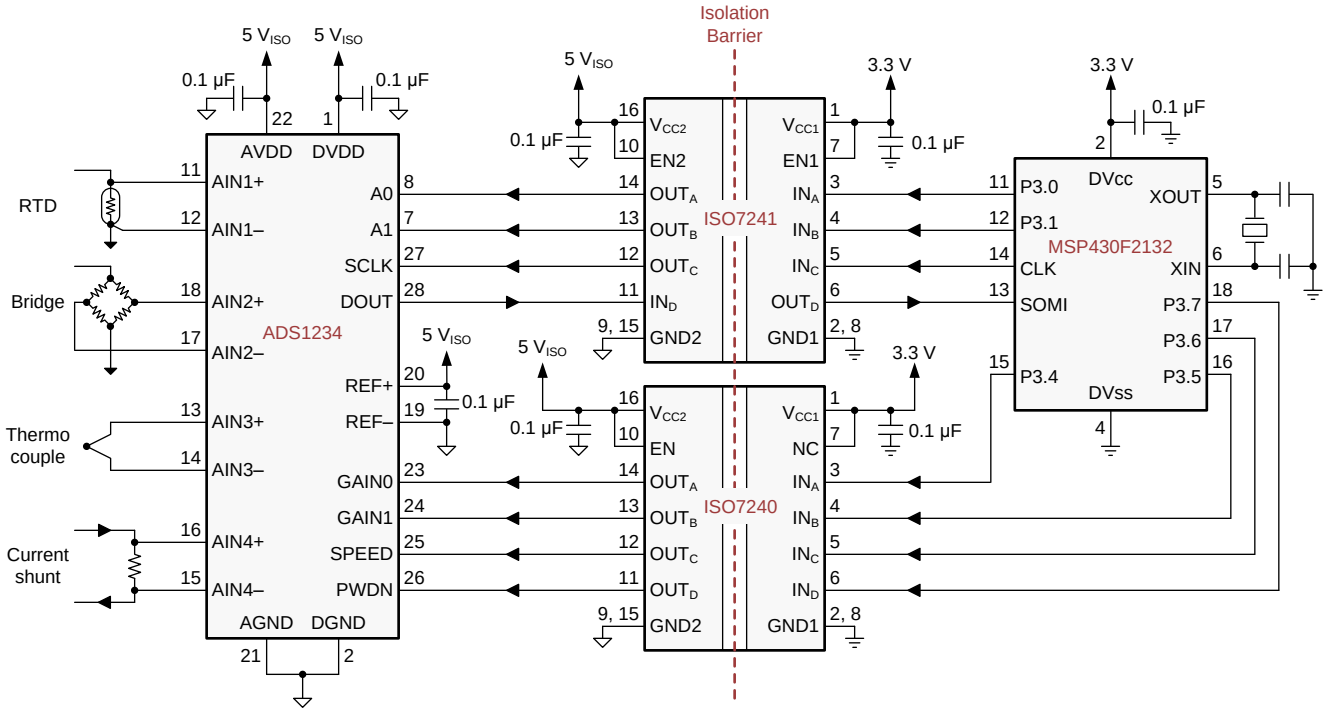

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Figure 19. Isolated Data Acquisition System for Process Control

10.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x family of devices only require two external bypass capacitors to operate.

Typical Application (continued)

10.2.1.2 Detailed Design Procedure

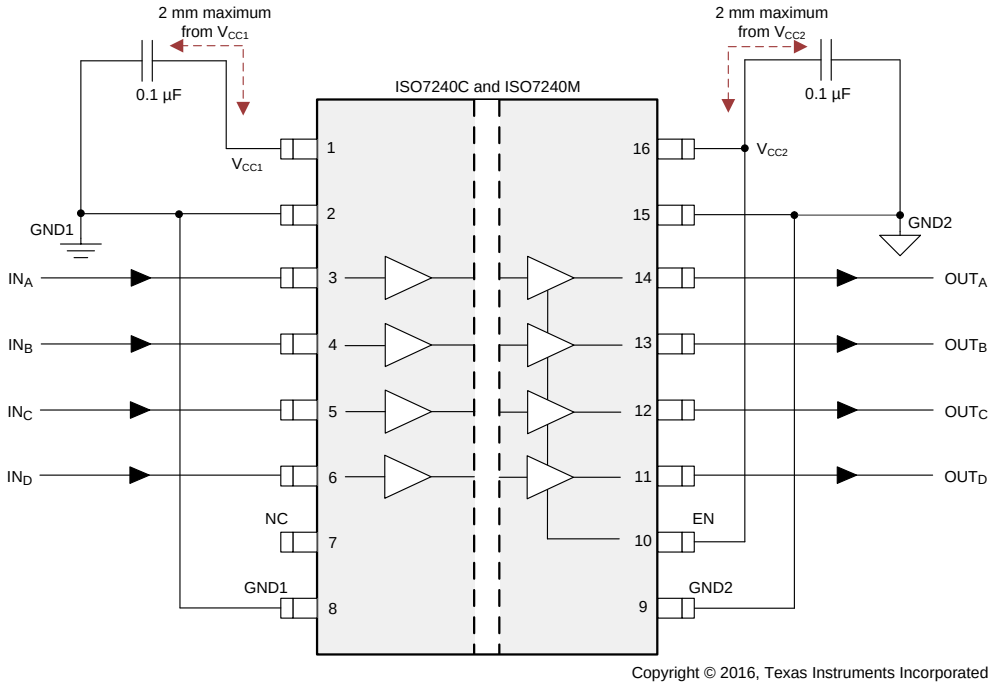

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Figure 20. ISO7240x Typical Circuit Hook-Up

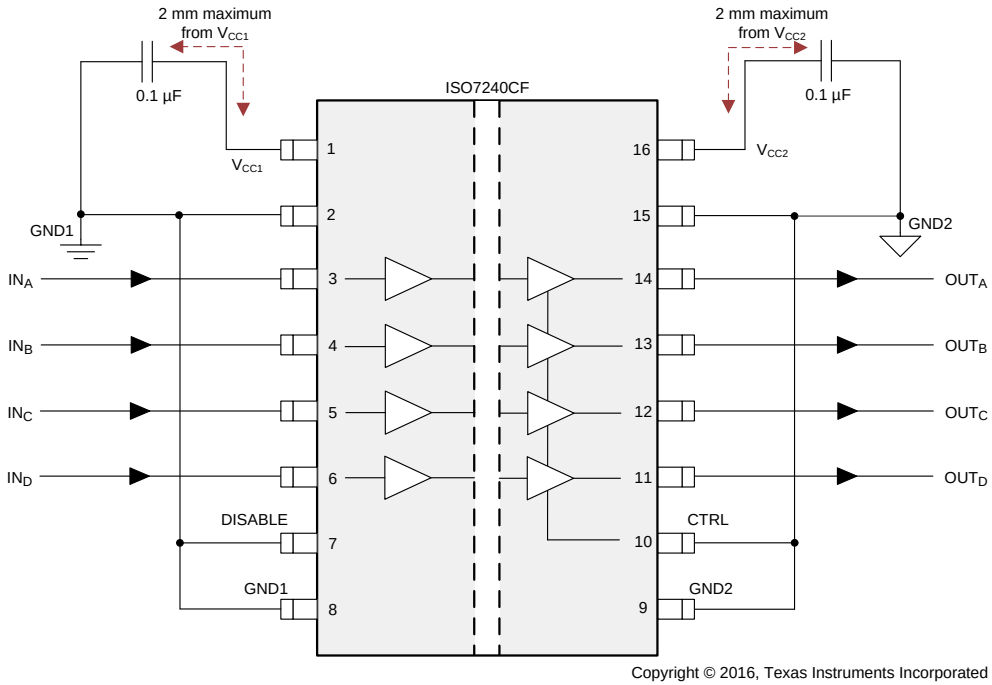

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Figure 21. ISO7240CF Typical Circuit Hook-Up

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Typical Application (continued)

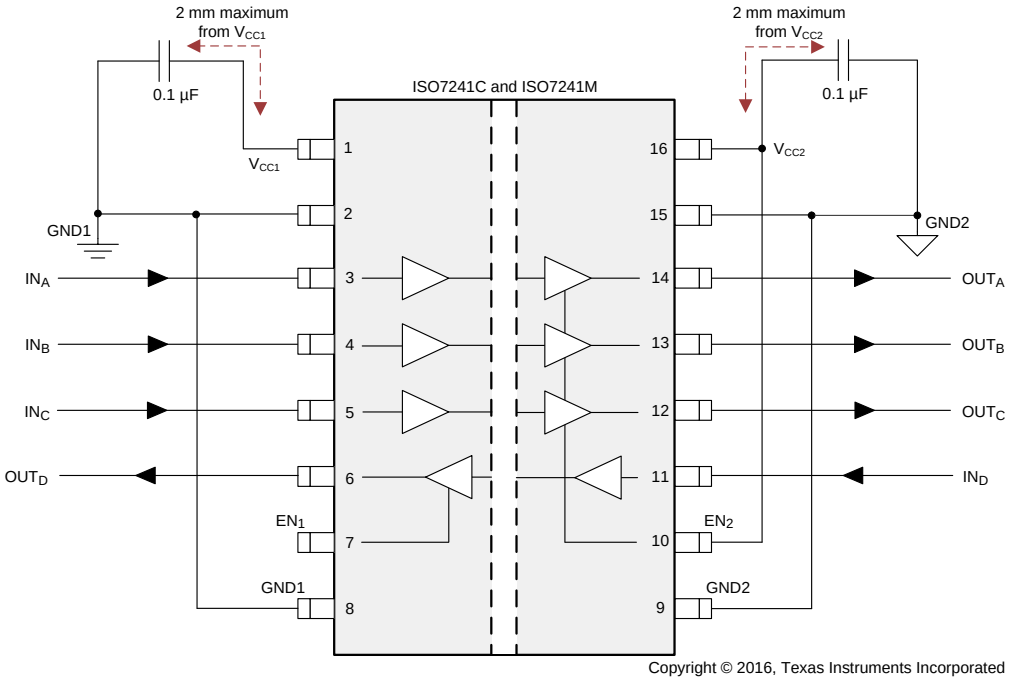

Figure 22. ISO7241x Typical Circuit Hook-Up

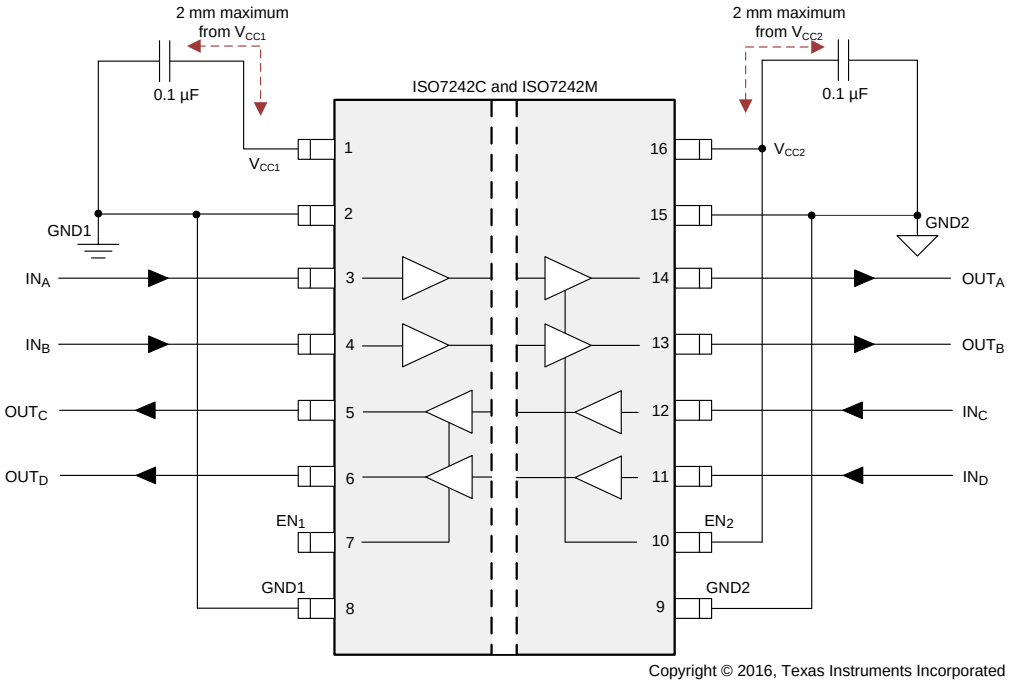

Figure 23. ISO7242x Typical Circuit Hook-Up

Typical Application (continued)

10.2.1.3 Application Curves

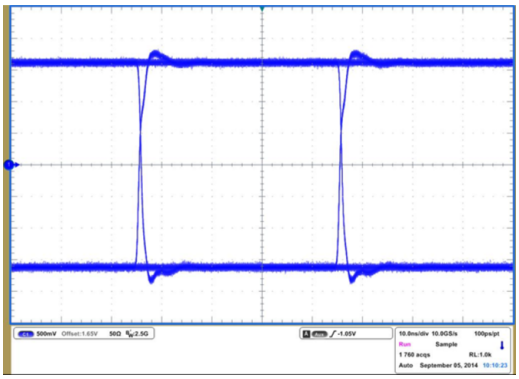

Figure 24. ISO7242M Eye Diagram at 25 Mbps, 3.3 V and 25°C

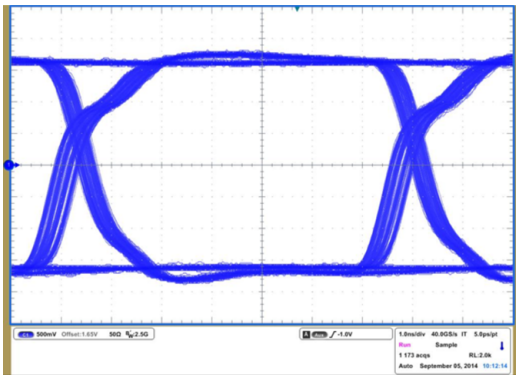

Figure 25. ISO7242M Eye Diagram at 150 Mbps, 3.3 V and 25°C

10.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.

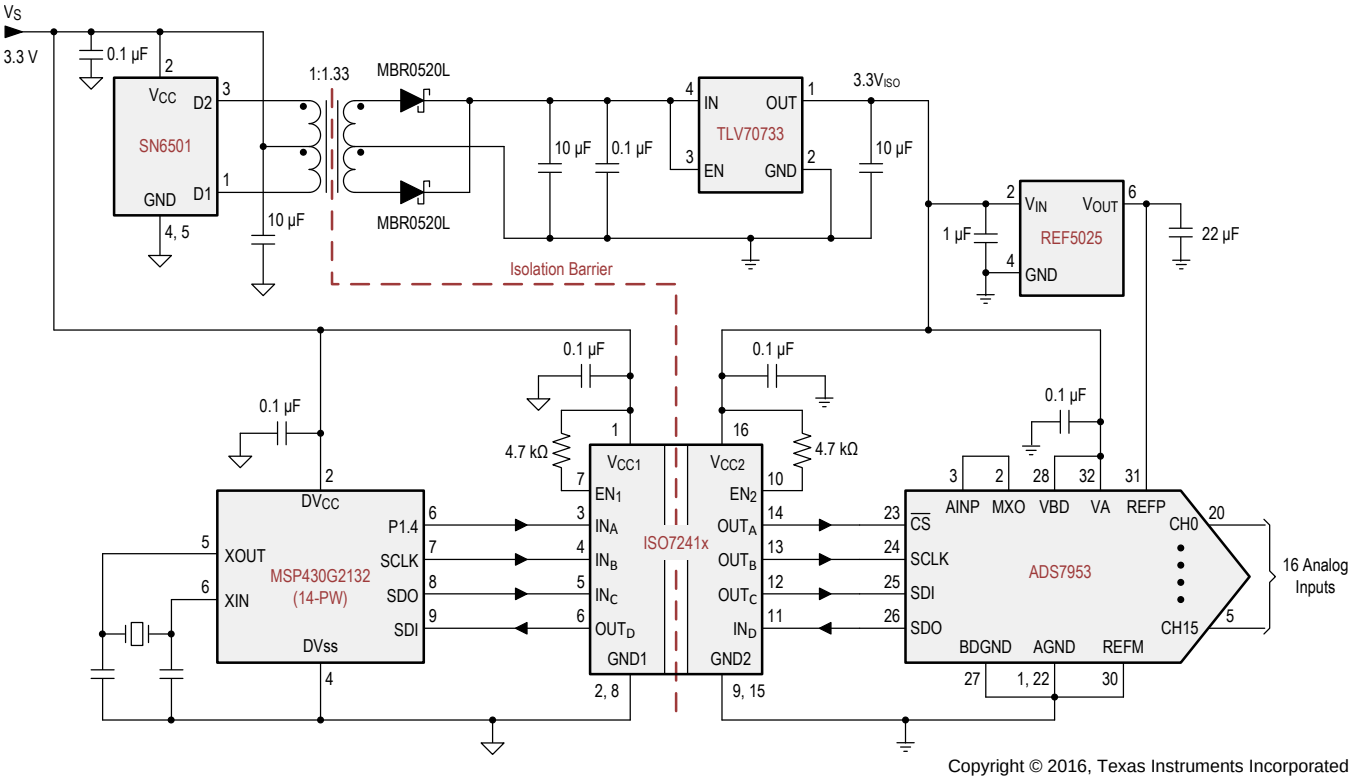

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Figure 26. Isolated SPI for an Analog Input Module With 16 Inputs

10.2.2.1 Design Requirements

See the *Design Requirements* in the *Isolated Data Acquisition System for Process Control* section.

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Typical Application (continued)

10.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure* in the *Isolated Data Acquisition System for Process Control* section..

10.2.2.3 Application Curve

See the *Application Curves* in the *Isolated Data Acquisition System for Process Control* section..

10.2.3 Isolated RS-232 Interface

Figure 27 shows a typical isolated RS-232 interface implementation.

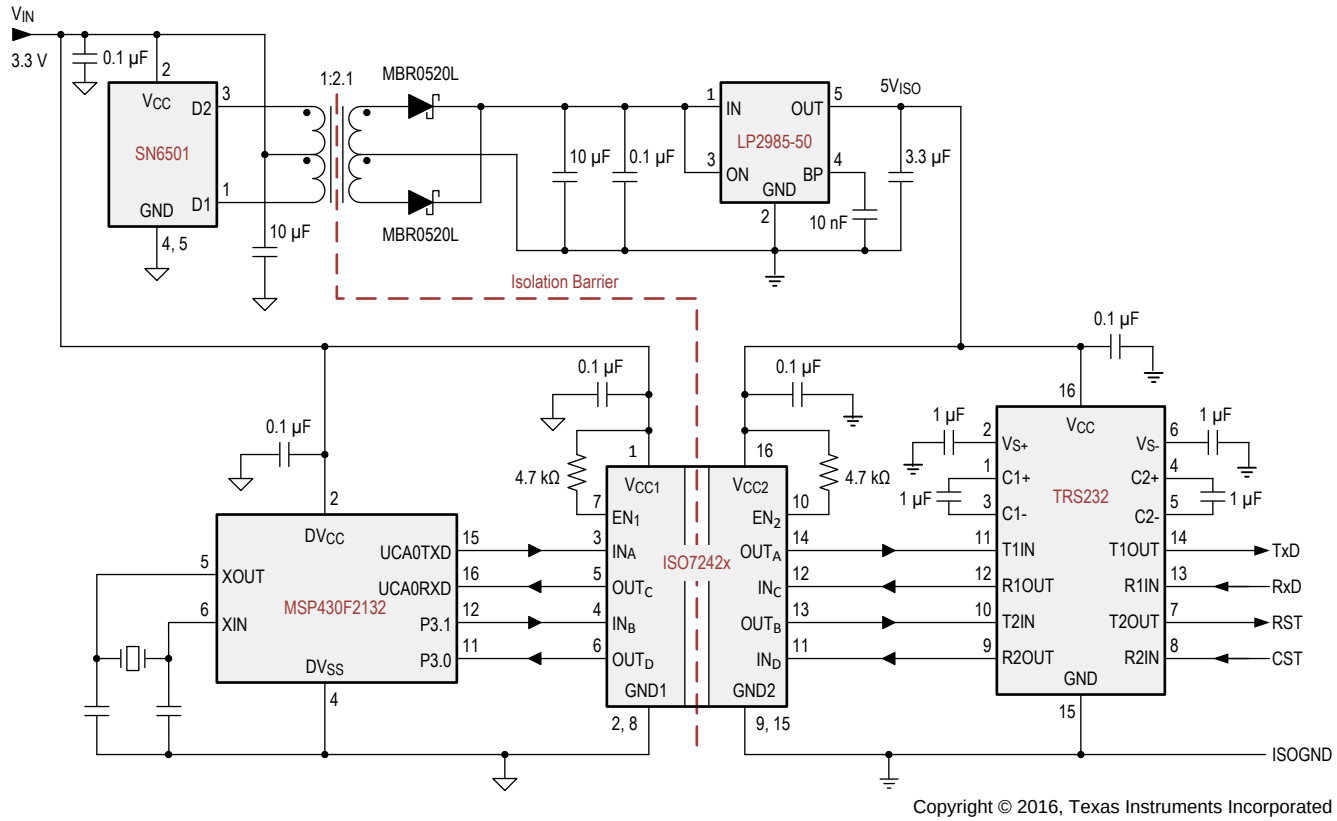

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Figure 27. Isolated RS-232 Interface

10.2.3.1 Design Requirements

See the *Design Requirements* in the *Isolated Data Acquisition System for Process Control* section.

10.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure* in the *Isolated Data Acquisition System for Process Control* section..

10.2.3.3 Application Curve

See the *Application Curves* in the *Isolated Data Acquisition System for Process Control* section..

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 28). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

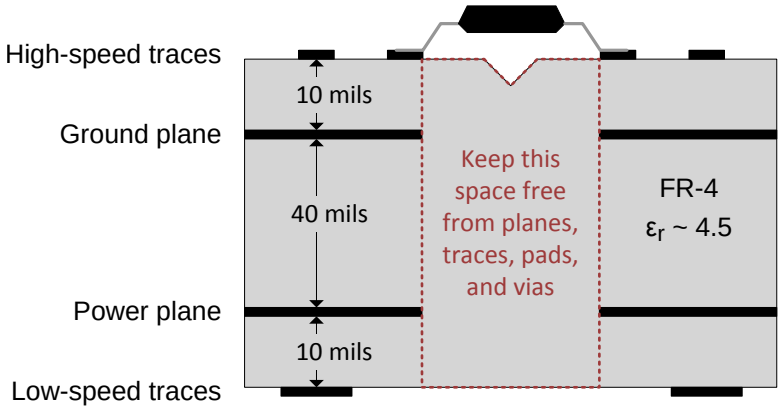

Figure 28. Recommended Layer Stack

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- ADS1234 *24-Bit Analog-to-Digital Converter For Bridge Sensors*
- *ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs*
- *Digital Isolator Design Guide*
- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*
- *ISO72x Digital Isolator Magnetic-Field Immunity*
- *Isolation Glossary*
- *LP2985 150-mA Low-noise Low-dropout Regulator With Shutdown*
- MSP430F2132 *Mixed Signal Microcontroller*
- *MSP430G2x32, MSP430G2x02 Mixed Signal Microcontroller*
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- *SN6501 Transformer Driver for Isolated Power Supplies*
- *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*
- TRS232 *Dual RS-232 Driver/Receiver With IEC61000-4-2 Protection*

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7240CF	Click here	Click here	Click here	Click here	Click here
ISO7240C	Click here	Click here	Click here	Click here	Click here
ISO7240M	Click here	Click here	Click here	Click here	Click here
ISO7241C	Click here	Click here	Click here	Click here	Click here
ISO7241M	Click here	Click here	Click here	Click here	Click here
ISO7242C	Click here	Click here	Click here	Click here	Click here
ISO7242M	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

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13.5 Trademarks (continued)

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CFDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240CF	Samples
ISO7240CFDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240CF	Samples
ISO7240CFDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240CF	Samples
ISO7240MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7240MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7240MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7240MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7241CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7241MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7241MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7241MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7242CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242C	Samples
ISO7242CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242C	Samples
ISO7242CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242C	Samples
ISO7242MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples
ISO7242MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples
ISO7242MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples
ISO7242MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :

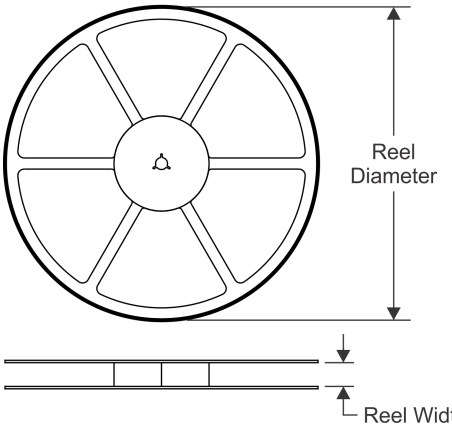
- Automotive: ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1

NOTE: Qualified Version Definitions:

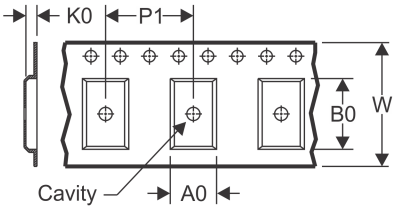
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

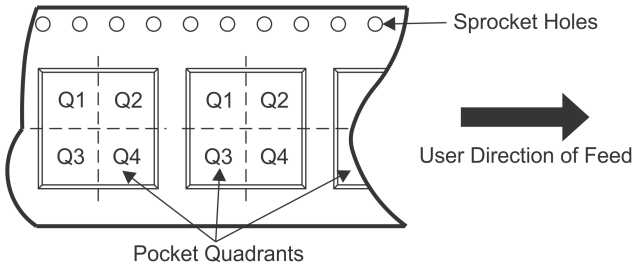


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

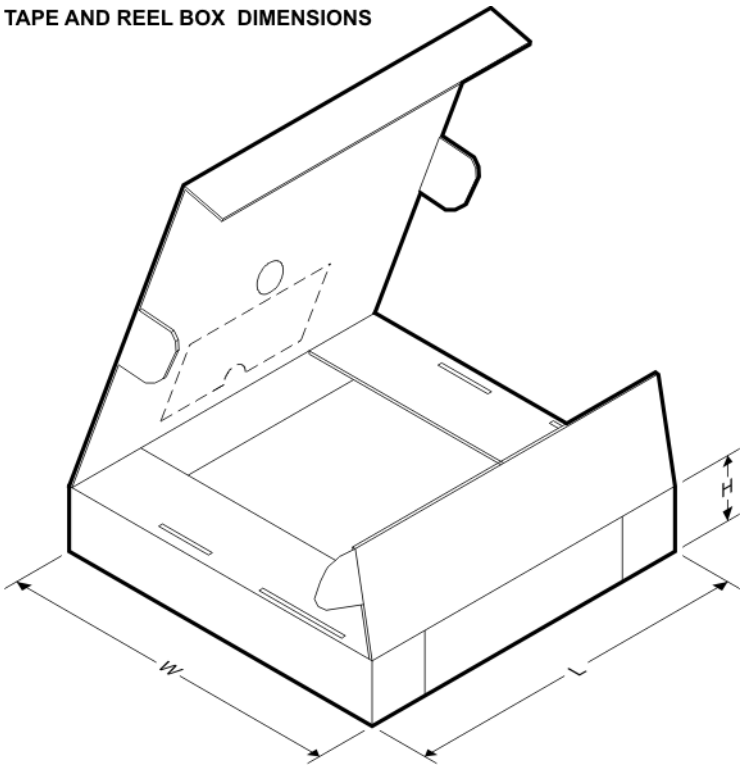
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240CFDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240CFDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

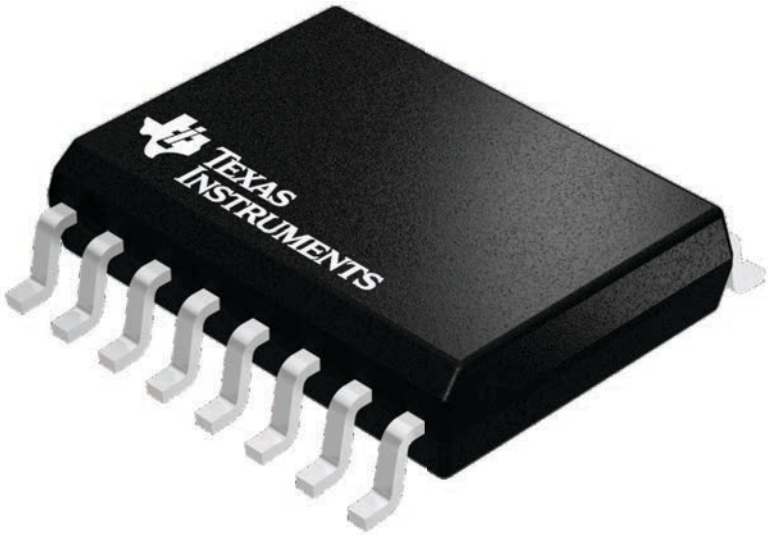
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

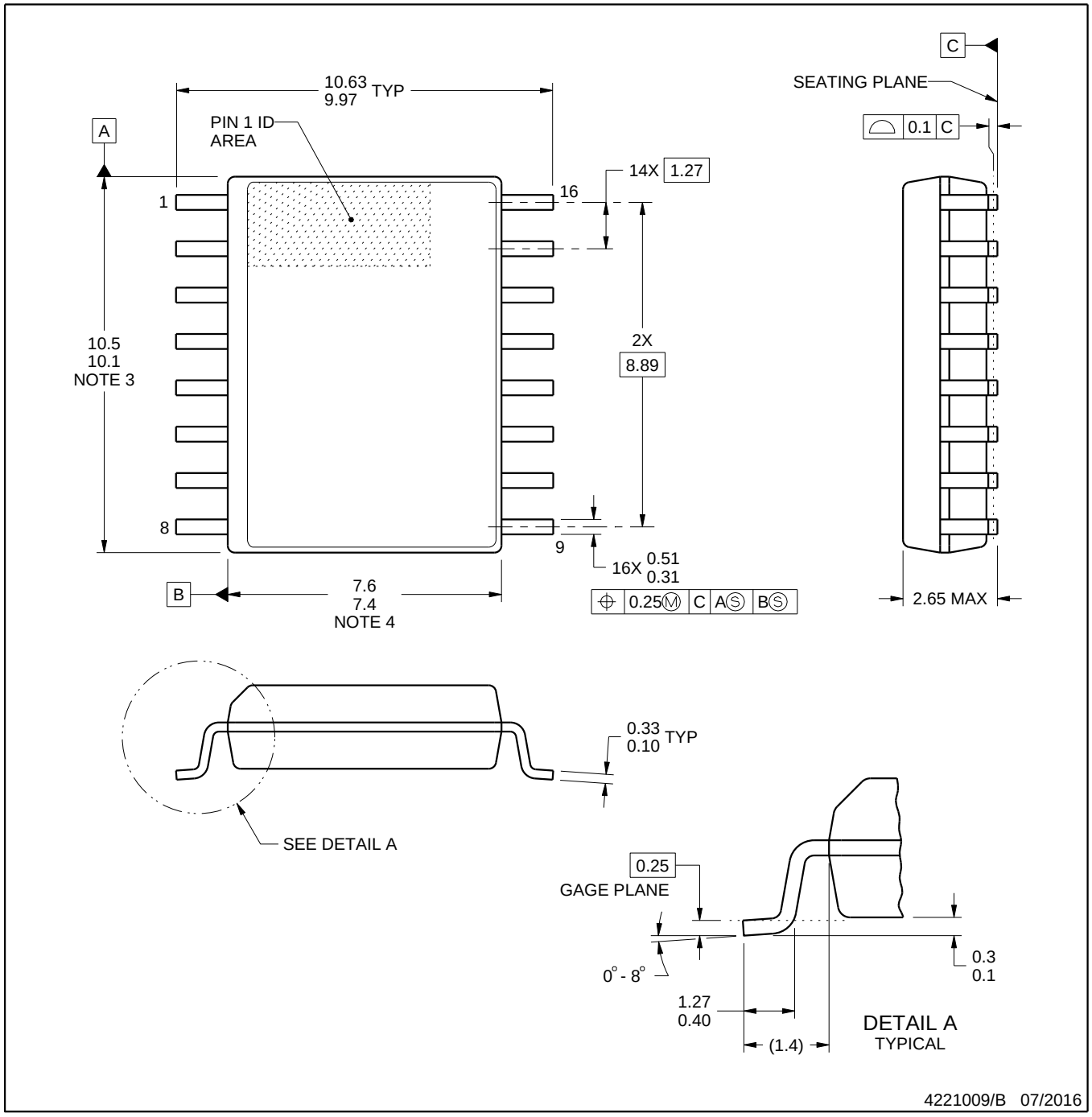
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



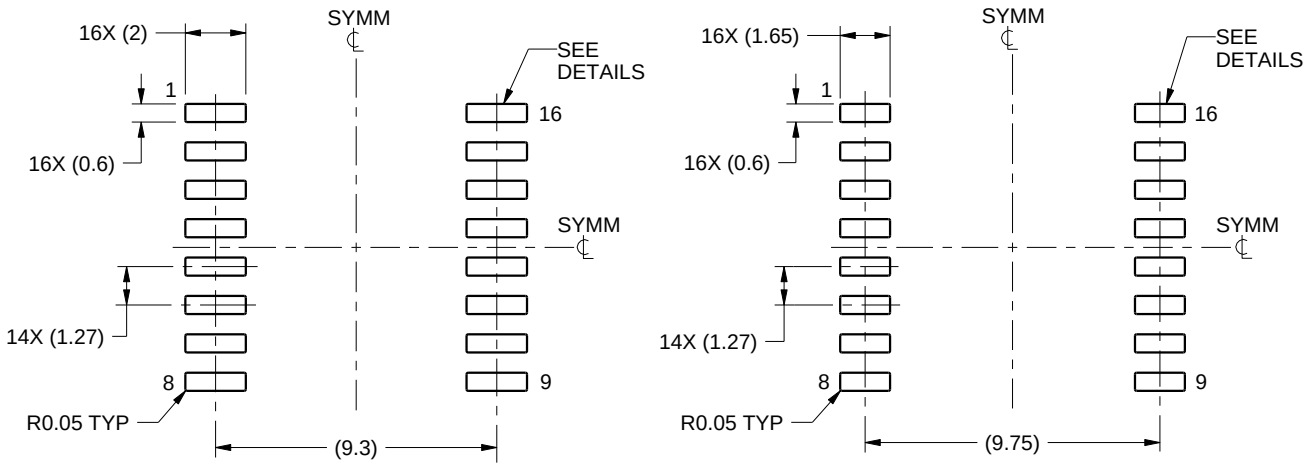
4224780/A

SOIC



NOTES:

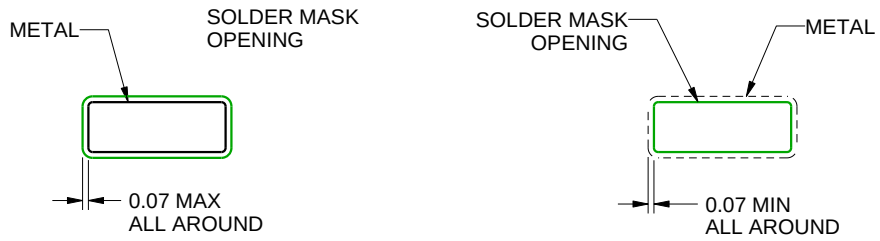
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

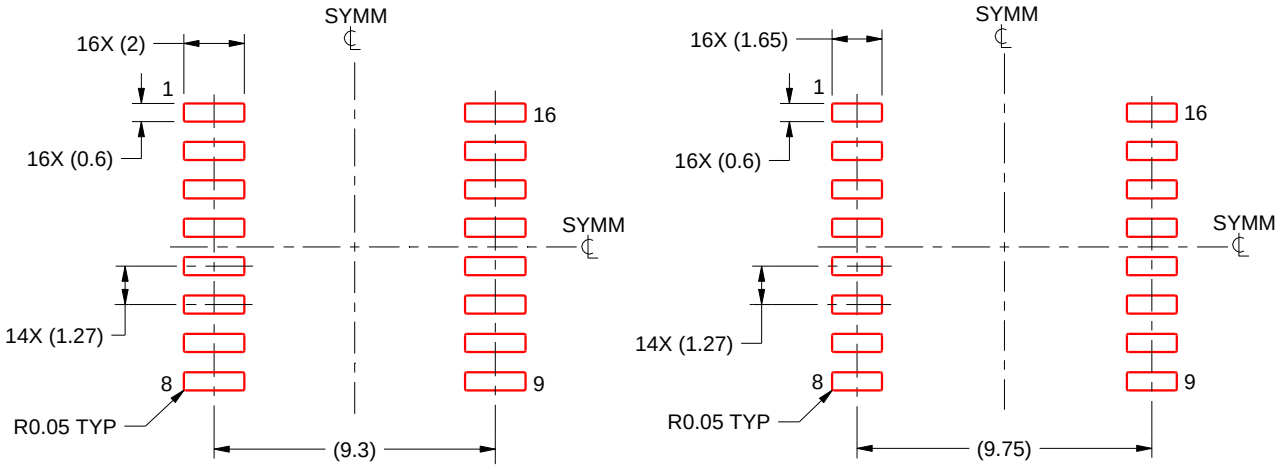
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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