24-Bit, 192-kHz Sampling, Enhanced Multilevel, Delta-Sigma, Audio Digital-to-Analog Converter

FEATURES

- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range: 105 dB Typical
  - SNR: 105 dB Typical
  - THD+N: 0.002% Typical
  - Full-Scale Output: 3.9 V_{PP} Typical
- 4x/8x Oversampling Interpolation Filter:
  - Stop-Band Attenuation: –50 dB
  - Passband Ripple: ±0.04 dB
- Sampling Frequency: 5 kHz to 200 kHz
- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, or 1152 f_S with Autodetect
- Zero Flags for Selectable Channel Combinations
- Serial Port (SPI™/I^2C™) for Mode Control
- User-Programmable Functions:
  - Flexible Audio Data Formats
    - Right-Justified, I^2S™, and Left-Justified
    - 16-, 18-, 20-, and 24-Bit Audio Data
  - Digital Attenuation: Mode Selectable
    - 0 dB to –63 dB, 0.5-dB/step
    - 0 dB to –100 dB, 1-dB/step
  - Soft Mute
  - Digital De-Emphasis
  - Digital Filter Roll-Off: Sharp or Slow
- Single Power-Supply Operation: 5-V Analog, 5-V Digital
- Package: SSOP-28 (150 mil)
- Pin-Compatible with PCM1780

APPLICATIONS

- Integrated A/V Receivers
- DVD Movie and Audio Players
- HDTV Receivers
- Car Audio Systems
- DVD Add-On Cards for High-End PCs
- Digital Audio Workstations
- Other Multichannel Audio Systems

DESCRIPTION

The PCM1680 is a CMOS, monolithic integrated circuit which features eight 24-bit audio digital-to-analog converters (DACs) and support circuitry in a small SSOP-28. The DACs use TI's enhanced multilevel delta-sigma (ΔΣ) architecture to achieve excellent signal-to-noise performance and a high tolerance to clock jitter.

The PCM1680 accepts industry-standard audio data formats with 16-bit to 24-bit audio data. Sampling rates up to 200 kHz are supported. The PCM1680 provides a full set of user-programmable functions through a serial control port, using an SPI or I^2C interface.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	PCM1680	UNIT
Supply voltage: $V_{CC}1$, $V_{CC}2$, V_{DD}	–0.3 to 6.5	V
Supply voltage differences: $V_{CC}1$, $V_{CC}2$, V_{DD}	±0.1	V
Ground voltage differences: AGND1, AGND2, DGND	±0.1	V
Input voltage to digital pins	–0.3 to V_{DD} + 0.3, < 6.5	V
Input voltage to analog pins	–0.3 to V_{CC} + 0.3, < 6.5	V
Input current (all pins except supplies)	±10	mA
Operating temperature	–40 to +110	°C
Storage temperature	–55 to +150	°C
Junction temperature	+150	°C
Lead temperature (soldering, 5 seconds)	+260	°C
Package temperature (IR reflow, peak)	+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range.

		MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC}1$, $V_{CC}2$		4.75	5	5.25	V
Digital supply voltage, V_{DD}		4.75	5	5.25	V
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		36.864	MHz
	Sampling clock	32		192	kHz
Analog output load resistance		5			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		+70	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{CC} = V_{DD} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				24		Bits
DATA FORMAT						
	Audio data interface format			Right-justified, I^2S, left-justified		
	Audio data bit length			16-, 18-, 20-, or 24-bits, selectable		
	Audio data format			MSB-first, twos complement		
f_S	Sampling frequency		5		200	kHz
	System clock frequency			128, 192, 256, 384, 512, 768, 1152 f_S		

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{CC} = V_{DD} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Logic family			TTL-compatible		
V_{IH}	Input logic level		2			V_{DC}
V_{IL}					0.8	
I_{IH} (1)	Input logic current	V_{IN} = V_{CC}			10	µA
I_{IL} (1)		V_{IN} = 0 V			–10	
I_{IH} (2)		V_{IN} = V_{CC}		65	100	
I_{IL} (2)		V_{IN} = 0 V			–10	
V_{OH} (3)	Output logic level	I_{OH} = –1 mA	2.4			V_{DC}
V_{OL} (4)		I_{OL} = 1 mA			0.4	
DYNAMIC PERFORMANCE (5)						
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 48 kHz		0.002	0.008	%
		V_{OUT} = 0 dB, f_S = 96 kHz, system clock = 256 f_S		0.003		
		V_{OUT} = 0 dB, f_S = 192 kHz, system clock = 128 f_S		0.004		
	Dynamic range	EIAJ, A-weighted, f_S = 48 kHz	100	105		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		103		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		102		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 48 kHz	100	105		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		103		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		102		
	Channel separation	f_S = 48 kHz	94	103		dB
		f_S = 96 kHz, system clock = 256 f_S		101		
		f_S = 192 kHz, system clock = 128 f_S		100		
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±6	% of FSR
	Bipolar zero error	V_{OUT} = 0.486 V_{CC} at BPZ input		±30	±80	mV
ANALOG OUTPUT						
	Output voltage	Full-scale (–0 dB)		0.78 V_{CC}		V_{PP}
	Bipolar zero voltage			0.486 V_{CC}		V_{DC}
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE						
Filter Characteristics (Sharp Roll-Off)						
	Passband	±0.04 dB			0.454	f_S
	Stop band		0.546			f_S
	Passband ripple				±0.04	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–50			dB

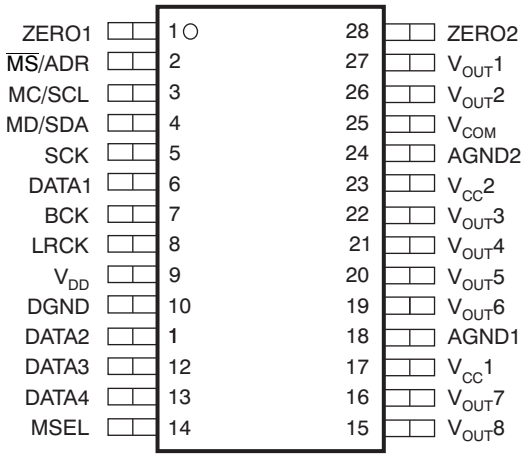
(1) Pins 5, 6, 7, 8, 11, 12, 13: SCK, DATA1, BCK, LRCK, DATA2, DATA3, DATA4.
(2) Pins 2, 3, 4, 14: $\overline{MS}$/ADR, MC/SCL, MD/SDA, MSEL.
(3) Pins 1, 28: ZERO1, ZERO2.
(4) Pins 1, 4, 28: ZERO1, MD/SDA, ZERO2.
(5) Analog performance characteristics are measured using the System Two™ Cascade audio measurement system by Audio Precision™.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{CC} = V_{DD} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER PERFORMANCE (continued)						
Filter Characteristics (Slow Roll-Off)						
	Passband	±0.5 dB			0.198	f_S
	Stop band		0.884			f_S
	Passband ripple				±0.5	dB
	Stop-band attenuation	Stop band = 0.884 f_S	–35			dB
	Delay time			20/f_S		
	De-emphasis error			±0.1		dB
ANALOG FILTER PERFORMANCE						
	Frequency response	at 20 kHz		–0.02		dB
		at 44 kHz		–0.07		
POWER-SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		4.75	5	5.25	V_{DC}
V_{CC}			4.75	5	5.25	
I_{DD} + I_{CC}	Supply current	f_S = 48 kHz		91	110	mA
		f_S = 96 kHz, system clock = 256 f_S		102		
		f_S = 192 kHz, system clock = 128 f_S		106		
	Power dissipation	f_S = 48 kHz		455	605	mW
		f_S = 96 kHz, system clock = 256 f_S		510		
		f_S = 192 kHz, system clock = 128 f_S		530		
TEMPERATURE RANGE						
	Operating temperature		–25		+70	°C
θ_{JA}	Thermal resistance			70		°C/W

DBQ PACKAGE
SSOP-28, QSOP-28
(TOP VIEW)

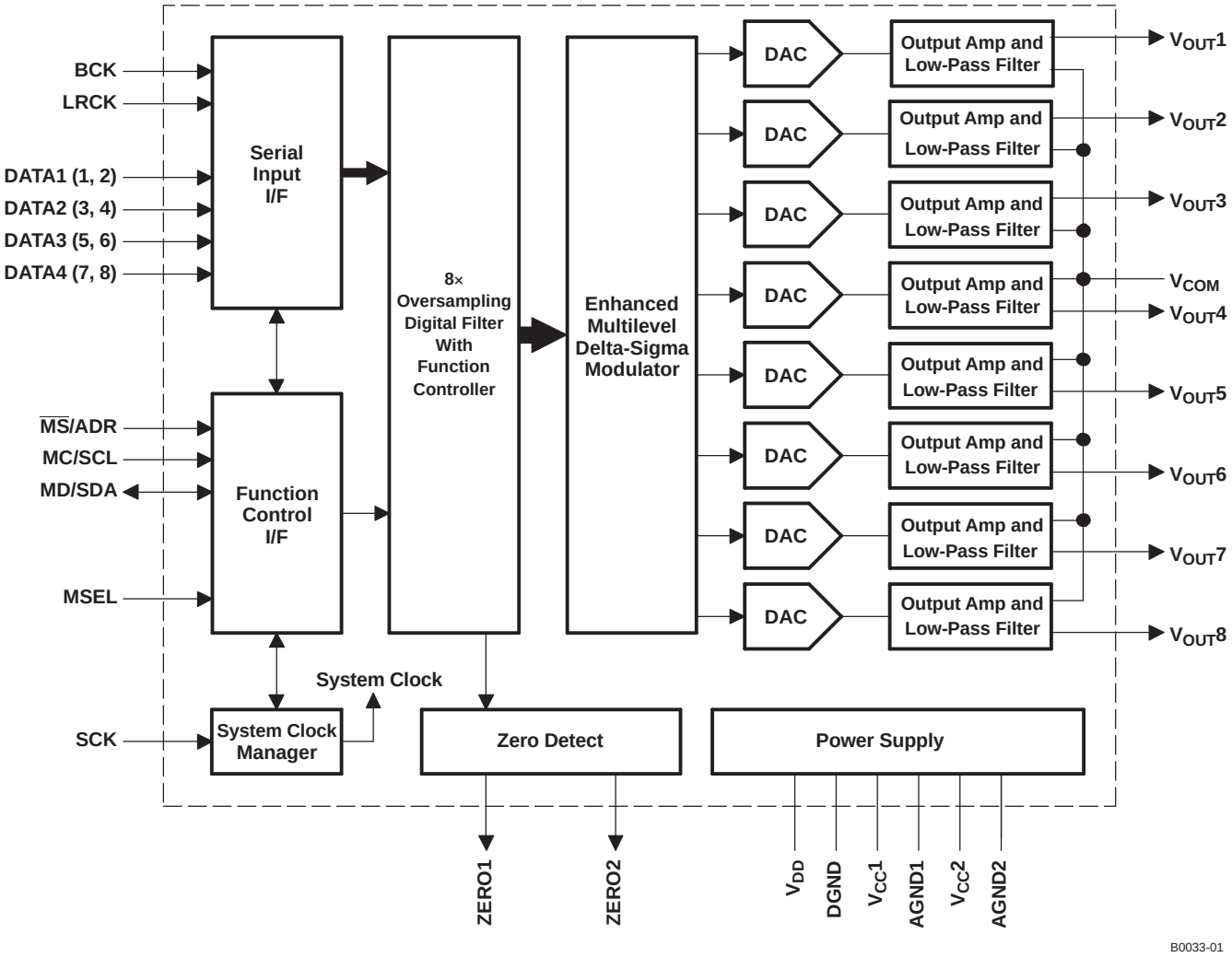


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	18	–	Analog ground
AGND2	24	–	Analog ground
BCK	7	I	Shift clock input for serial audio data(1)
DATA1	6	I	Serial audio data input for $V_{OUT}1$ and $V_{OUT}2$(1)
DATA2	11	I	Serial audio data input for $V_{OUT}3$ and $V_{OUT}4$(1)
DATA3	12	I	Serial audio data input for $V_{OUT}5$ and $V_{OUT}6$(1)
DATA4	13	I	Serial audio data input for $V_{OUT}7$ and $V_{OUT}8$(1)
DGND	10	–	Digital ground
LRCK	8	I	Left and right clock input. The frequency of this clock is equal to the sampling rate, f_S.(1)
MC/SCL	3	I	Shift clock input for SPI, serial clock input for I^2C(1)(2)
MD/SDA	4	I/O	Serial data input for SPI, serial data input/output for I^2C(1)(2)(3)
$\overline{MS}$/ADR	2	I	Select input for SPI, address input for I^2C(1)(4)
MSEL	14	I	$I^2C/\overline{SPI}$ select(1)(4)
SCK	5	I	System clock input. Input frequency is 128, 192, 256, 384, 512, 768, or 1152 f_S.(1)
$V_{CC}1$	17	–	Analog power supply, 5 V
$V_{CC}2$	23	–	Analog power supply, 5 V
V_{COM}	25	–	Common voltage output. This pin should be bypassed with a 10-μF capacitor to AGND.
V_{DD}	9	–	Digital power supply, 5 V
$V_{OUT}1$	27	O	Voltage output for audio signal corresponding to L-ch on DATA1
$V_{OUT}2$	26	O	Voltage output for audio signal corresponding to R-ch on DATA1
$V_{OUT}3$	22	O	Voltage output for audio signal corresponding to L-ch on DATA2
$V_{OUT}4$	21	O	Voltage output for audio signal corresponding to R-ch on DATA2
$V_{OUT}5$	20	O	Voltage output for audio signal corresponding to L-ch on DATA3
$V_{OUT}6$	19	O	Voltage output for audio signal corresponding to R-ch on DATA3
$V_{OUT}7$	16	O	Voltage output for audio signal corresponding to L-ch on DATA4
$V_{OUT}8$	15	O	Voltage output for audio signal corresponding to R-ch on DATA4
ZERO1	1	O	Zero-flag output 1
ZERO2	28	O	Zero-flag output 2

(1) Schmitt-trigger input.
(2) Pull-down in SPI mode.
(3) Open-drain output in I^2C mode.
(4) Pull-down.

Functional Block Diagram



TYPICAL CHARACTERISTICS: DIGITAL FILTER (DE-EMPHASIS OFF)

All specifications at T_A = +25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

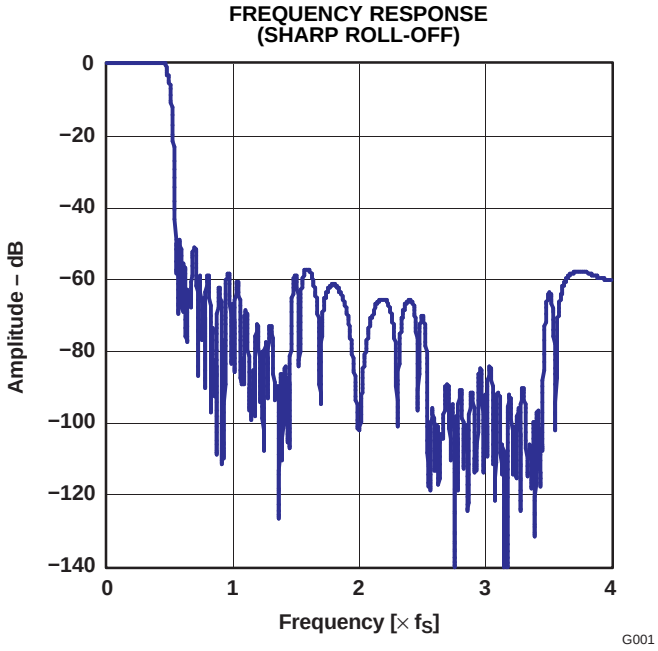


Figure 1.

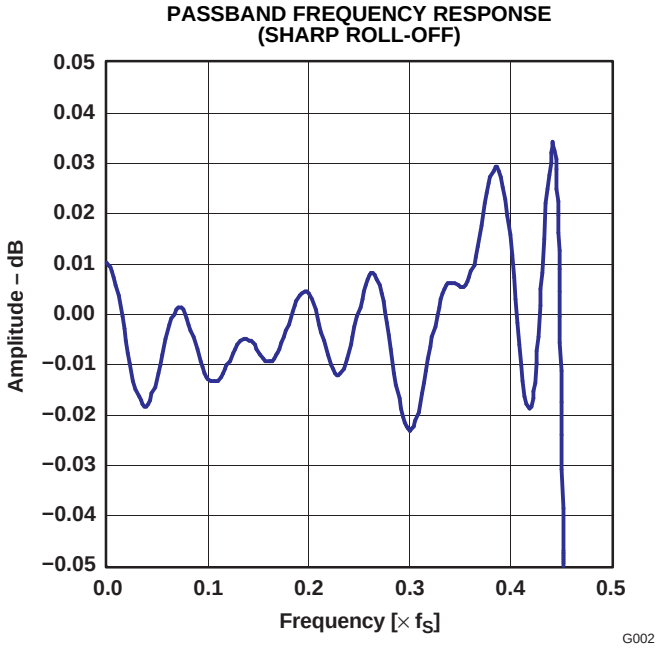


Figure 2.

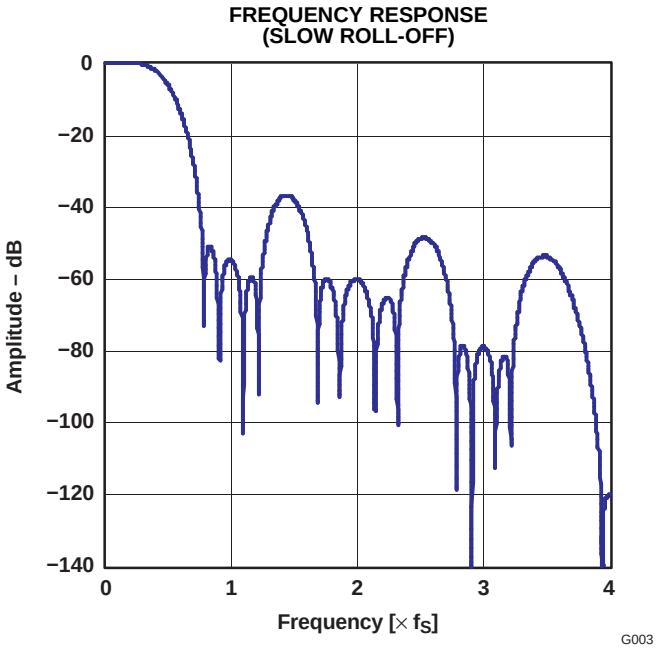


Figure 3.

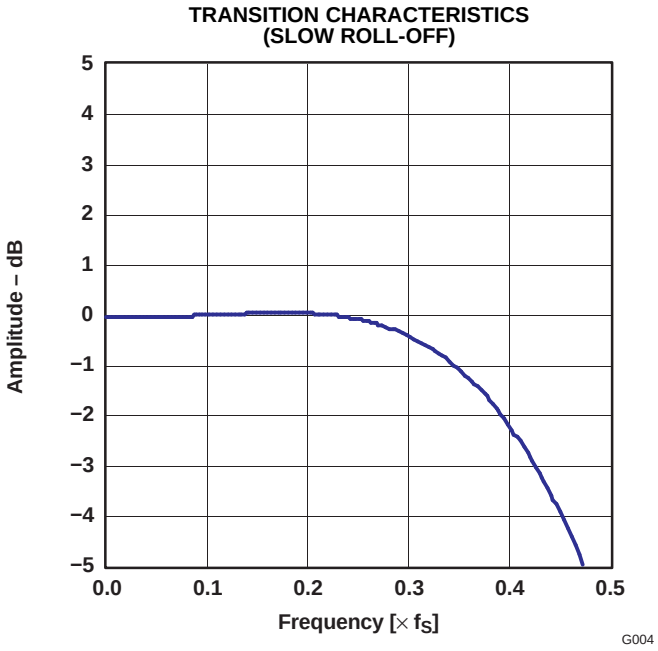


Figure 4.

TYPICAL CHARACTERISTICS: DE-EMPHASIS FILTER

All specifications at T_A = +25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

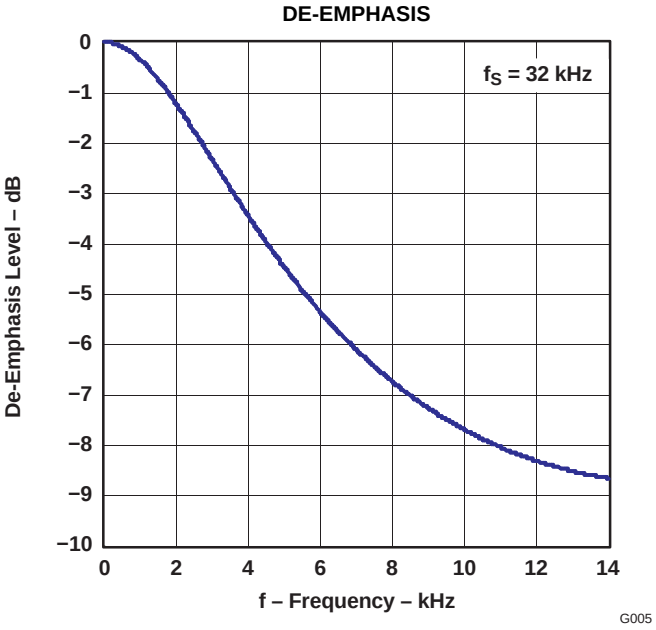


Figure 5.

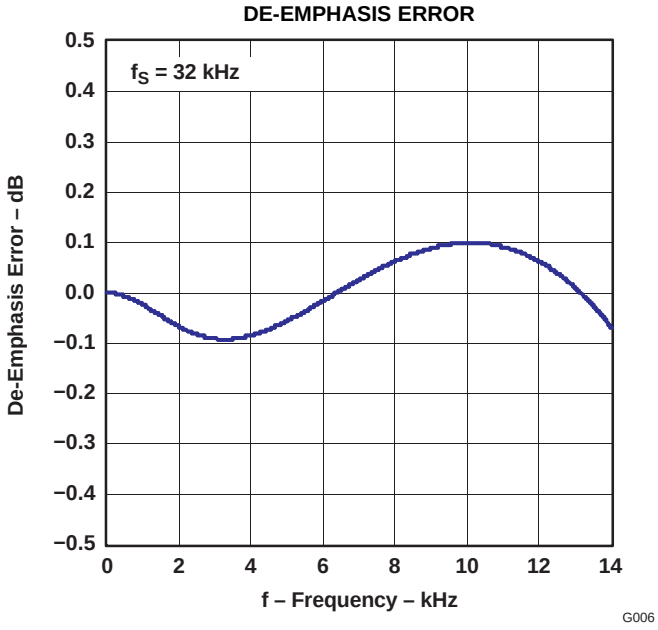


Figure 6.

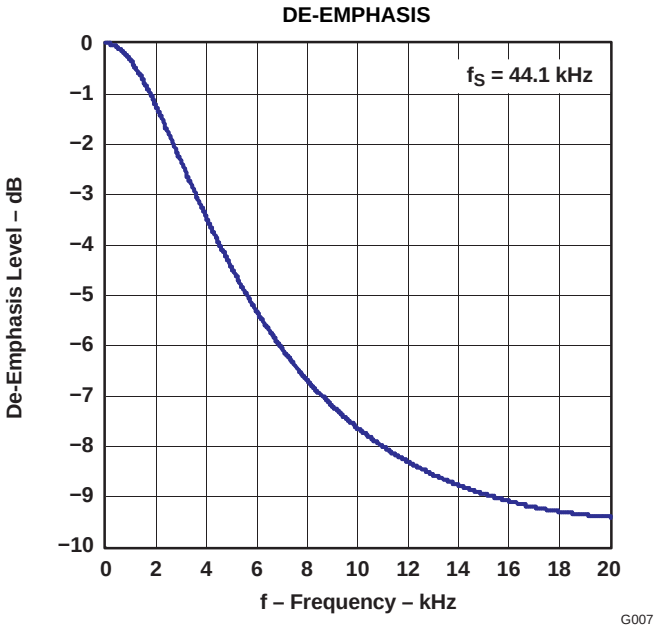


Figure 7.

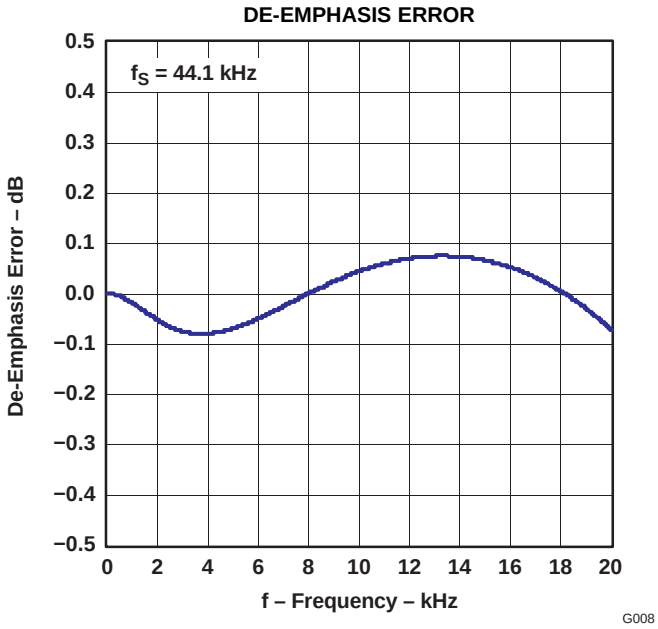


Figure 8.

TYPICAL CHARACTERISTICS: DE-EMPHASIS FILTER (continued)

All specifications at T_A = +25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

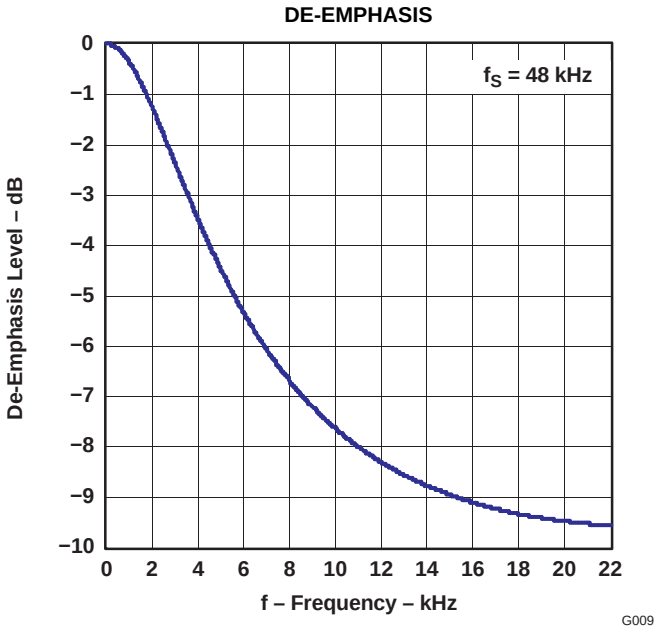


Figure 9.

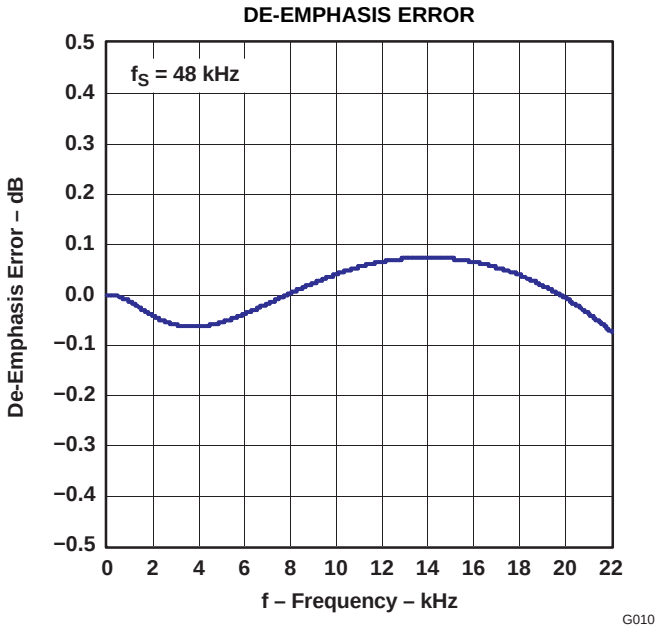


Figure 10.

TYPICAL CHARACTERISTICS: ANALOG FILTER

All specifications at T_A = 25C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

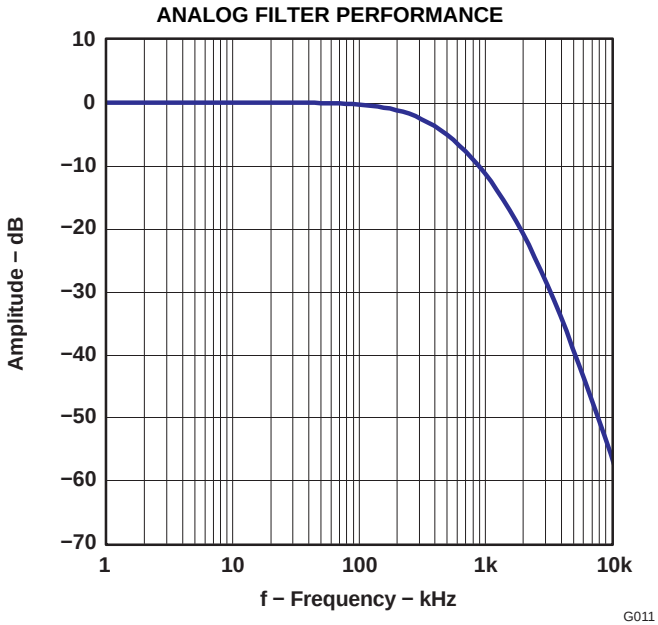


Figure 11.

TYPICAL CHARACTERISTICS: ANALOG DYNAMIC PERFORMANCE

All specifications at T_A = 25C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

Supply Voltage Characteristics

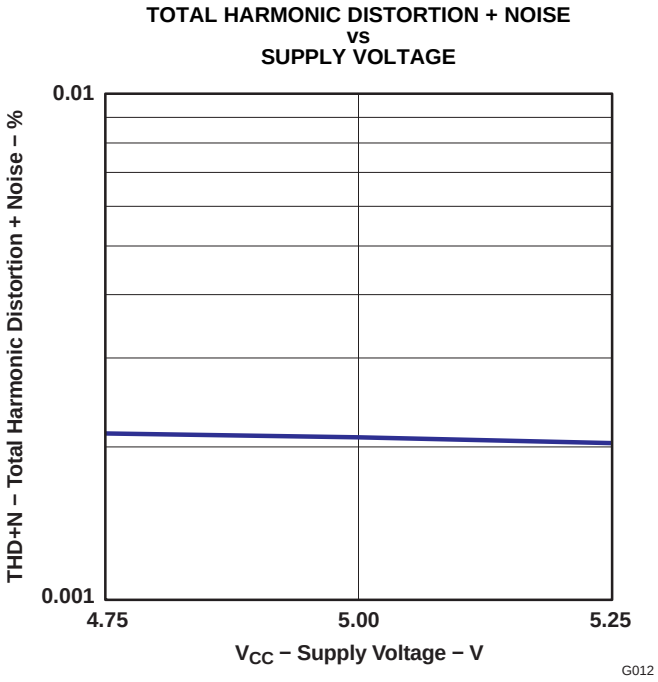


Figure 12.

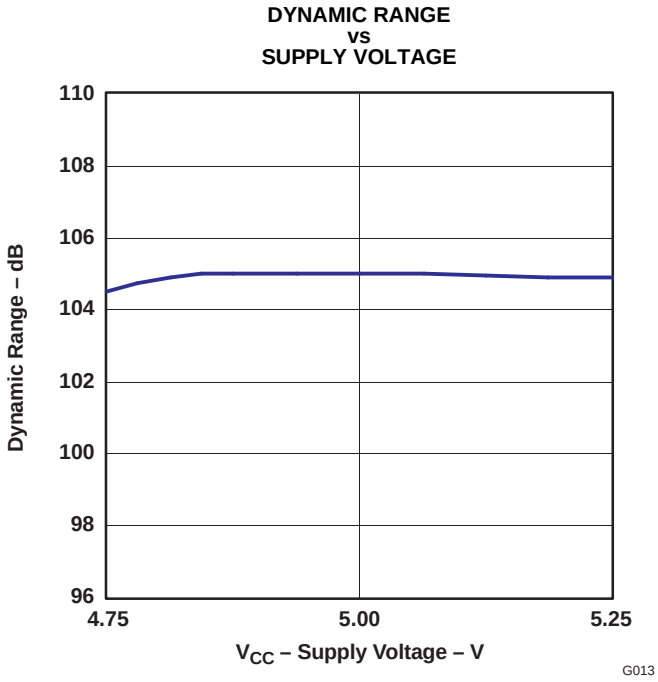


Figure 13.

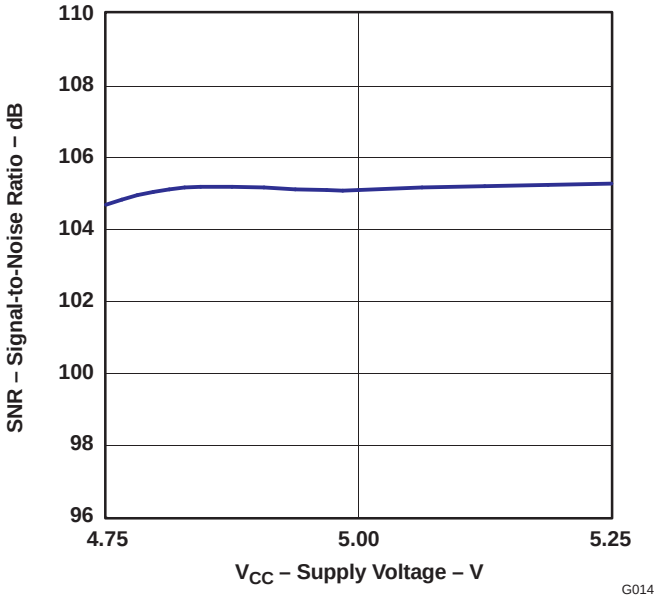


Figure 14.

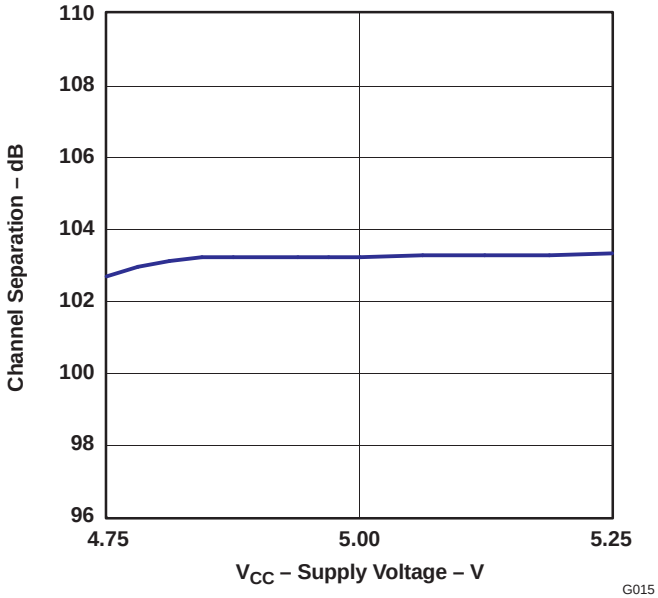


Figure 15.

TYPICAL CHARACTERISTICS: ANALOG DYNAMIC PERFORMANCE (continued)

All specifications at T_A = 25C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

Temperature Characteristics

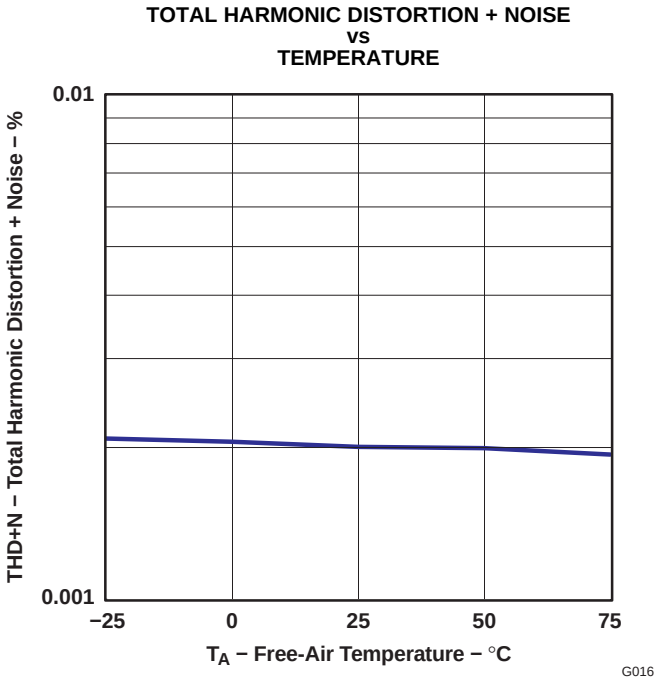


Figure 16.

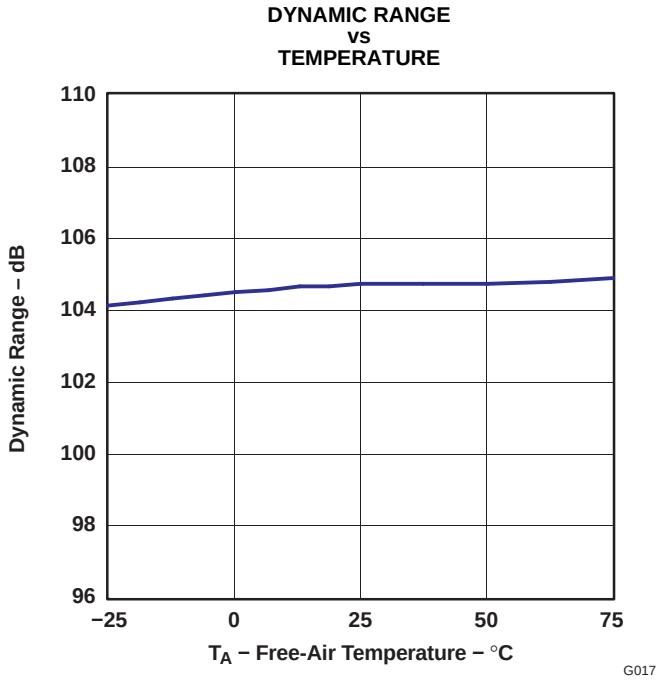


Figure 17.

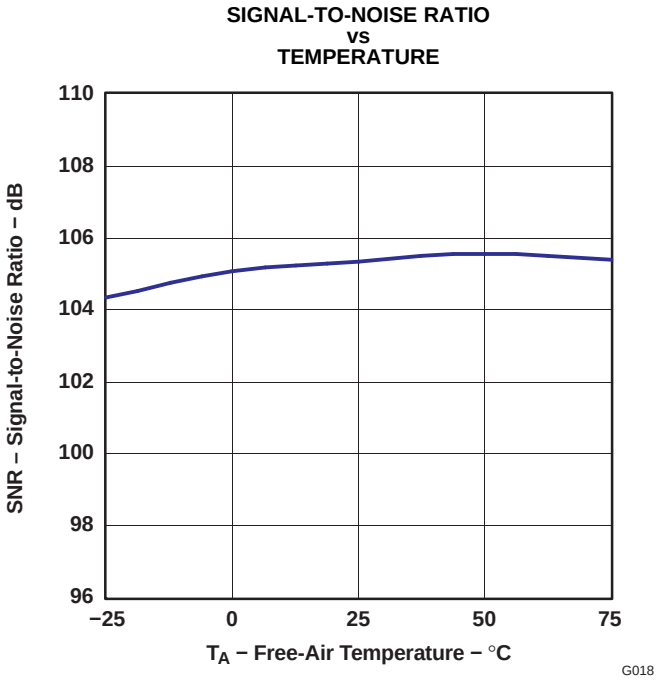


Figure 18.

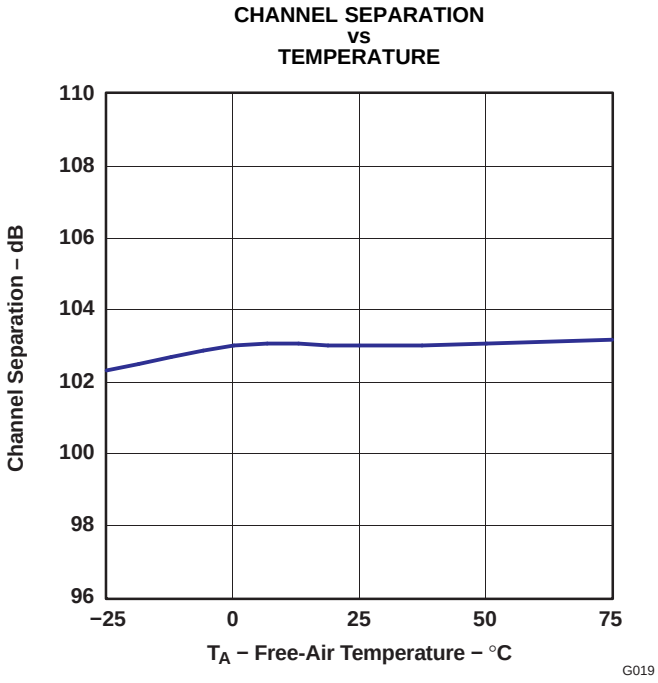


Figure 19.

SYSTEM CLOCK INPUT

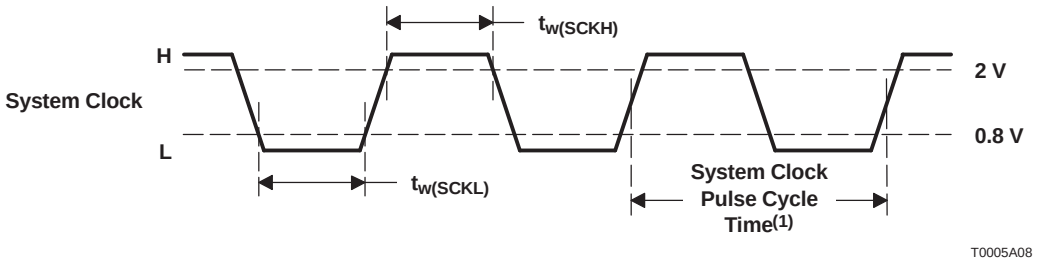
The PCM1680 requires a system clock for operating the digital interpolation filters and multilevel ΔΣ modulators. The system clock is applied at the SCK (pin 5) input. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 20 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Texas Instruments' PLL170x multi-clock generator is an excellent choice for providing the PCM1680 system clock source.

Table 1. System Clock Frequencies for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCK}), MHz						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	—(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	—(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	—(1)	—(1)	—(1)
96 kHz	12.288	18.432	24.576	36.864	—(1)	—(1)	—(1)
192 kHz	24.576	36.864	—(1)	—(1)	—(1)	—(1)	—(1)

(1) This system clock frequency is not supported for the given sampling frequency.



(1) 1/128 f_S, 1/192 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S.

PARAMETER		MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	7		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	7		ns

Figure 20. System Clock Timing

POWER-ON-RESET FUNCTION

The PCM1680 includes a power-on-reset function. Figure 21 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on-reset function is enabled. The initialization sequence requires 3072 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V). After the initialization period, the PCM1680 is set to its reset default state, as described in the *Mode Control Registers* section of this data sheet.

During the reset period (3072 system clocks), the analog output is forced to the common voltage (V_{COM}), or V_{CC}/2. After the reset period, the internal registers are initialized in the next 1/f_S period and if SCK, BCK, and LRCK are provided continuously, the PCM1680 provides the proper analog output with group delay corresponding to the input data.

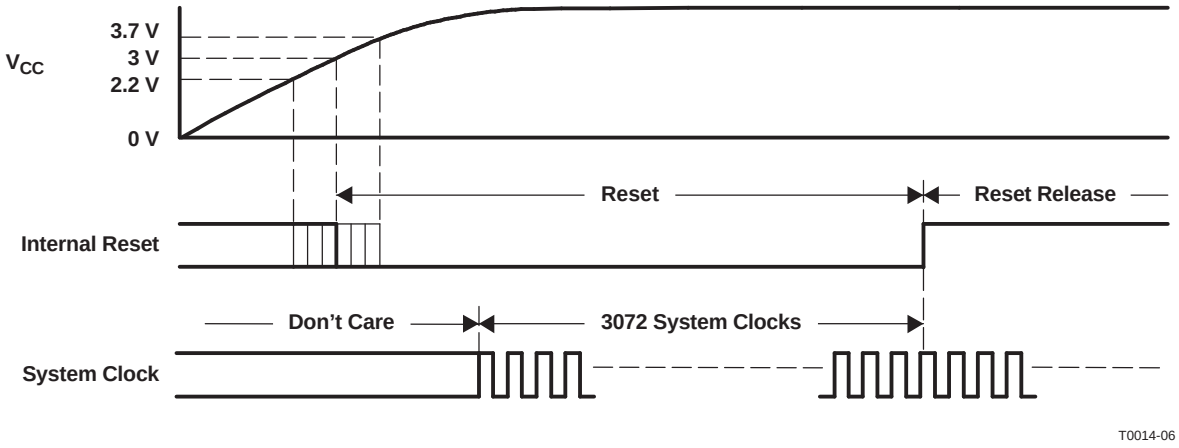


Figure 21. Power-On-Reset Timing

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1680 consists of a 6-wire synchronous serial port. It includes LRCK (pin 8), BCK (pin 7), and DATA1 (pin 6), DATA2 (pin 11), DATA3 (pin 12), and DATA4 (pin 13). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA1, DATA2, DATA3, and DATA4 into the audio interface serial shift register. Serial data are clocked into the PCM1680 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface internal registers.

Both LRCK and BCK must be synchronous with the system clock. Ideally, it is recommended that LRCK and BCK are derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, or 64 times the sampling frequency.

Internal operation of the PCM1680 is synchronized with LRCK. Accordingly, internal operation is suspended when the sampling rate clock, LRCK, is changed or when SCK and/or BCK is interrupted at least for a 3-bit clock cycle. If SCK, BCK, and LRCK are provided continuously after this suspended condition, the internal operation is resynchronized automatically within the following 3/f_S period. External resetting is not required.

AUDIO DATA FORMATS AND TIMING

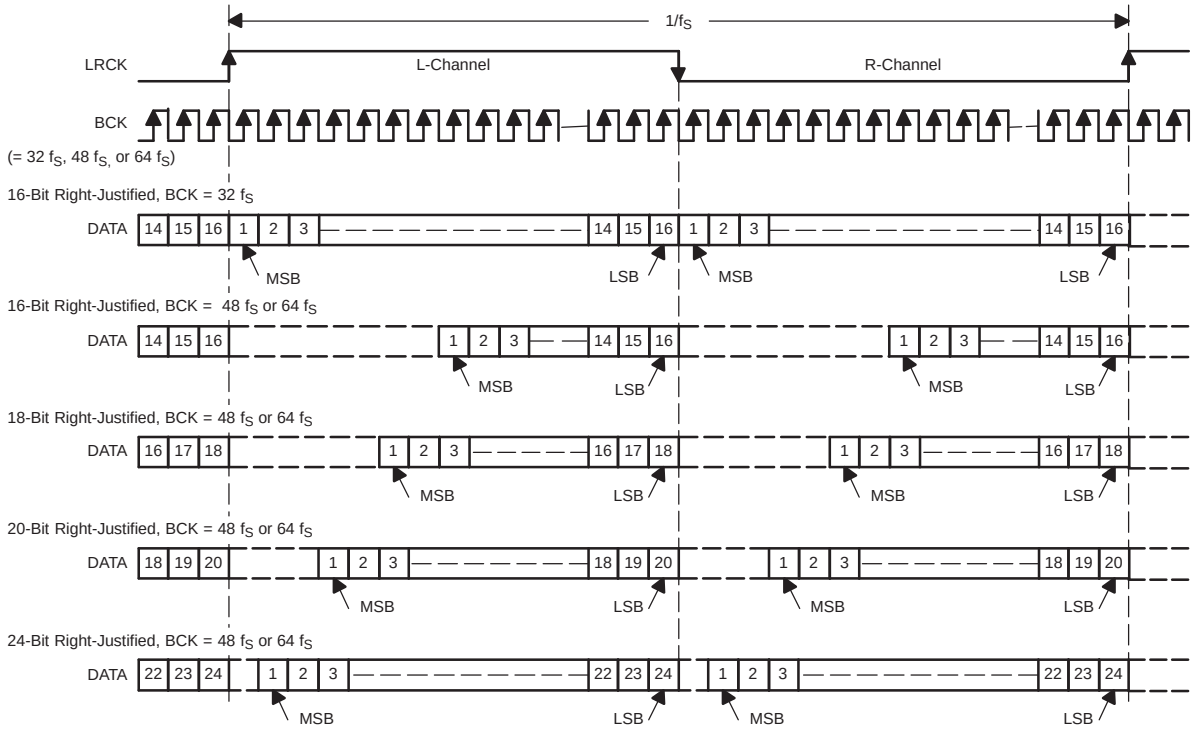
The PCM1680 supports industry-standard audio data formats, including right-justified, I^2S, and left-justified. The data formats are shown in Figure 22. Data formats are selected using the format bits, FMT[2:0], located in control register 9 of the PCM1680. The default data format is 24-bit left-justified. All formats require binary twos complement, MSB-first audio data. Figure 22 shows a detailed timing diagram for the serial audio interface.

DATA1, DATA2, DATA3, and DATA4 each carry two audio channels, designated as the left and right channels. The left-channel data always precedes the right-channel data in the serial data stream for all data formats. Table 2 shows the mapping of the digital input data to the analog output pins.

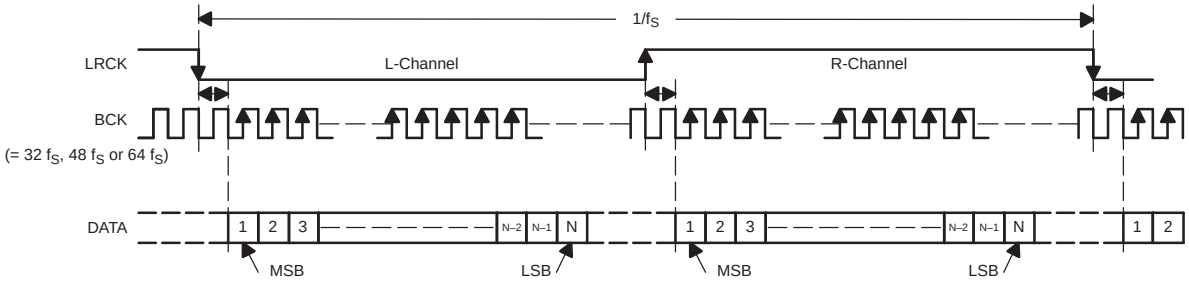
Table 2. Audio Input Data to Analog Output Mapping

DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA1	Left	$V_{OUT}1$
	Right	$V_{OUT}2$
DATA2	Left	$V_{OUT}3$
	Right	$V_{OUT}4$
DATA3	Left	$V_{OUT}5$
	Right	$V_{OUT}6$
DATA4	Left	$V_{OUT}7$
	Right	$V_{OUT}8$

(1) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

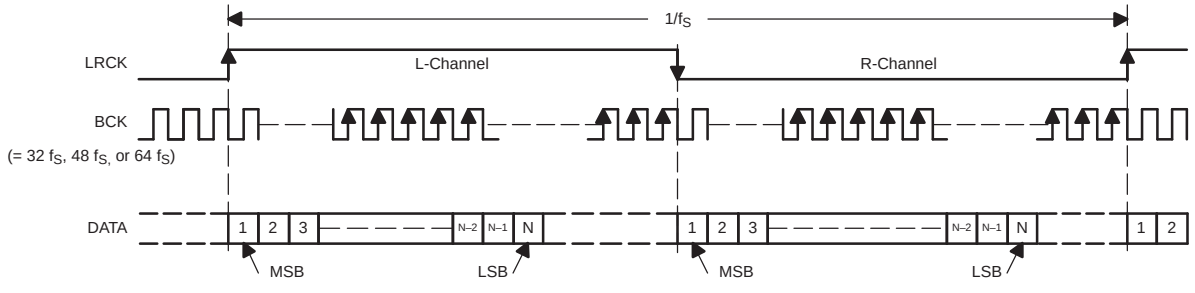
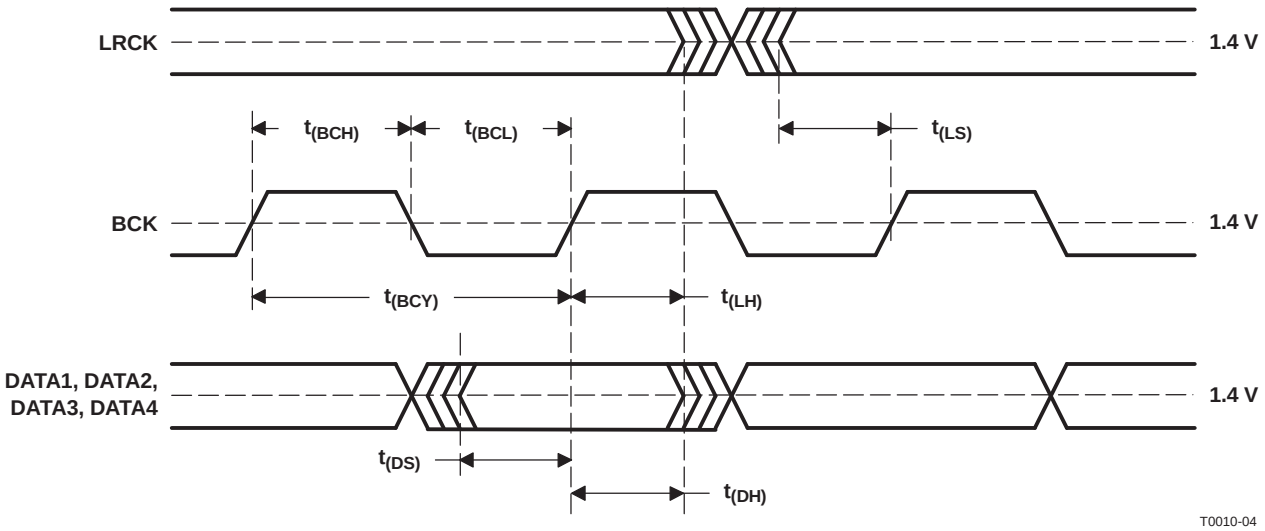


Figure 22. Audio Data Input Formats



PARAMETER		MIN	UNIT
$t_{(BCY)}$	BCK pulse cycle time	1/(32 f_S), 1/(48 f_S), 1/(64 f_S)(1)	
$t_{(BCH)}$	BCK pulse duration, HIGH	35	ns
$t_{(BCL)}$	BCK pulse duration, LOW	35	ns
$t_{(LS)}$	LRCK setup time to BCK rising edge	10	ns
$t_{(LH)}$	LRCK hold time to BCK rising edge	10	ns
$t_{(DS)}$	DATA1, DATA2, DATA3, DATA4 setup time	10	ns
$t_{(DH)}$	DATA1, DATA2, DATA3, DATA4 hold time	10	ns

(1) f_S is the sampling frequency.

Figure 23. Audio Interface Timing

OVERSAMPLING RATE CONTROL

The PCM1680 automatically controls the oversampling rate of the delta-sigma DACs using the system clock frequency. The oversampling rate is set to 64x oversampling with an 1152-f_S, 768-f_S, or 512-f_S system clock; 32x oversampling with a 384-f_S or 256-f_S system clock; and 16x oversampling with a 192-f_S or 128-f_S system clock.

ZERO FLAG

The PCM1680 has two zero-flag pins, ZERO1 (pin 1) and ZERO2 (pin 28), which are assigned to the combinations A through D as shown in Table 3. Zero-flag combinations are selected using the zero-flag combination bits, AZRO[1:0], located in control register 13 of the PCM1680. If the input data of the L-channel and/or R-channel of all assigned channels remain at a logic-0 level for 1024 sampling periods (LRCK clock periods), ZERO1 and ZERO2 are set to a logic-1 state, or high level. If the input data of any of the assigned channels contain a logic-1, ZERO1, and ZERO2 are set to a logic-0 state immediately.

The active polarity of the zero-flag output can be inverted by setting the ZREV bit of control register 10 to 1. The reset default is active-high output or ZREV = 0.

Table 3. Zero-Flag Output Combinations

ZERO-FLAG COMBINATION	ZERO1 (PIN 1)	ZERO2 (PIN 28)
A	DATA1 L-ch	DATA1 R-ch
B	N/A	DATA[1:4]
C	DATA4	DATA[1:3]
D	DATA1	DATA[2:4]

MODE CONTROL

The PCM1680 has many programmable functions which can be controlled in the software control mode. The functions are controlled by programming and reading the internal registers using the SPI or I^2C interface. These two interfaces for mode control can be selected by MSEL (pin 14). The functions of pins 2, 3, and 4 are changed by MSEL selection as shown in Table 4.

Table 4. Interface Mode Control

MSEL	INTERFACE MODE	PIN FUNCTION		
		PIN 2	PIN 3	PIN 4
LOW	SPI	$\overline{MS}$	MC	MD
HIGH	I^2C	ADR	SCL	SCA

SPI CONTROL INTERFACE

The SPI control interface of the PCM1680 is a 3-wire synchronous serial port that operates asynchronously to the serial audio interface. The SPI control interface is used to program the on-chip mode registers. The control interface includes MD (pin 4), MC (pin 3), and $\overline{MS}$ (pin 2). MD is the serial data input, used to program the mode registers. MC is the control port for the serial bit clock, used to shift in the serial data, and $\overline{MS}$ is the control port for mode control select, which is used to enable the mode control.

REGISTER WRITE OPERATION

All write operations for the serial control port use 16-bit data words. Figure 24 shows the control data word format. The most significant bit is a fixed '0' for the write operation. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 25 shows the functional timing diagram for writing to the serial control port. $\overline{MS}$ is held at a logic-1 state until a register must be written. To start the register write cycle, $\overline{MS}$ is set to logic-0. 16 clock cycles are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the completion of the 16th clock cycle, $\overline{MS}$ is set to logic-1 to latch the data into the indexed mode control register.

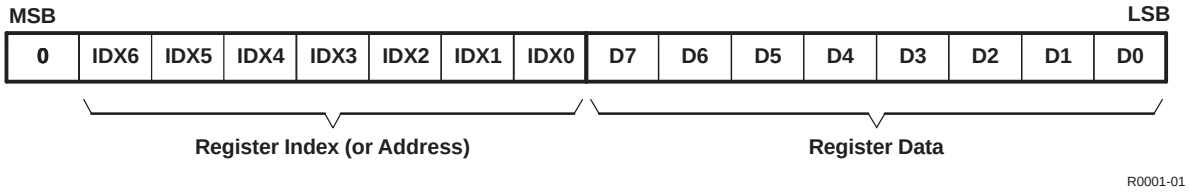


Figure 24. Control Data Word Format for MD

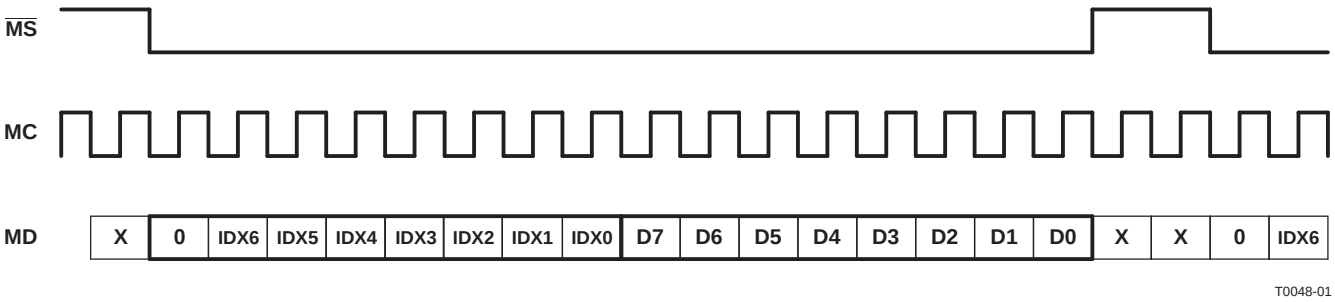
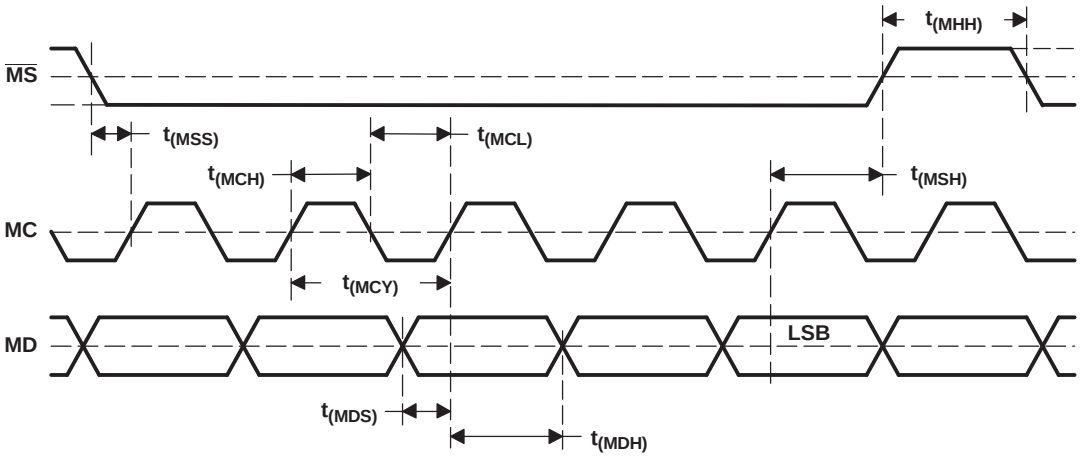


Figure 25. Write Operation Timing

INTERFACE TIMING REQUIREMENTS

Figure 26 shows a detailed timing diagram for the serial control interface. Special attention to the setup and hold times is required. Also, $t_{(MSS)}$ and $t_{(MSH)}$, which define minimum delays between edges of the MS and MC clocks, require special attention. These timing parameters are critical for proper control port operation.



T0013-03

PARAMETER		MIN	UNIT
$t_{(MCY)}$	MC pulse cycle time	100	ns
$t_{(MCL)}$	MC pulse duration, LOW	50	ns
$t_{(MCH)}$	MC pulse duration, HIGH	50	ns
$t_{(MHH)}$	$\overline{MS}$ pulse duration, HIGH	(1)	
$t_{(MSS)}$	$\overline{MS}$ falling edge to MC rising edge	20	ns
$t_{(MSH)}$	$\overline{MS}$ hold time, MC rising edge for LSB to $\overline{MS}$ rising edge	20	ns
$t_{(MDH)}$	MD hold time	15	ns
$t_{(MDS)}$	MD setup time	20	ns

(1) $3/(256\ f_S)$, f_S: sampling rate

Figure 26. Interface Timing

I²C INTERFACE

The PCM1680 supports the I²C serial bus and data transmission protocol for standard mode as a slave device. This protocol is explained in the I²C specification 2.0. The PCM1680 does not support a board-to-board interface. Figure 27 shows the I²C framework for basic read and write operations.

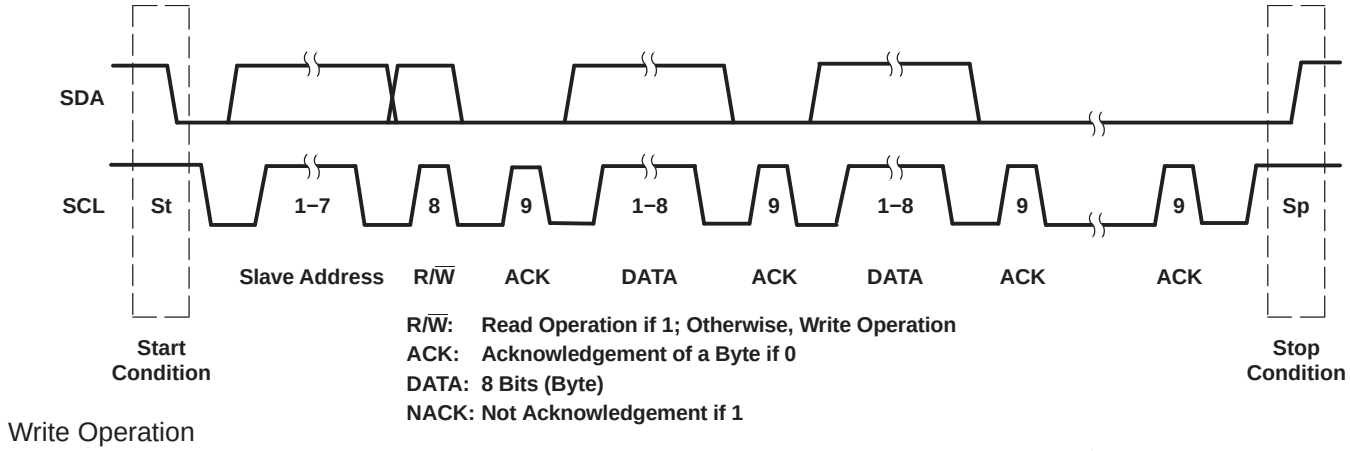
SLAVE ADDRESS

MSB							LSB
1	0	0	1	1	0	ADR	R/$\overline{W}$

The PCM1680 has seven bits for its own slave address. The first six bits (MSBs) of the slave address are factory preset to 1001 10. The next bit of the address byte is the device select bit, which can be user-defined using the ADR terminal. A maximum of two PCM1680s can be connected on the same bus at one time. Each PCM1680 responds when it receives its own slave address.

PACKET PROTOCOL

A master device must control packet protocol, which consists of a start condition, slave address, read/write bit, data if writing or acknowledge if reading, and a stop condition. The PCM1680 supports only slave receivers and slave transmitters.



Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Read Operation

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*		*M*	*M*
Data Type	St	Slave Address	R	ACK	DATA	ACK	DATA	ACK		NACK	Sp

M: Master Device *S: Slave Device* St: Start Condition
Sp: Stop Condition $\overline{W}$: Write R: Read

T0049-01

Figure 27. Basic I²C Framework

WRITE OPERATION

A master can write to any PCM1680 registers using a single access. The master sends a PCM1680 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the PCM1680 sends an acknowledgment, but the write operation does not occur. Figure 28 is a diagram of the write operation.

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Write Data	ACK	Sp

M: Master Device *S: Slave Device*
St: Start Condition $\overline{W}$: Write ACK: Acknowledge Sp: Stop Condition

R0002-01

Figure 28. Write Operation

READ OPERATION

A master can read any PCM1680 register using a single access. The master sends a PCM1680 slave address with a read bit after transferring the register address. Then the PCM1680 transfers the data in the register specified. Figure 29 is a diagram of the read operation.

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*M*	*M*	*S*	*S*	*M*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

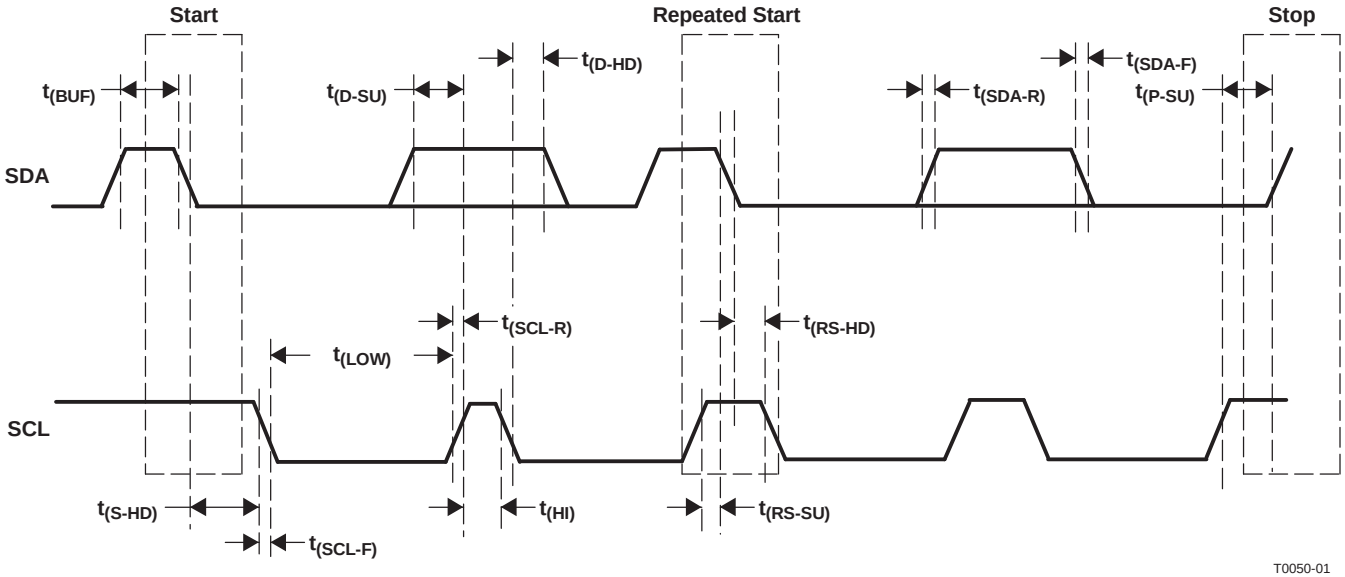
M: Master Device *S: Slave Device* St: Start Condition
Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge
$\overline{W}$: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 29. Read Operation

TIMING DIAGRAM



T0050-01

PARAMETER		MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	4.7		µs
$t_{(LOW)}$	Low period of the SCL clock	4.7		µs
$t_{(HI)}$	High period of the SCL clock	4		µs
$t_{(RS-SU)}$	Setup time for (repeated) START condition	4.7		µs
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for (repeated) START condition	4		µs
$t_{(D-SU)}$	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	20 + 0.1 C_B	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	4		µs
C_B	Capacitive load for SDA and SCL lines		400	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	0.2 V_{DD}		V

Figure 30. Interface Timing

MODE CONTROL REGISTERS

USER-PROGRAMMABLE MODE CONTROLS

The PCM1680 includes a number of user-programmable functions which are accessed via control registers. The registers are programmed using the serial control interface which is discussed in the *Mode Control* section of this data sheet. Table 5 lists the available mode control functions, along with the respective reset default conditions and associated register index.

REGISTER MAP

The mode control register map is shown in Table 6. The MSB of all registers is fixed to 0. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

RESERVED REGISTERS

Registers 0, 11, and 15 are reserved for factory use. To ensure proper operation, the user should not write to these registers.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	1–6, 16, 17	AT1[7:0], AT2[7:0], AT3[7:0], AT4[7:0], AT5[7:0], AT6[7:0], AT7[7:0], AT8[7:0]
Soft mute control	Mute disabled	7, 18	MUT[6:1], MUT[8:7]
DAC1–DAC8 operation control	DAC1–DAC8 enabled	8, 19	DAC[6:1], DAC[8:7]
Audio data format control	24-bit, left-justified	9	FMT[2:0]
Digital filter roll-off control	Sharp roll-off	9	FLT
De-emphasis all-channel function control	De-emphasis of all channels disabled	10	DMC
De-emphasis all-channel sample rate selection	44.1 kHz	10	DMF[1:0]
Output phase select	Normal phase	10	DREV
Zero-flag polarity select	High	10	ZREV
Software reset control	Reset disabled	10	SRST
Oversampling rate control	x64, x32, x16	12	OVER
Zero-flag combination select	ZERO1: DATA1 Lch ZERO2: DATA1 Rch	13	AZRO[1:0]
Digital attenuation mode select	0 to –63 dB, 0.5-dB step	13	DAMS
Zero-detect status (read-only, I^2C interface only)	N/A	14	ZERO[8:1]

Table 6. Mode Control Register Map

IDX (B8–B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
01h	1	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
02h	2	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
03h	3	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
04h	4	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
05h	5	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
06h	6	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
07h	7	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
08h	8	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
09h	9	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	FLT	RSV(1)	RSV(1)	FMT2	FMT1	FMT0
0Ah	10	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	ZREV	DREV	DMF1	DMF0	RSV(1)	RSV(1)	DMC
0Ch	12	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)
0Dh	13	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DAMS	AZRO1	AZRO0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)
0Eh	14	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1
10h	16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT71	AT70
11h	17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80
12h	18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	MUT8	MUT7
13h	19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	DAC8	DAC7

(1) Reserved for test operation. It should be set to '0' during normal operation.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 1	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
REGISTER 2	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
REGISTER 3	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
REGISTER 4	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
REGISTER 5	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
REGISTER 6	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
REGISTER 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT711	AT70
REGISTER 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80

ATx[7:0]: Digital Attenuation Level Setting

Where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 1111 1111b.

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING	
		DAMS = 0	DAMS = 1
1111 1111b	255	0 dB, no attenuation (default)	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB	–1 dB
1111 1101b	253	–1 dB	–2 dB
:	:	:	:
1001 1100b	156	–49.5 dB	–99 dB
1001 1011b	155	–50 dB	–100 dB
1001 1010b	154	–50.5 dB	Mute
:	:	:	:
1000 0010b	130	–62.5 dB	Mute
1000 0001b	129	–63 dB	Mute
1000 0000b	128	Mute	Mute
:	:	:	:
0000 0000b	0	Mute	Mute

Each DAC output, $V_{OUT}1$ through $V_{OUT}8$, has a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuation levels are made by incrementing or decrementing by one step (S-dB) for every $8/f_S$ time interval until the programmed attenuation setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute). Range (R) and step (S) are –63 and 0.5, respectively, for DAMS = 0 and –100 and 1, respectively, for DAMS = 1. The DAMS bit is defined in register 13. The attenuation data for each channel can be set individually. The attenuation level can be calculated using the following formula:

$$\text{Attenuation level (dB)} = S \times (ATx[7:0]_{DEC} - 255)$$

Where $ATx[7:0]_{DEC}$ = 0 through 255. For $ATx[7:0]_{DEC}$ = 0 through 128 with DAMS = 0 or for $ATx[7:0]_{DEC}$ = 0 through 154 with DAMS = 1, the attenuation is set to infinite attenuation (mute).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 7	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
REGISTER 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	MUT8	MUT7

MUTx: Soft Mute Control

Where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 through MUT8, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}1$ through $V_{OUT}8$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to the infinite-attenuation setting one attenuator step (S-dB) at a time. This provides a quiet, pop-free muting of the DAC output. On returning from soft mute, by setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuator level. The step size, S, is 0.5 dB for DAMS = 0 and 1 dB for DAMS = 1.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 8	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
REGISTER 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	DAC8	DAC7

DACx: DAC Operation Control

Where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}1$ through $V_{OUT}8$. When DACx = 0, the output amplifier input is connected to the DAC output. When DACx = 1, the output amplifier input is switched to the dc common voltage (V_{COM}), equal to $V_{CC}/2$.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 9	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

FLT: Digital Filter Roll-Off Control

Default value: 0

FLT = 0	Sharp roll-off (default)
FLT = 1	Slow roll-off

The FLT bit allows users to select the digital filter roll-off that is best suited to their application. Two filter roll-off selections are available: sharp or slow. The filter responses for these selections are shown in the Typical Characteristics section of this data sheet.

FMT[2:0]: Audio Interface Data Format

Default value: 101b

FMT[2:0]	Audio Data Format Selection
000	24-bit right-justified format, standard data
001	20-bit right-justified format, standard data
010	18-bit right-justified format, standard data
011	16-bit right-justified format, standard data
100	I^2S format, 16- to 24-bit
101	Left-justified format, 16- to 24-bit (default)
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 10	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	ZREV	DREV	DMF1	DMF0	RSV	RSV	DMC

SRST: Reset

Default value: 0

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as the power-on-reset function with the exception of the reset period, which is 1024 system clocks for the SRST function. All registers are initialized.

ZREV: Zero-Flag Polarity Select

Default value: 0

ZREV = 0	Zero-flag pins high at a zero detect (default)
ZREV = 1	Zero-flag pins low at a zero detect

The ZREV bit allows the user to select the polarity of the zero-flag pins.

DREV: Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is the output analog signal phase control.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00b

DMF[1:0]	De-Emphasis Sampling Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits select the sampling frequency used for the digital de-emphasis function when it is enabled. The de-emphasis curves are shown in the Typical Characteristics section of this data sheet. The preceding table shows the available sampling frequencies.

DMC: Digital De-Emphasis All-Channel Function Control

Default value: 0

DMC = 0	De-emphasis disabled for all channels (default)
DMC = 1	De-emphasis enabled for all channels

The DMC bit is used to enable or disable the de-emphasis function for all channels.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 12	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV	RSV	RSV	RSV	RSV	RSV	RSV

OVER: Oversampling Rate Control

Default value: 0

System clock frequency = 512 f_S, 768 f_S, or 1152 f_S

OVER = 0	x64 oversampling (default)
OVER = 1	x128 oversampling (applicable only if sampling clock frequency ≤ 24 kHz)

System clock frequency = 256 f_S or 384 f_S

OVER = 0	x32 oversampling (default)
OVER = 1	x64 oversampling (applicable only if sampling clock frequency ≤ 48 kHz)

System clock frequency = 128 f_S or 192 f_S.

OVER = 0	x16 oversampling (default)
OVER = 1	x32 oversampling (applicable only if sampling clock frequency ≤ 96 kHz)

The OVER bit is used to control the oversampling rate of the ΔΣ DACs.

Setting OVER = 1 is recommended under the following conditions:

- System clock frequency = 512 f_S, 768 f_S, or 1152 f_S and sampling clock frequency ≤ 24 kHz
- System clock frequency = 256 f_S or 384 f_S and sampling clock frequency ≤ 48 kHz
- System clock frequency = 128 f_S or 192 f_S and sampling clock frequency ≤ 96 kHz

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 13	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DAMS	AZRO1	AZRO0	RSV	RSV	RSV	RSV	RSV

DAMS: Digital Attenuation Mode Select

Default value: 0

DAMS = 0	Fine step, 0.5 dB/step for 0 to –63 dB range (default)
DAMS = 1	Wide range, 1 dB/step for 0 to –100 dB range

The DAMS bit is used to select the digital attenuation mode.

AZRO[1:0]: Zero-Flag Channel-Combination Select

Default value: 00b

AZRO[1:0]	Zero-Flag Channel-Combination Select
00	Combination A (ZERO1: DATA1 L-ch, ZERO2: DATA1 R-ch) (default)
01	Combination B (ZERO1: N/A, ZERO2: DATA1–DATA4)
10	Combination C (ZERO1: DATA4, ZERO2: DATA1–DATA3)
11	Combination D (ZERO1: DATA1, ZERO2: DATA2–DATA4)

The AZRO[1:0] bits are used to select the zero-flag channel combinations for ZERO1 and ZERO2.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 14	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1

ZERO[8:1]: Zero-Detect Status (Read-Only, I^2C Interface Only)

Default value: N/A

The ZERO[8:1] bits show the status of zero detect for each channel. The status is set to '1' by detecting a zero state without regard to the ZREV bit setting.

ANALOG OUTPUTS

The PCM1680 includes eight independent output channels, $V_{OUT}1$ through $V_{OUT}8$. These channels are unbalanced outputs, each capable of driving 3.9 V_{PP} typical into a 5-kΩ ac load with V_{CC} = 5 V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}8$ are biased to the dc common voltage, equal to 0.5 × V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM1680 ΔΣ DACs. The frequency response of this filter is shown in Figure 11. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section of this data sheet.

V_{COM} OUTPUT

One unbuffered common voltage output pin, V_{COM} (pin 25), is brought out for decoupling purposes. This pin is nominally biased to the dc common voltage, equal to $V_{CC}/2$. If this pin is to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 31 shows an example of using the V_{COM} pin for external biasing applications.

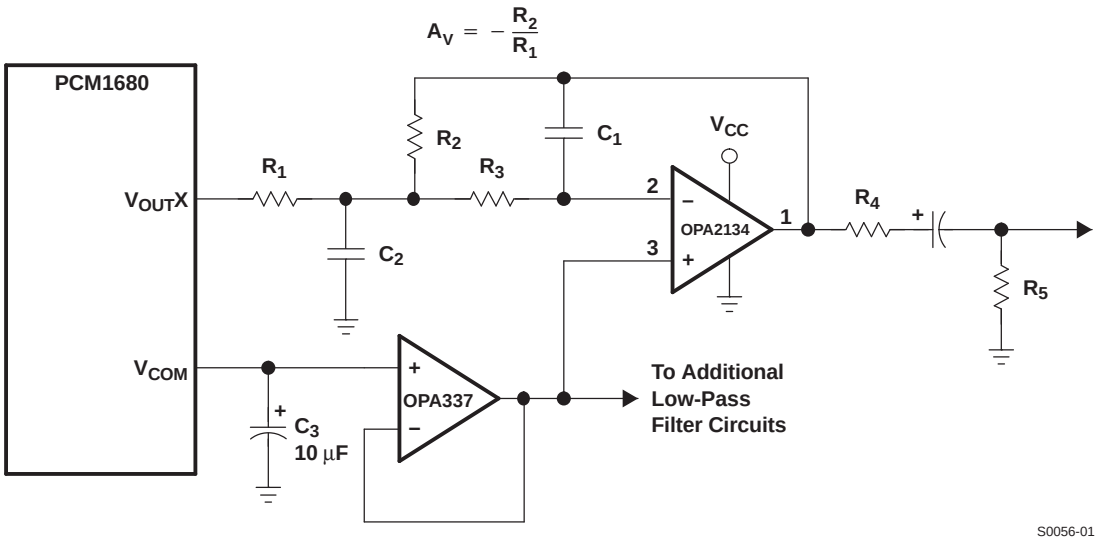
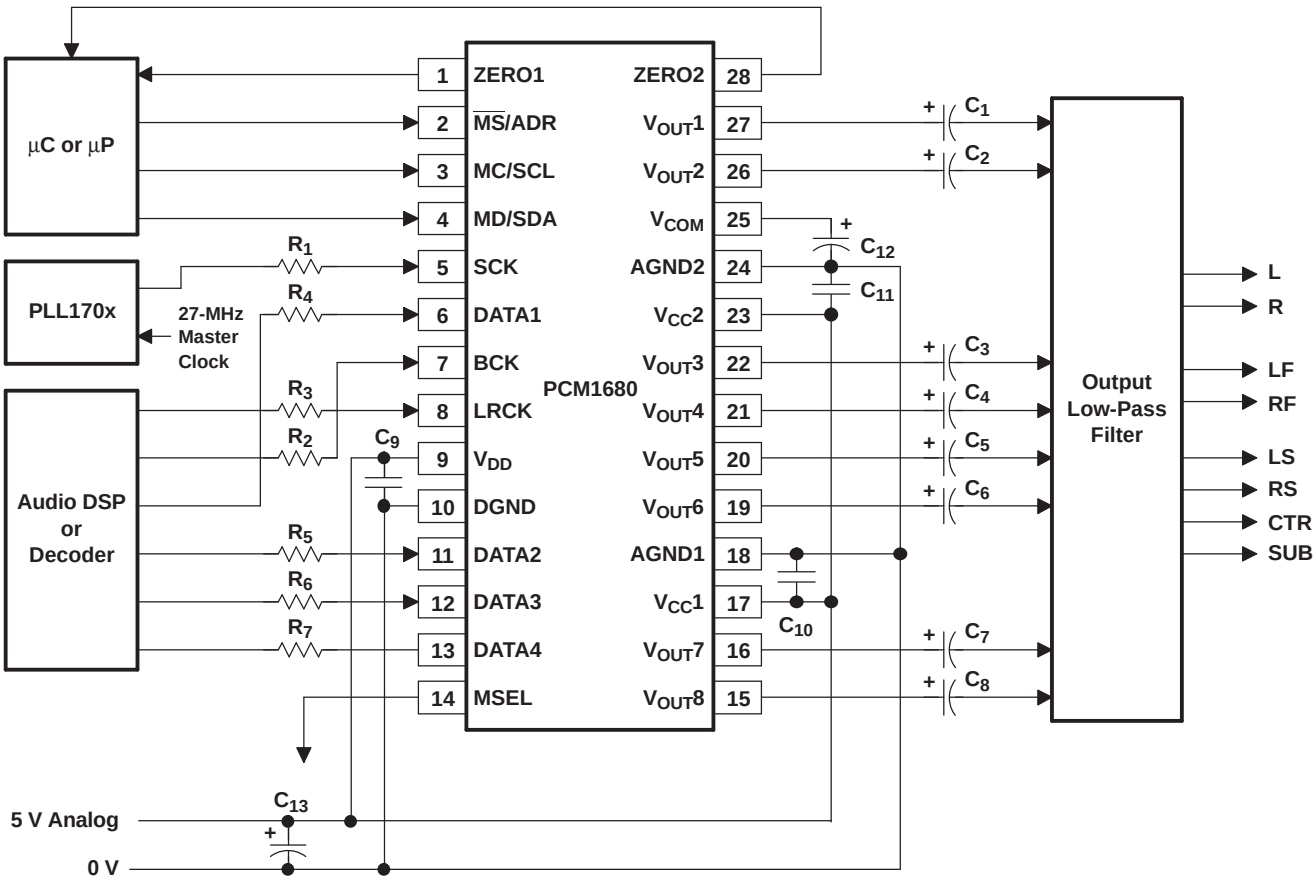


Figure 31. Single-Supply Filter Circuit Using V_{COM} for External Biasing Applications

APPLICATION INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 32, with the necessary power-supply bypassing and decoupling components. Texas Instruments' PLL170x is used to generate the system clock input at SCK, as well as generating the clock for the audio signal processor. The use of series resistors (22 Ω to 100 Ω) is recommended for SCK, LRCK, BCK, DATA1, DATA2, DATA3, and DATA4. The series resistor combines with the stray printed circuit board (PCB) capacitance and device input capacitance to form a low-pass filter that removes high-frequency noise from the digital signal, thus reducing high-frequency emission.



C_1–C_8: 4.7-µF to 10-µF Electrolytic Typical
C_9–C_{11}: 1-µF Ceramic Typical
C_{12}, C_{13}: 10-µF Electrolytic Typical
R_1–R_7: 22 Ω to 100 Ω Typical

S0057-01

Figure 32. Basic Connection Diagram

POWER SUPPLY AND GROUNDING

The PCM1680 requires 5 V for the analog supply and digital supply. The 5-V supply is used to power not only the DAC analog and output filter circuitry, but also the digital filter and serial interface circuitry. For best performance, a 5-V supply using a linear regulator is recommended.

Four capacitors are required for supply bypassing, as shown in Figure 32. These capacitors should be located as close as possible to the PCM1680 package. The 10-µF capacitor should be tantalum or aluminum electrolytic, while the three 1-µF capacitors are ceramic.

DAC OUTPUT FILTER CIRCUITS

ΔΣ DACs use noise shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 31 and Figure 33 show the recommended external low-pass active filter circuits for dual- and single-supply applications. These circuits are second-order Butterworth filters using a multiple-feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see *Dynamic Performance Testing of Digital Audio D/A Converters* (SBAA055).

Because the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. Texas Instruments' OPA2134 and OPA2353 dual operational amplifiers are shown in Figure 31 and Figure 33, and are recommended for use with the PCM1680.

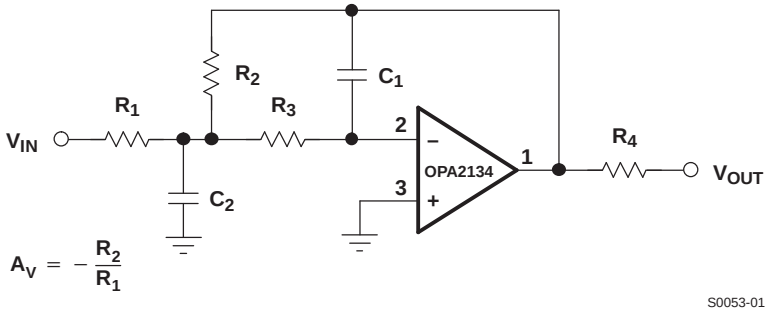


Figure 33. Dual-Supply Filter Circuit

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1680 is shown in Figure 34. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1680 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This separation prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1680. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 35 shows the recommended approach for single-supply applications.

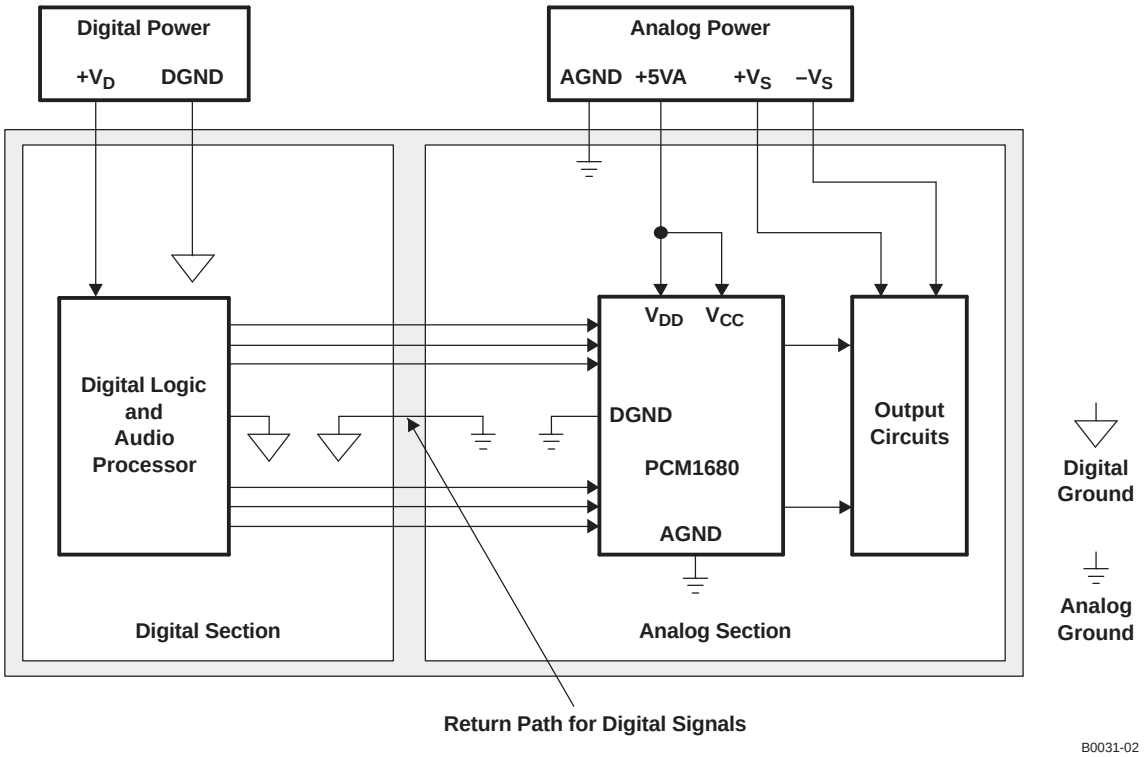


Figure 34. Recommended PCB Layout

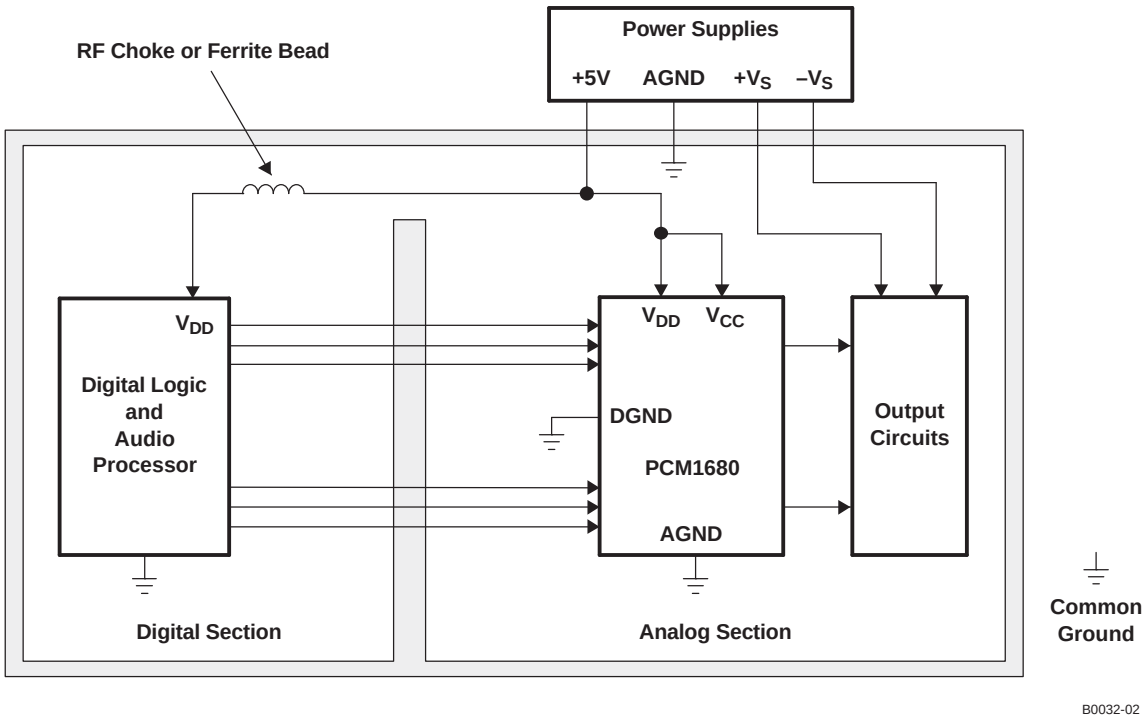


Figure 35. Single-Supply PCB Layout

Revision History

Changes from Revision A (August 2006) to Revision B	Page
• Changed *0.49 V_{CC}* to *0.486 V_{CC}* in the *DC Accuracy* section of the Electrical Characteristics table	3
• Corrected footnote 1 in Figure 26	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1680DBQ	ACTIVE	SSOP	DBQ	28	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 70	PCM1680	Samples
PCM1680DBQG4	ACTIVE	SSOP	DBQ	28	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 70	PCM1680	Samples
PCM1680DBQR	ACTIVE	SSOP	DBQ	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 70	PCM1680	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

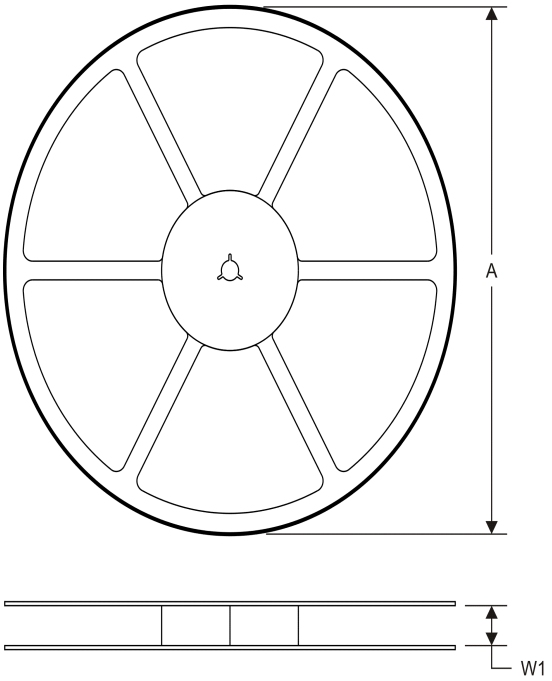
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

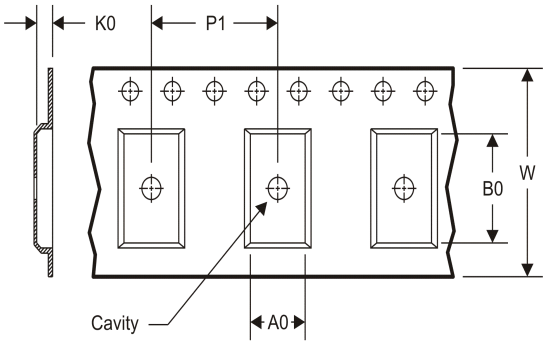
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



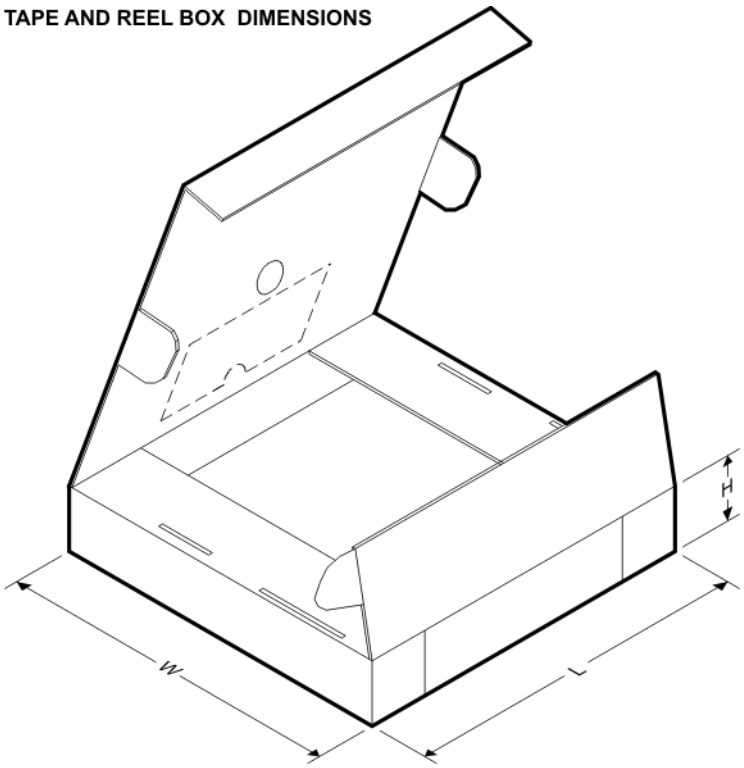
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1680DBQR	SSOP	DBQ	28	2000	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

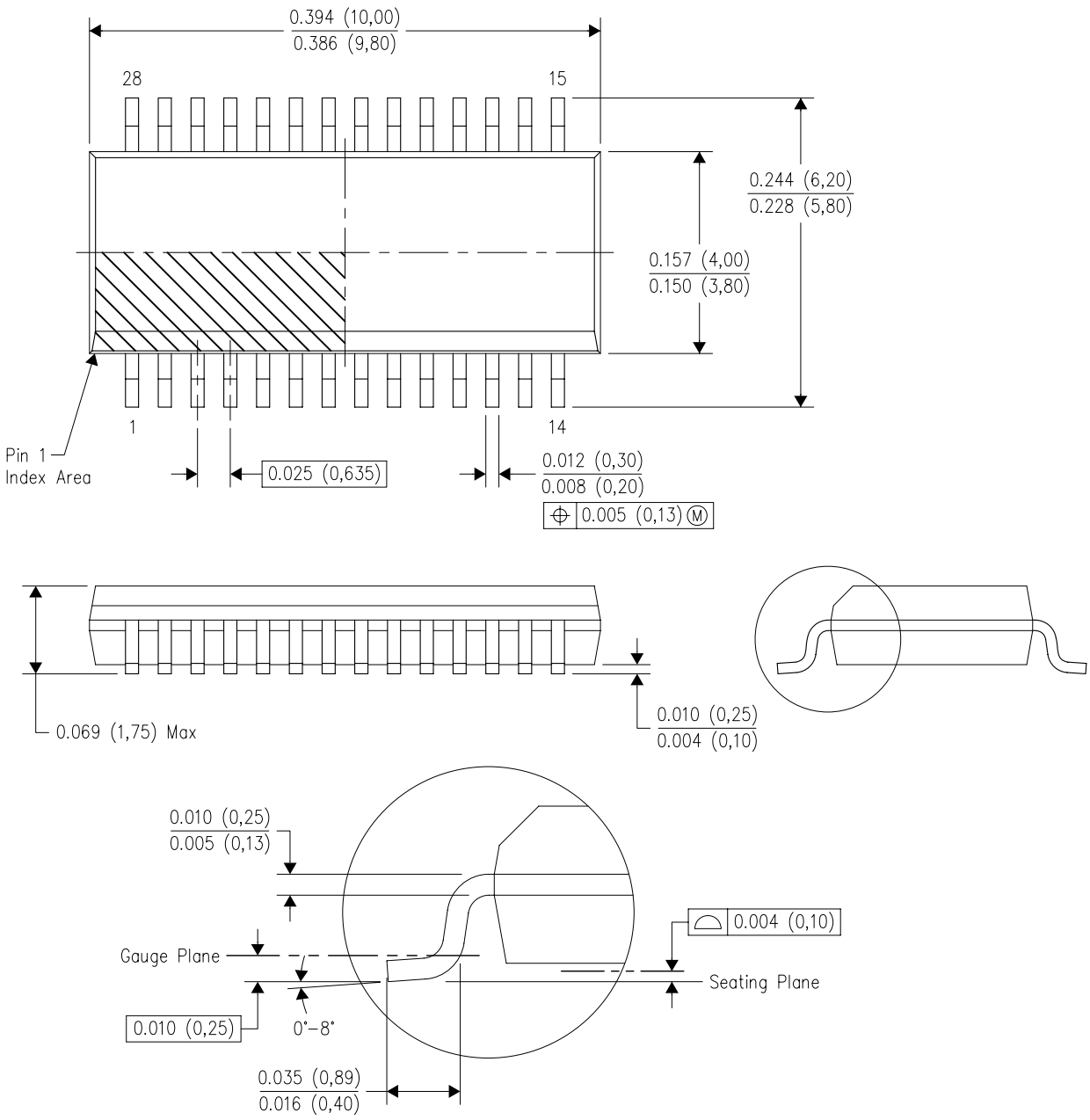
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

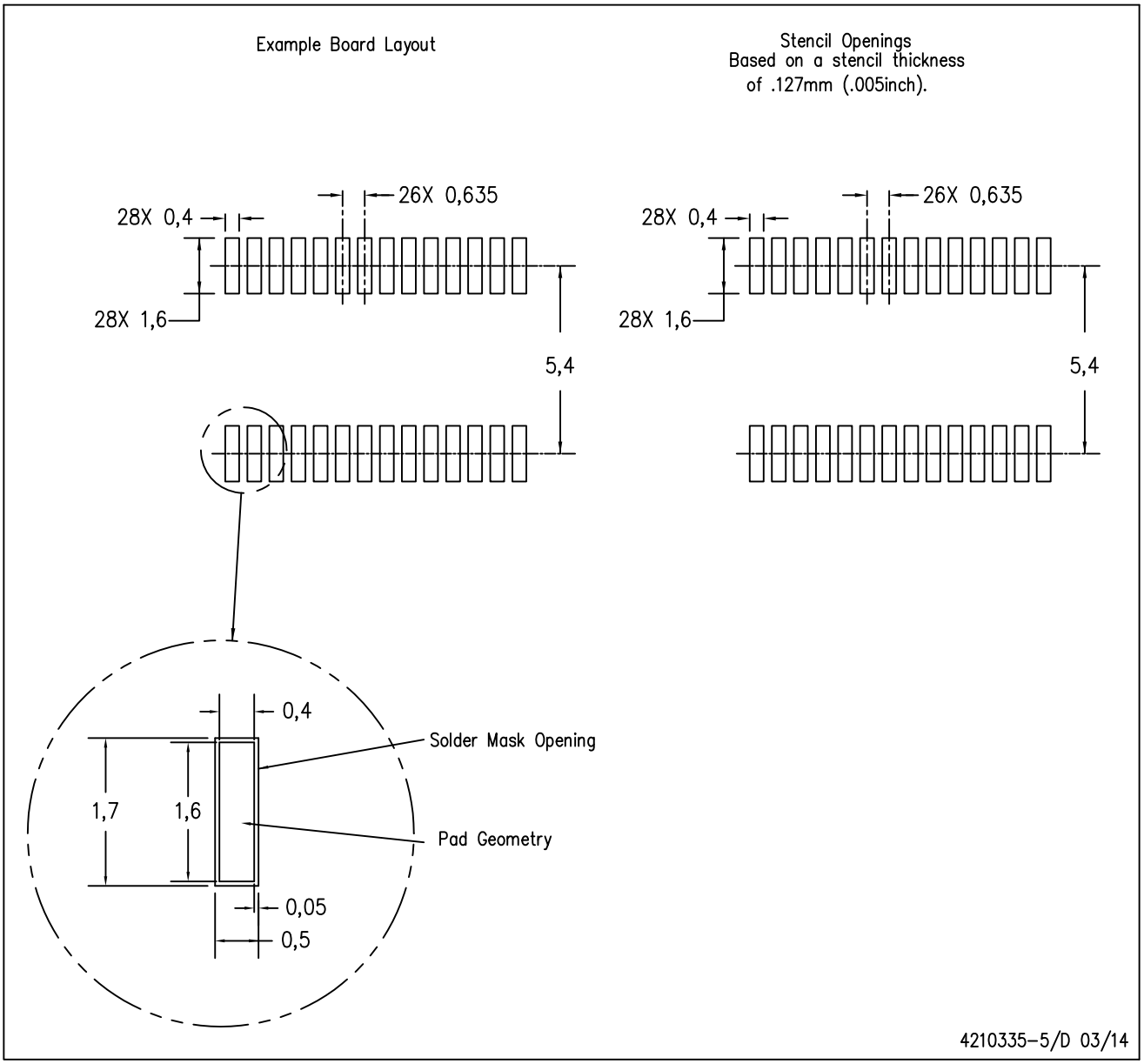
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1680DBQR	SSOP	DBQ	28	2000	367.0	367.0	38.0

DBQ (R–PDSO–G28) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AF.

DBQ (R–PDSO–G28) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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