

# SN74AHCT16245 16-Bit Bus Transceivers With 3-State Outputs

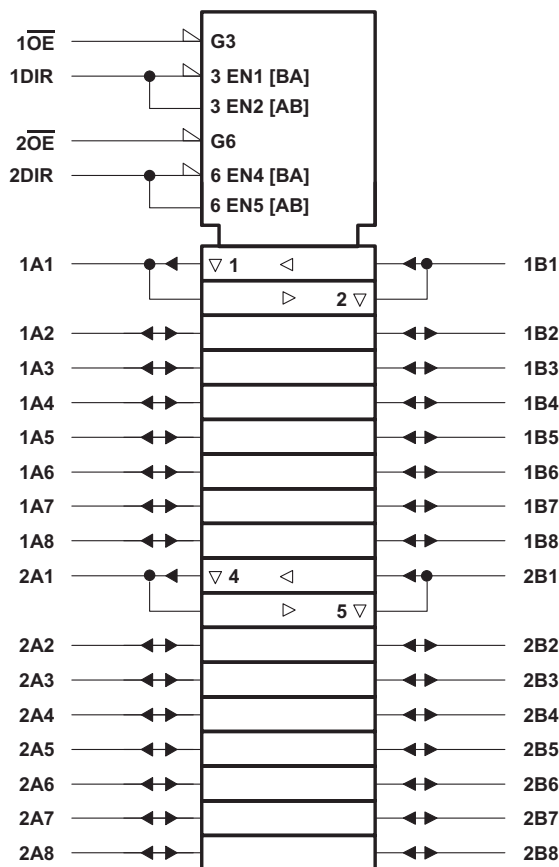
## 1 Features

- Members of Texas Instruments' Widebus™ Family
- Inputs are TTL-Voltage Compatible
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17

## 2 Applications

- Telecom and Wireless Infrastructures
- Electronic Points of Sale
- Printers and Other Peripherals
- Motor Drives
- Health and Fitness

## 4 Simplified Schematic



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## 3 Description

The SN74AHCT16245 device is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses.

### Device Information<sup>(1)</sup>

| PART NUMBER   | PACKAGE    | BODY SIZE (NOM)    |
|---------------|------------|--------------------|
| SN74AHCT16245 | TVSOP (48) | 9.70 mm × 4.40 mm  |
|               | SSOP (48)  | 15.80 mm × 7.50 mm |
|               | TSSOP (48) | 12.50 mm × 6.10 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

|  |          |  |           |
|--|----------|--|-----------|
| <b>1 Features</b> .....                          | <b>1</b> | <b>9 Detailed Description</b> .....                              | <b>9</b>  |
| <b>2 Applications</b> .....                      | <b>1</b> | 9.1 Overview .....   | 9         |
| <b>3 Description</b> .....                       | <b>1</b> | 9.2 Functional Block Diagrams .....                              | 9         |
| <b>4 Simplified Schematic</b> .....              | <b>1</b> | 9.3 Feature Description .....                                    | 10        |
| <b>5 Revision History</b> .....                  | <b>2</b> | 9.4 Device Functional Modes .....                                | 10        |
| <b>6 Pin Configuration and Functions</b> .....   | <b>3</b> | <b>10 Application and Implementation</b> .....                   | <b>11</b> |
| <b>7 Specifications</b> .....                    | <b>5</b> | 10.1 Application Information .....                               | 11        |
| 7.1 Absolute Maximum Ratings .....               | 5        | 10.2 Typical Application .....                                   | 11        |
| 7.2 Handling Ratings .....                       | 5        | <b>11 Power Supply Recommendations</b> .....                     | <b>12</b> |
| 7.3 Recommended Operating Conditions .....       | 5        | <b>12 Layout</b> .....   | <b>12</b> |
| 7.4 Thermal Information .....                    | 6        | 12.1 Layout Guidelines .....                                     | 12        |
| 7.5 Electrical Characteristics .....             | 6        | 12.2 Layout Example .....  | 12        |
| 7.6 Switching Characteristics .....              | 7        | <b>13 Device and Documentation Support</b> .....                 | <b>13</b> |
| 7.7 Noise Characteristics .....                  | 7        | 13.1 Trademarks .....  | 13        |
| 7.8 Operating Characteristics .....              | 7        | 13.2 Electrostatic Discharge Caution .....                       | 13        |
| 7.9 Typical Characteristics .....                | 7        | 13.3 Glossary .....  | 13        |
| <b>8 Parameter Measurement Information</b> ..... | <b>8</b> | <b>14 Mechanical, Packaging, and Orderable Information</b> ..... | <b>13</b> |

## 5 Revision History

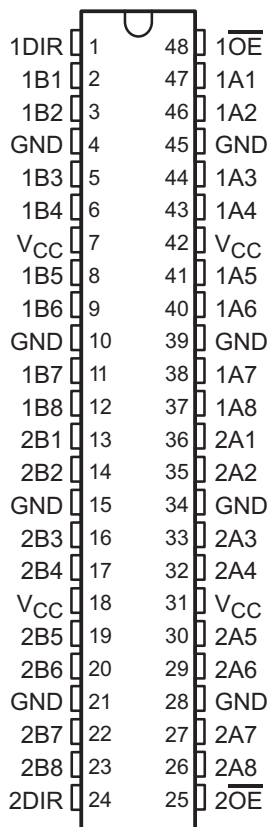
### Changes from Revision J (October 2000) to Revision K

Page

|   |    |
|---|----|
| • Updated document to new TI data sheet format. ....  | 1  |
| • Deleted Ordering Information table. ....  | 1  |
| • Deleted SN54AHCT16245 device from data sheet. ....  | 1  |
| • Added Applications. ....  | 1  |
| • Added Pin Functions table. ....   | 3  |
| • Added Handling Ratings table. ....  | 5  |
| • Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. ....              | 5  |
| • Added Thermal Information table. ....   | 6  |
| • Added –40°C to 125°C range for SN74AHCT16245 in Electrical Characteristics table. ....                  | 6  |
| • Added $T_A = -40^\circ\text{C}$ to 125°C for SN74AHCT16245 in the Switching Characteristics table. .... | 7  |
| • Added Typical Characteristics. ....   | 7  |
| • Added Detailed Description section. ....  | 9  |
| • Added Application and Implementation section. ....  | 11 |
| • Added Power Supply Recommendations and Layout sections. ....  | 12 |

## 6 Pin Configuration and Functions

SN74AHCT16245 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



Pin Functions

| PIN |                 | I/O | DESCRIPTION         |
|-----|-----------------|-----|---------------------|
| NO. | NAME            |     |                     |
| 1   | 1DIR            | I   | Direction pin 1     |
| 2   | 1B1             | I/O | 1B1 input or output |
| 3   | 1B2             | I/O | 1B2 input or output |
| 4   | GND             | —   | Ground pin          |
| 5   | 1B3             | I/O | 1B3 input or output |
| 6   | 1B4             | I/O | 1B4 input or output |
| 7   | V <sub>CC</sub> | —   | Power pin           |
| 8   | 1B5             | I/O | 1B5 input or output |
| 9   | 1B6             | I/O | 1B6 input or output |
| 10  | GND             | —   | Ground pin          |
| 11  | 1B7             | I/O | 1B7 input or output |
| 12  | 1B8             | I/O | 1B8 input or output |
| 13  | 2B1             | I/O | 2B1 input or output |
| 14  | 2B2             | I/O | 2B2 input or output |
| 15  | GND             | —   | Ground pin          |
| 16  | 2B3             | I/O | 2B3 input or output |
| 17  | 2B4             | I/O | 2B4 input or output |
| 18  | V <sub>CC</sub> | —   | Power pin           |

**Pin Functions (continued)**

| PIN |                  | I/O | DESCRIPTION         |
|-----|------------------|-----|---------------------|
| NO. | NAME             |     |                     |
| 19  | 2B5              | I/O | 2B5 input or output |
| 20  | 2B6              | I/O | 2B6 input or output |
| 21  | GND              | —   | Ground pin          |
| 22  | 2B7              | I/O | 2B7 input or output |
| 23  | 2B8              | I/O | 2B8 input or output |
| 24  | 2DIR             | —   | Direction pin 2     |
| 25  | $\overline{2OE}$ | I   | Output Enable 2     |
| 26  | 2A8              | I/O | 2A8 input or output |
| 27  | 2A7              | I/O | 2A7 input or output |
| 28  | GND              | —   | Ground pin          |
| 29  | 2A6              | I/O | 2A6 input or output |
| 30  | 2A5              | I/O | 2A5 input or output |
| 31  | V <sub>CC</sub>  | —   | Power pin           |
| 32  | 2A4              | I/O | 2A4 input or output |
| 33  | 2A3              | I/O | 2A3 input or output |
| 34  | GND              | —   | Ground pin          |
| 35  | 2A2              | I/O | 2A2 input or output |
| 36  | 2A1              | I/O | 2A1 input or output |
| 37  | 1A8              | I/O | 1A8 input or output |
| 38  | 1A7              | I/O | 1A7 input or output |
| 39  | GND              | —   | Ground pin          |
| 40  | 1A6              | I/O | 1A6 input or output |
| 41  | 1A5              | I/O | 1A5 input or output |
| 42  | V <sub>CC</sub>  | —   | Power pin           |
| 43  | 1A4              | I/O | 1A4 input or output |
| 44  | 1A3              | I/O | 1A3 input or output |
| 45  | GND              | —   | Ground pin          |
| 46  | 1A2              | I/O | 1A2 input or output |
| 47  | 1A1              | I/O | 1A1 input or output |
| 48  | $\overline{1OE}$ | I   | Output Enable 1     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |                           |                                     |                             | MIN  | MAX            | UNIT |
|--|---------------------------|-------------------------------------|-----------------------------|------|----------------|------|
| $V_{CC}$                                   | Supply voltage range      |                                     |                             | -0.5 | 7              | V    |
| $V_I$                                      | Control Inputs            | Input voltage range <sup>(2)</sup>  |                             | -0.5 | 7              | V    |
| $V_O$                                      | I/O                       | Output voltage range <sup>(2)</sup> |                             | -0.5 | $V_{CC} + 0.5$ | V    |
| $I_{IK}$                                   | Control Inputs            | Input clamp current                 | $V_I < 0$                   |      | -20            | mA   |
| $I_{OK}$                                   | I/O                       | Output clamp current                | $V_O < 0$ or $V_O > V_{CC}$ |      | ±20            | mA   |
| $I_O$                                      | Continuous output current |                                     | $V_O = 0$ to $V_{CC}$       |      | ±25            | mA   |
| Continuous current through $V_{CC}$ or GND |                           |                                     |                             |      | ±75            | mA   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 Handling Ratings

|             |                           |  |  | MIN | MAX  | UNIT |
|-------------|---------------------------|--|--|-----|------|------|
| $T_{stg}$   | Storage temperature range |  |  | -65 | 150  | °C   |
| $V_{(ESD)}$ | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              |  | 0   | 1500 | V    |
|             |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> |  | 0   | 2000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                    |  |  | SN74AHCT16245 |          | UNIT |
|---------------------|------------------------------------|--|--|---------------|----------|------|
|                     |                                    |  |  | MIN           | MAX      |      |
| $V_{CC}$            | Supply voltage                     |  |  | 4.5           | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           |  |  | 2             |          | V    |
| $V_{IL}$            | Low-level input voltage            |  |  |               | 0.8      | V    |
| $V_I$               | Input voltage                      |  |  | 0             | 5.5      | V    |
| $V_{IO}$            | Input/Output voltage, A or B pins  |  |  | 0             | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |  |  |               | -8       | mA   |
| $I_{OL}$            | Low-level output current           |  |  |               | 8        | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |  |  |               | 20       | ns/V |
| $T_A$               | Operating free-air temperature     |  |  | -40           | 125      | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | SN74AHCT16245 |      |      | UNIT |
|-------------------------------|--|---------------|------|------|------|
|                               |  | DGG           | DGV  | DL   |      |
|                               |  | 48 PINS       |      |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 68.1          | 79.3 | 61.0 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 22.6          | 31.3 | 30.8 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 35.0          | 42.3 | 32.8 |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 1.3           | 2.4  | 8.4  |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 34.7          | 41.8 | 32.5 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a           | n/a  | n/a  |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS               | V <sub>CC</sub>   | T <sub>A</sub> = 25°C |     |       | SN74AHCT16245 |      | –40°C to 125°C<br>SN74AHCT16245 |     | UNIT |
|---------------------------------|-------------------------------|---|-----------------------|-----|-------|---------------|------|---------------------------------|-----|------|
|                                 |                               |   | MIN                   | TYP | MAX   | MIN           | MAX  | MIN                             | MAX |      |
| V <sub>OH</sub>                 | I <sub>OH</sub> = –50 μA      | 4.5 V   | 4.4                   | 4.5 |       | 4.4           |      | 4.4                             | V   |      |
|                                 | I <sub>OH</sub> = –8 mA       |   | 3.94                  |     |       | 3.8           |      | 3.8                             |     |      |
| V <sub>OL</sub>                 | I <sub>OL</sub> = 50 μA       | 4.5 V   |                       |     | 0.1   |               |      | 0.1                             | V   |      |
|                                 | I <sub>OL</sub> = 8 mA        |   |                       |     | 0.36  |               | 0.44 | 0.44                            |     |      |
| I <sub>I</sub>                  | $\overline{\text{OE}}$ or DIR | V <sub>I</sub> = V <sub>CC</sub> or GND                       |                       |     | ±0.1  |               |      | ±1                              | μA  |      |
| I <sub>OZ</sub> <sup>(1)</sup>  | A or B Inputs                 | V <sub>O</sub> = V <sub>CC</sub> or GND                       |                       |     | ±0.25 |               |      | ±2.5                            | μA  |      |
| I <sub>CC</sub>                 |                               | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0   |                       |     | 4     |               |      | 40                              | μA  |      |
| ΔI <sub>CC</sub> <sup>(2)</sup> |                               | One input at 3.4 V,<br>Other inputs at V <sub>CC</sub> or GND |                       |     | 1.35  |               |      | 1.5                             | mA  |      |
| C <sub>i</sub>                  | $\overline{\text{OE}}$ or DIR | V <sub>I</sub> = V <sub>CC</sub> or GND                       |                       | 2.5 | 10    |               |      | 10                              | pF  |      |
| C <sub>io</sub>                 | A or B Inputs                 |   |                       | 4   |       |               |      |                                 | pF  |      |

(1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

### 7.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 2)

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ C$ |                    | SN74AHCT16245 |      | $T_A = -40^\circ C$ to $125^\circ C$<br>SN74AHCT16245 |      | UNIT |
|-------------|-----------------|-------------|------------------|--------------------|--------------------|---------------|------|---|------|------|
|             |                 |             |                  | TYP                | MAX                | MIN           | MAX  | MIN   | MAX  |      |
| $t_{PLH}$   | A or B          | B or A      | $C_L = 15 pF$    | 4.5 <sup>(1)</sup> | 8.5 <sup>(1)</sup> | 1             | 9.5  | 1   | 11   | ns   |
| $t_{PHL}$   |                 |             |                  | 4.5 <sup>(1)</sup> | 8.5 <sup>(1)</sup> | 1             | 9.5  | 1   | 11   |      |
| $t_{PZH}$   | $\overline{OE}$ | A or B      | $C_L = 15 pF$    | 8.9 <sup>(1)</sup> | 13 <sup>(1)</sup>  | 1             | 14   | 1   | 15   | ns   |
| $t_{PZL}$   |                 |             |                  | 8.9 <sup>(1)</sup> | 13 <sup>(1)</sup>  | 1             | 14   | 1   | 15   |      |
| $t_{PHZ}$   | $\overline{OE}$ | A or B      | $C_L = 15 pF$    | 9.2 <sup>(1)</sup> | 14 <sup>(1)</sup>  | 1             | 15   | 1   | 15.7 | ns   |
| $t_{PLZ}$   |                 |             |                  | 9.2 <sup>(1)</sup> | 14 <sup>(1)</sup>  | 1             | 15   | 1   | 15.7 |      |
| $t_{PLH}$   | A or B          | B or A      | $C_L = 50 pF$    | 7                  | 9.5                | 1             | 10.5 | 1   | 12   | ns   |
| $t_{PHL}$   |                 |             |                  | 5.3                | 9.5                | 1             | 10.5 | 1   | 12   |      |
| $t_{PZH}$   | $\overline{OE}$ | A or B      | $C_L = 50 pF$    | 8.3                | 14                 | 1             | 15   | 1   | 16   | ns   |
| $t_{PZL}$   |                 |             |                  | 8.3                | 14                 | 1             | 15   | 1   | 16   |      |
| $t_{PHZ}$   | $\overline{OE}$ | A or B      | $C_L = 50 pF$    | 8                  | 14                 | 1             | 15   | 1   | 15.7 | ns   |
| $t_{PLZ}$   |                 |             |                  | 8                  | 14                 | 1             | 15   | 1   | 15.7 |      |
| $t_{sk(o)}$ |                 |             | $C_L = 50 pF$    |                    | 1 <sup>(2)</sup>   |               | 1    |   | 1    | ns   |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

### 7.7 Noise Characteristics

$V_{CC} = 5 V$ ,  $C_L = 50 pF$ ,  $T_A = 25^\circ C$ <sup>(1)</sup>

| PARAMETER   | DESCRIPTION                            | SN74AHCT16245 |      |      | UNIT |
|-------------|--|---------------|------|------|------|
|             |  | MIN           | TYP  | MAX  |      |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |               | 0.6  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |               | -0.6 | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |               | 4.8  |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2             |      |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |               |      | 0.8  | V    |

(1) Characteristics are for surface-mount packages only.

### 7.8 Operating Characteristics

$V_{CC} = 5 V$ ,  $T_A = 25^\circ C$

| PARAMETER | TEST CONDITIONS      | TYP | UNIT |
|-----------|----------------------|-----|------|
| $C_{pd}$  | No load, $f = 1 MHz$ | 17  | pF   |

### 7.9 Typical Characteristics

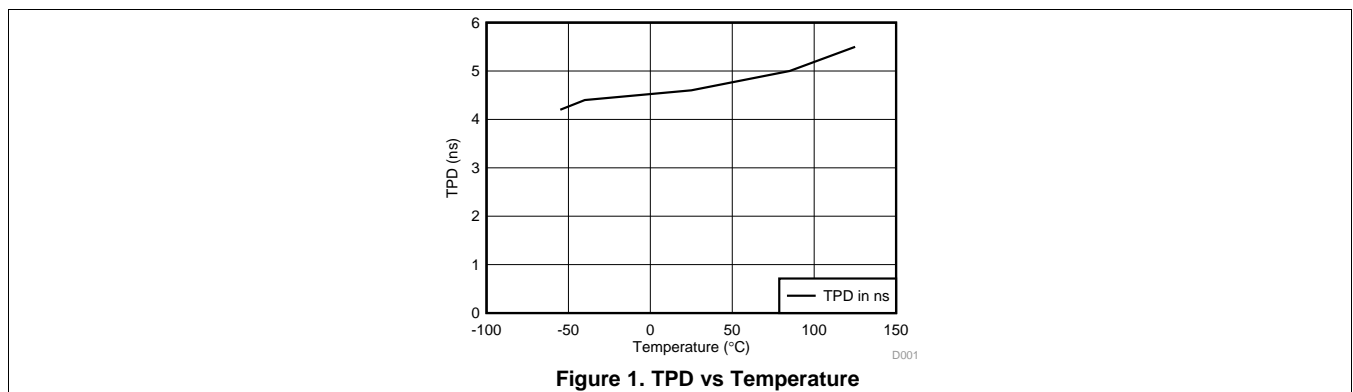
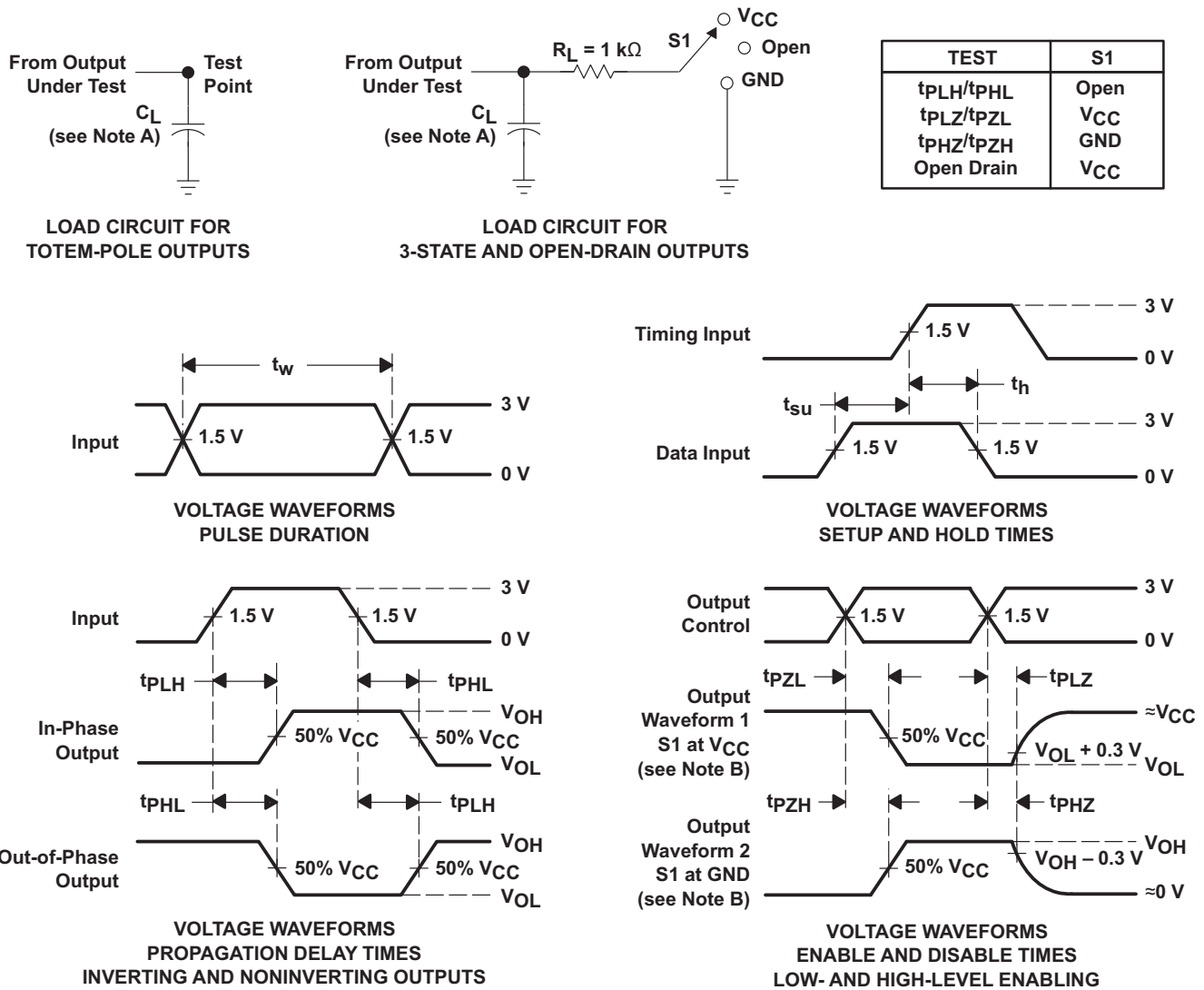


Figure 1. TPD vs Temperature

## 8 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



## 9 Detailed Description

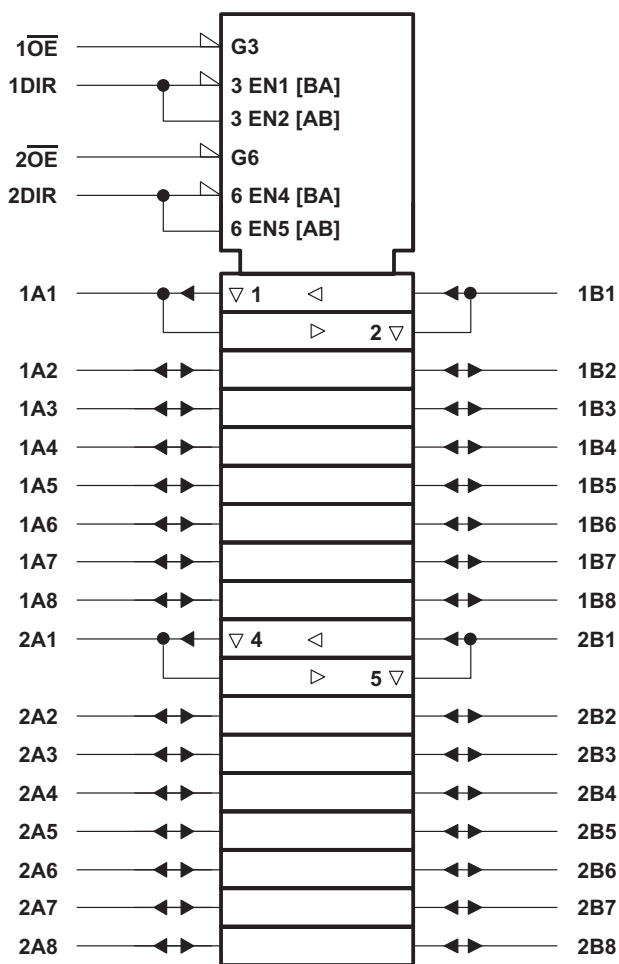
### 9.1 Overview

The SN74AHCT16245 device is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

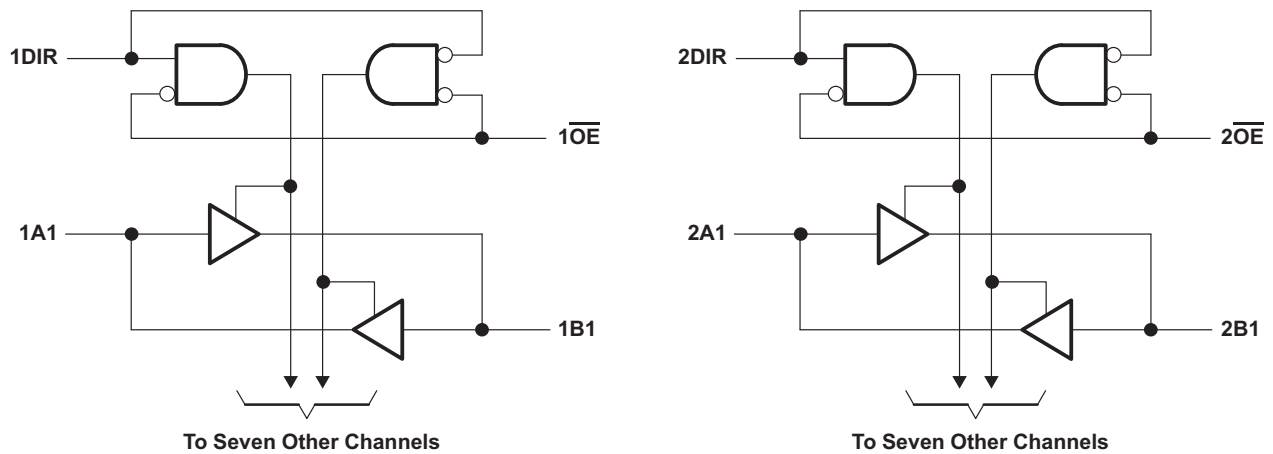
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.2 Functional Block Diagrams



A. † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 3. Logic Symbol

**Functional Block Diagrams (continued)**

**Figure 4. Logic Diagram (Positive Logic)**
**9.3 Feature Description**

- TTL inputs
  - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

**9.4 Device Functional Modes**
**Table 1. Function Table  
(Each 8-bit Transceiver)**

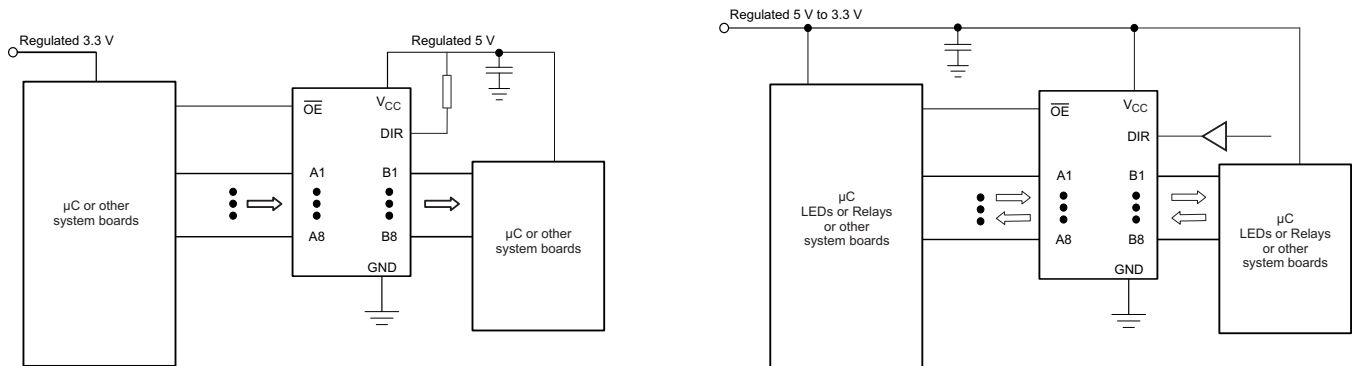
| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

## 10 Application and Implementation

### 10.1 Application Information

The SN74AHCT16245 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V  $V_{IL}$  and 2-V  $V_{IH}$ . This feature makes the device ideal for translating up from 3.3 V to 5 V. Figure 6 shows this type of translation.

### 10.2 Typical Application



**Figure 5. Typical Application Diagram**

#### 10.2.1 Design Requirements

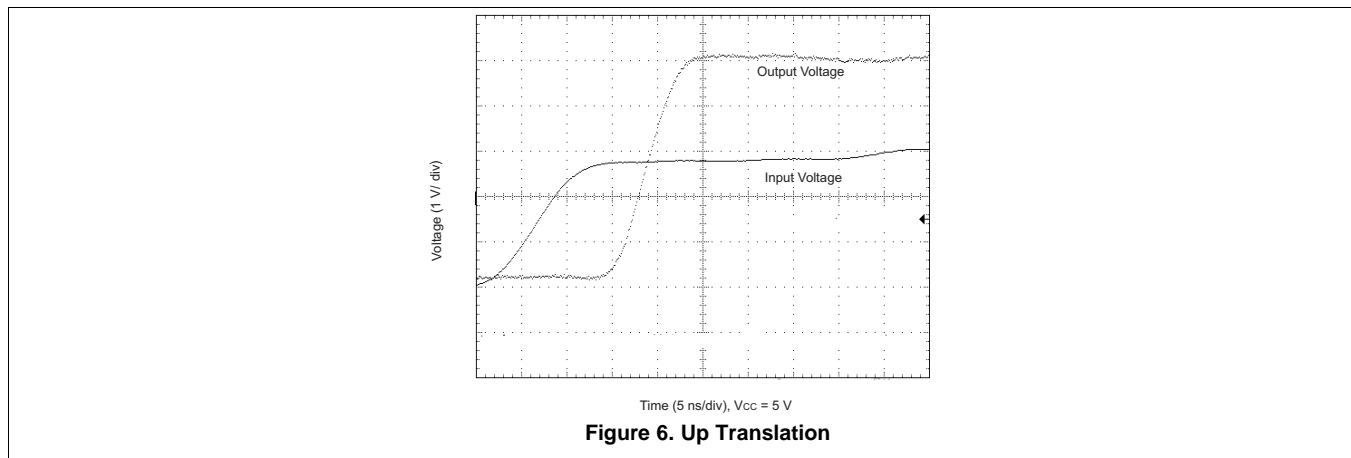
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions:
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended and if there are multiple  $V_{CC}$  pins than 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

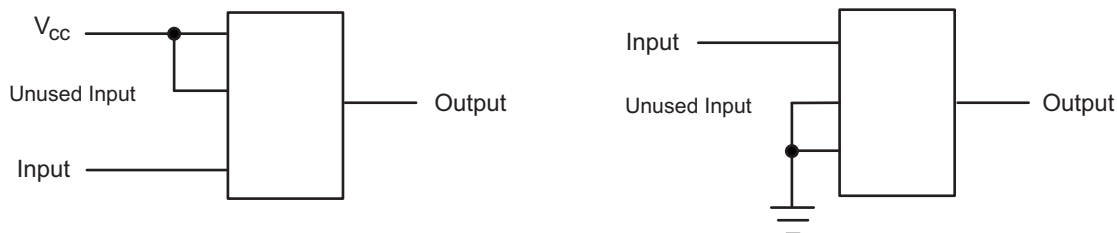
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

### 12.2 Layout Example



**Figure 7. Layout Diagram**

## 13 Device and Documentation Support

### 13.1 Trademarks

Widebus is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74AHCT16245DGGRG4 | ACTIVE        | TSSOP        | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | AHCT16245               | <a href="#">Samples</a> |
| 74AHCT16245DLRG4  | ACTIVE        | SSOP         | DL              | 48   | 1000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | AHCT16245               | <a href="#">Samples</a> |
| SN74AHCT16245DGGR | ACTIVE        | TSSOP        | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | AHCT16245               | <a href="#">Samples</a> |
| SN74AHCT16245DGVR | ACTIVE        | TVSOP        | DGV             | 48   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | HF245                   | <a href="#">Samples</a> |
| SN74AHCT16245DL   | ACTIVE        | SSOP         | DL              | 48   | 25          | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | AHCT16245               | <a href="#">Samples</a> |
| SN74AHCT16245DLR  | ACTIVE        | SSOP         | DL              | 48   | 1000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | AHCT16245               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT16245DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74AHCT16245DGVR | TVSOP        | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |
| SN74AHCT16245DLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT16245DGGR | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74AHCT16245DGVR | TVSOP        | DGV             | 48   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74AHCT16245DLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

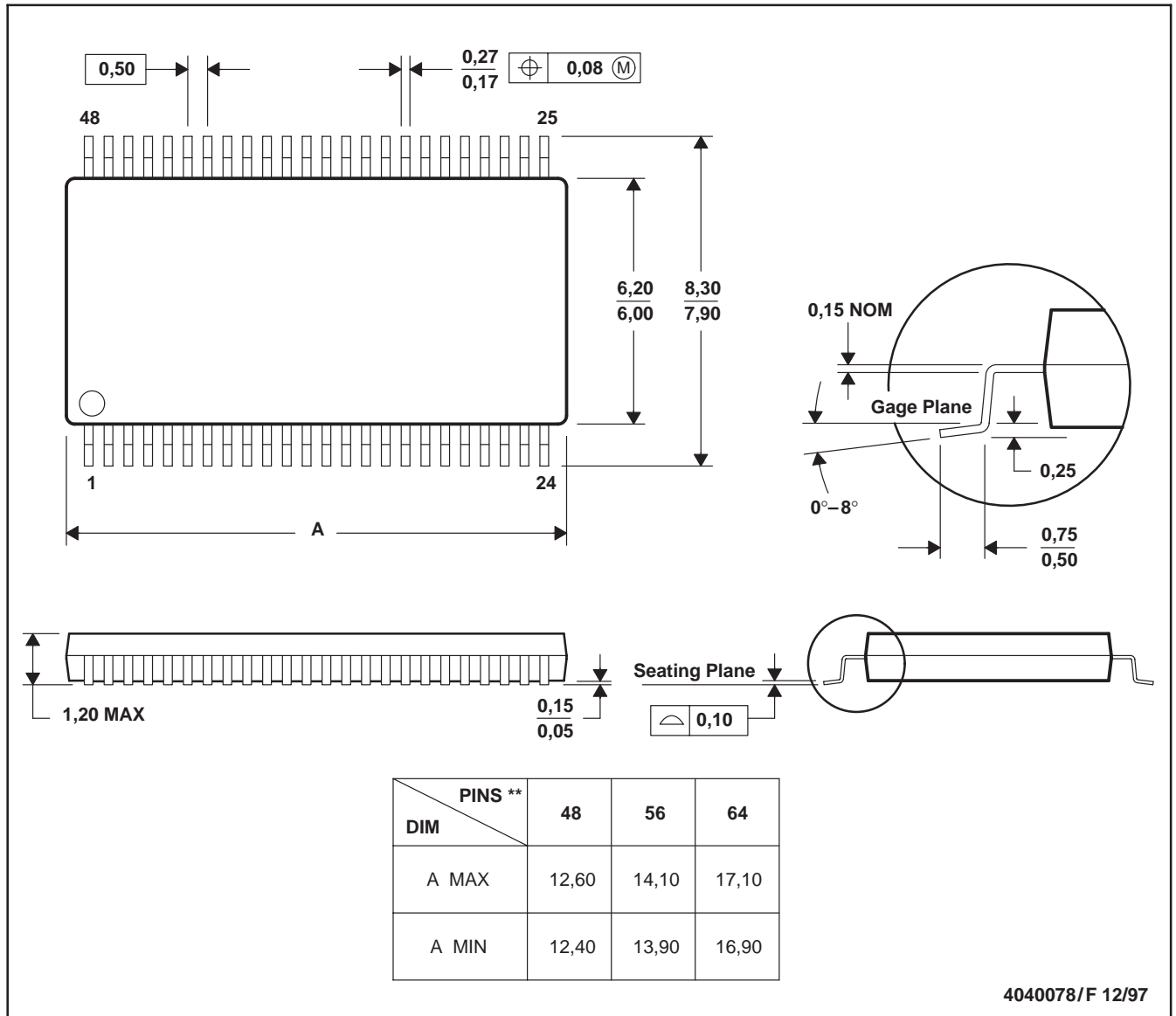


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated