LM5109A High Voltage 1A Peak Half Bridge Gate Driver

Check for Samples: LM5109A

FEATURES

- **Drives Both a High-Side and Low-Side N-Channel MOSFET**
- **1A peak Output Current (1.0A Sink / 1.0A Source)**
- **Independent TTL Compatible Inputs**
- **Bootstrap Supply Voltage to 108V DC**
- **Fast Propagation Times (30 ns Typical)**
- **Drives 1000 pF Load with 15ns Rise and Fall Times**
- **Excellent Propagation Delay Matching (2 ns Typical)**
- **Supply Rail Under-Voltage Lockout**
- **Low Power Consumption**
- **Pin Compatible with ISL6700**

TYPICAL APPLICATIONS

- **Current Fed Push-Pull Converters**
- **Half and Full Bridge Power Converters**
- **Solid State Motor Drives**
- **Two Switch Forward Power Converters**

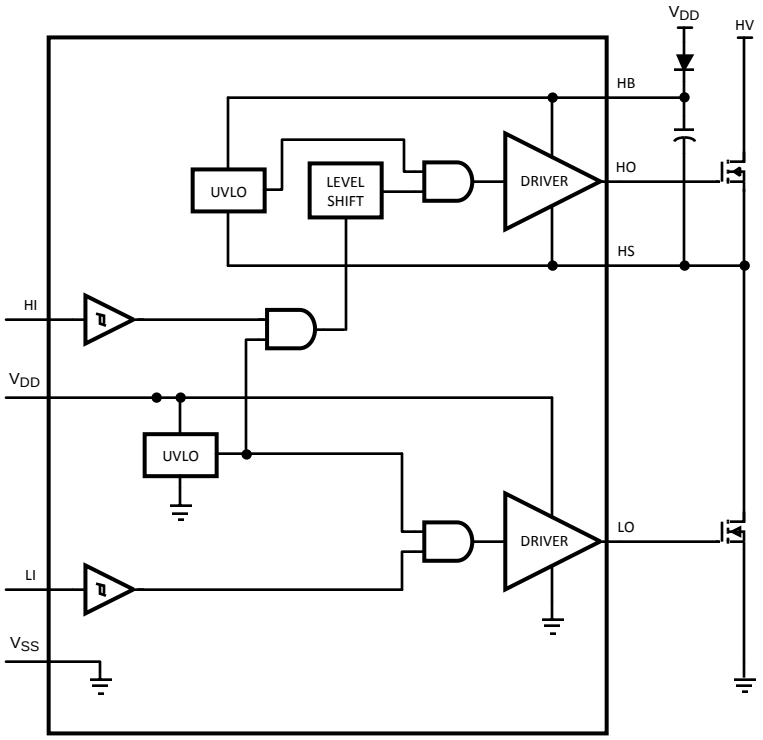
DESCRIPTION

The LM5109A is a cost effective, high voltage gate driver designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 90V. The outputs are independently controlled with TTL compatible input thresholds. The robust level shift technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. The device is available in the SOIC and the thermally enhanced WSON packages.

Package

- SOIC
- WSON-8 (4 mm x 4 mm)

Simplified Block Diagram



Connection Diagrams

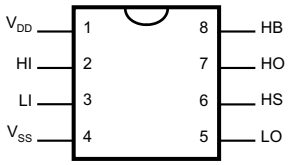


Figure 1. 8-Lead SOIC
See D Package

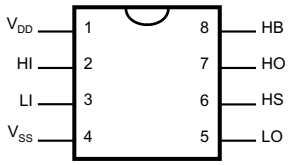


Figure 2. 8-Lead WSON
See NGT0008A Package

PIN DESCRIPTIONS

Pin #		NAME	DESCRIPTION	APPLICATION INFORMATION
SOIC	WSON(1)			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HI	High side control input	The HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open
3	3	LI	Low side control input	The LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.
4	4	V_{SS}	Ground reference	All signals are referenced to this ground.
5	5	LO	Low side gate driver output	Connect to the gate of the low-side N- MOS device.
6	6	HS	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	7	HO	High side gate driver output	Connect to the gate of the high-side N-MOS device.

(1) For WSON package it is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane should extend out from underneath the package to improve heat dissipation.

PIN DESCRIPTIONS (continued)

Pin #		NAME	DESCRIPTION	APPLICATION INFORMATION
SOIC	WSON(1)			
8	8	HB	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{DD} to V_{SS}	–0.3V to 18V
HB to HS	−0.3V to 18V
LI or HI to V_{SS}	−0.3V to V_{DD} + 0.3V
LO to V_{SS}	−0.3V to V_{DD} + 0.3V
HO to V_{SS}	V_{HS} − 0.3V to V_{HB} + 0.3V
HS to V_{SS}(3)	−5V to 90V
HB to V_{SS}	108V
Junction Temperature	–40°C to 150°C
Storage Temperature Range	−55°C to 150°C
ESD Rating HBM(4)	1.5 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics .
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed –5V.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

V_{DD}	8V to 14V
HS(1)	−1V to 90V
HB	V_{HS} + 8V to V_{HS} + 14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to 125°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed –5V.

Electrical Characteristics

Specifications in standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO(1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents						
I_{DD}	V_{DD} quiescent current	LI = HI = 0V		0.3	**0.6**	mA
I_{DDO}	V_{DD} operating current	f = 500 kHz		1.8	**2.9**	mA
I_{HB}	Total HB quiescent current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB operating current	f = 500 kHz		1.4	**2.8**	mA

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications in standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO(1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{HBS}	HB to V_{SS} current, quiescent	V_{HS} = V_{HB} = 90V		0.1	**10**	µA
I_{HBSO}	HB to V_{SS} current, operating	f = 500 kHz		0.5		mA
Input Pins LI and HI						
V_{IL}	Low-level input voltage threshold		**0.8**	1.8		V
V_{IH}	High-level input voltage threshold			1.8	**2.2**	V
R_I	Input pulldown resistance		**100**	200	**500**	kΩ
Under-Voltage Protection						
V_{DDR}	V_{DD} rising threshold	V_{DDR} = V_{DD} – V_{SS}	**6.0**	6.7	**7.4**	V
V_{DDH}	V_{DD} threshold hysteresis			0.5		V
V_{HBR}	HB rising threshold	V_{HBR} = V_{HB} – V_{HS}	**5.7**	6.6	**7.1**	V
V_{HBH}	HB threshold hysteresis			0.4		V
LO Gate Driver						
V_{OLL}	Low-level output voltage	I_{LO} = 100 mA, V_{OHL} = V_{LO} – V_{SS}		0.38	**0.65**	V
V_{OHL}	High-level output voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD} – V_{LO}		0.72	**1.20**	V
I_{OHL}	Peak pullup current	V_{LO} = 0V		1.0		A
I_{OLL}	Peak pulldown current	V_{LO} = 12V		1.0		A
HO Gate Driver						
V_{OLH}	Low-level output voltage	I_{HO} = 100 mA, V_{OLH} = V_{HO} – V_{HS}		0.38	**0.65**	V
V_{OHH}	High-level output voltage	I_{HO} = −100 mA, V_{OHH} = V_{HB} – V_{HO}		0.72	**1.20**	V
I_{OHH}	Peak pullup current	V_{HO} = 0V		1.0		A
I_{OLH}	Peak pulldown current	V_{HO} = 12V		1.0		A
Thermal Resistance						
θ_{JA}	Junction to ambient	SOIC(2)(3)		160		°C/W
		WSON(2)(3)		40		

(2) 4-layer board with Cu finished thicknesses 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.
(3) The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.

Switching Characteristics

Specifications in standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LM5109A						
t_{LPHL}	Lower turn-off propagation delay (LI falling to LO falling)			30	**56**	ns
t_{HPHL}	Upper turn-off propagation delay (HI falling to HO falling)			30	**56**	ns
t_{LPLH}	Lower turn-on propagation delay (LI rising to LO rising)			32	**56**	ns
t_{HPLH}	Upper turn-on propagation delay (HI rising to HO rising)			32	**56**	ns
t_{MON}	Delay matching: lower turn-on and upper turn-off			2	**15**	ns
t_{MOFF}	Delay matching: lower turn-off and upper turn-on			2	**15**	ns
t_{RC}, t_{FC}	Either output rise or fall time	C_L = 1000 pF		15	-	ns
t_{PW}	Minimum input pulse width that changes the output			50		ns

Typical Performance Characteristics

V_{DD} Operating Current vs Frequency

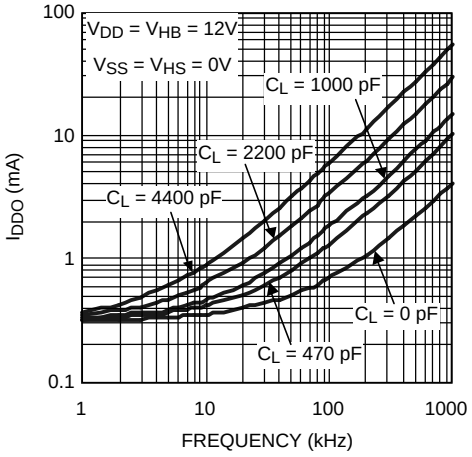


Figure 3.

HB Operating Current vs Frequency

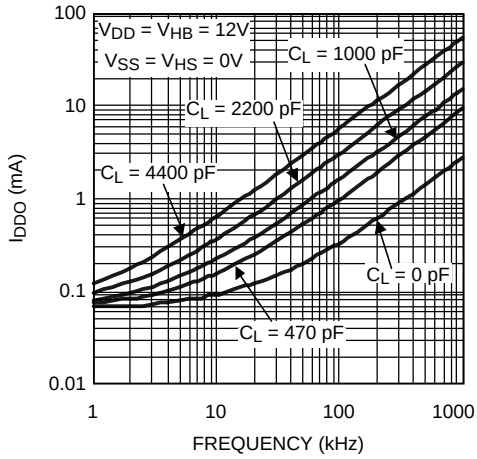


Figure 4.

Operating Current vs Temperature

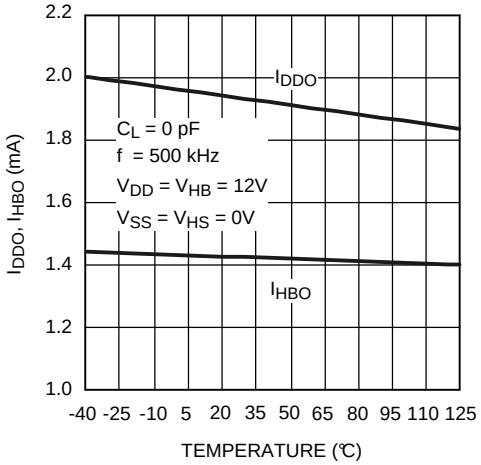


Figure 5.

Quiescent Current vs Temperature

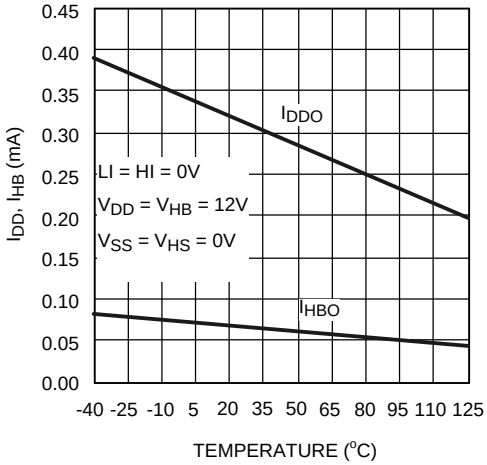


Figure 6.

Quiescent Current vs Voltage

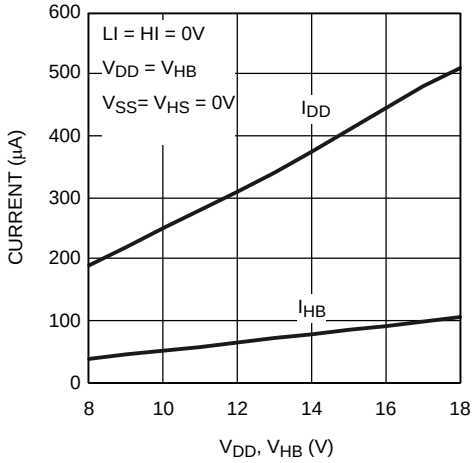


Figure 7.

Propagation Delay vs Temperature

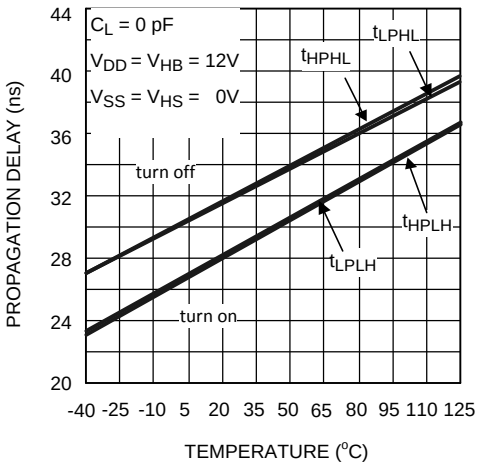


Figure 8.

Typical Performance Characteristics (continued)

LO and HO High Level Output Voltage vs Temperature

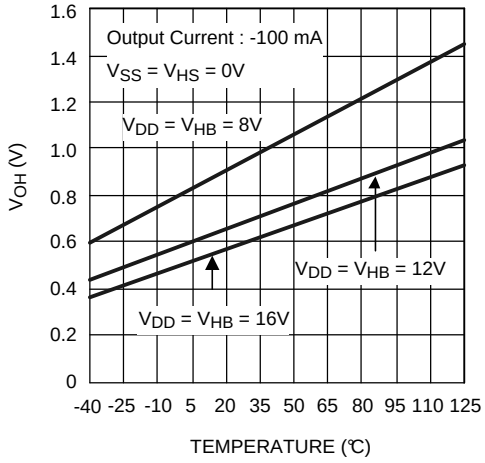


Figure 9.

LO and HO Low Level Output Voltage vs Temperature

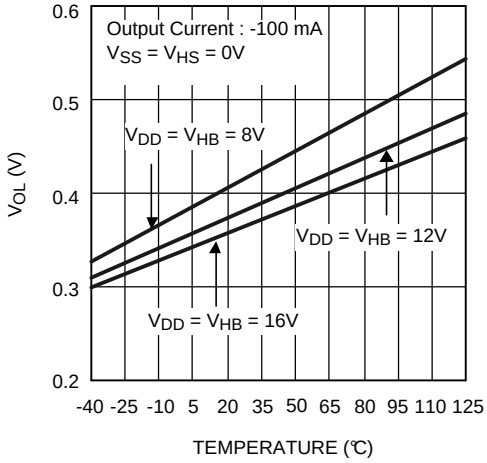


Figure 10.

Undervoltage Rising Thresholds vs Temperature

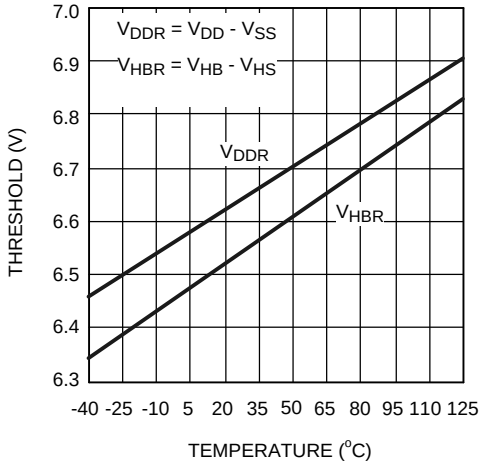


Figure 11.

Undervoltage Hysteresis vs Temperature

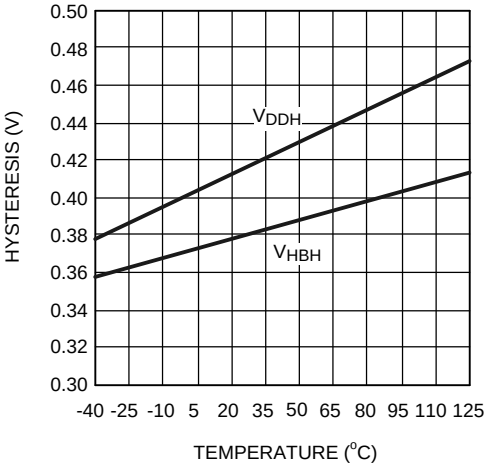


Figure 12.

Input Thresholds vs Temperature

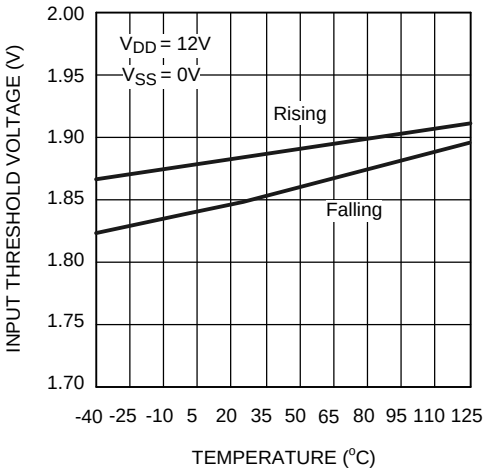


Figure 13.

Input Thresholds vs Supply Voltage

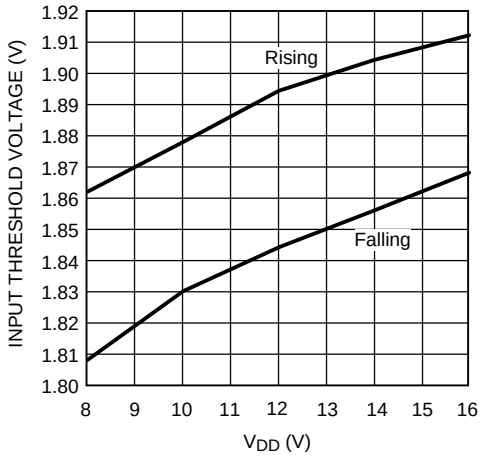


Figure 14.

Timing Diagram

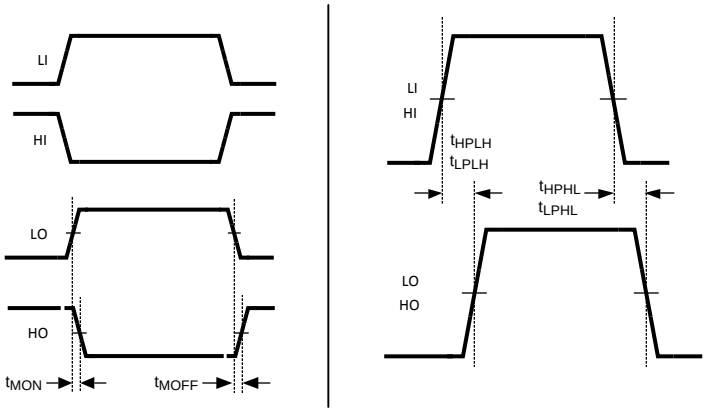


Figure 15.

Layout Considerations

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR / ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the top MOSFET source and the of the bottom MOSFET drain (synchronous rectifier) must be minimized.
4. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   – The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less. Hence, if the HS pin transient voltage is –5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The

capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5109AMA	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	L5109 AMA	Samples
LM5109AMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 AMA	Samples
LM5109AMAX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	L5109 AMA	Samples
LM5109AMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 AMA	Samples
LM5109ASD	ACTIVE	WSON	NGT	8	1000	TBD	Call TI	Call TI	-40 to 125	5109ASD	Samples
LM5109ASD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5109ASD	Samples
LM5109ASDX	ACTIVE	WSON	NGT	8		TBD	Call TI	Call TI	-40 to 125	5109ASD	Samples
LM5109ASDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5109ASD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

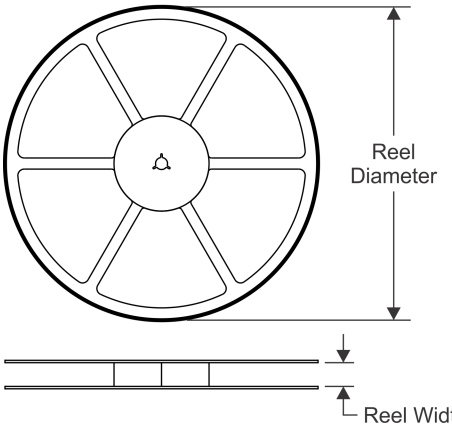
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

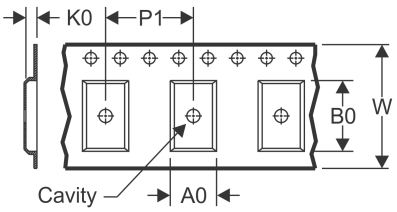
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

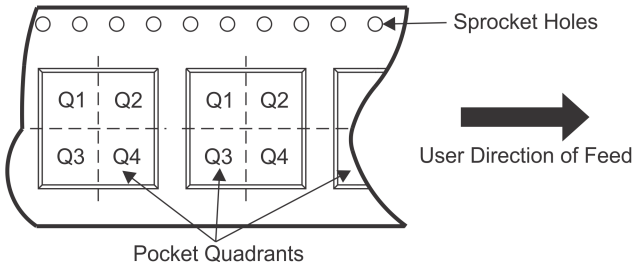


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

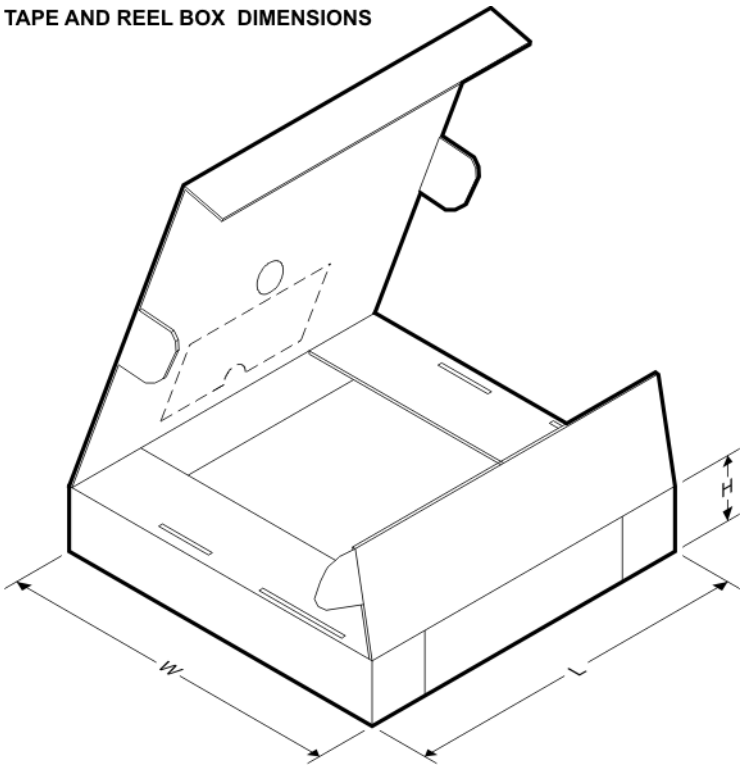
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5109AMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5109ASD	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5109ASD/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5109ASDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

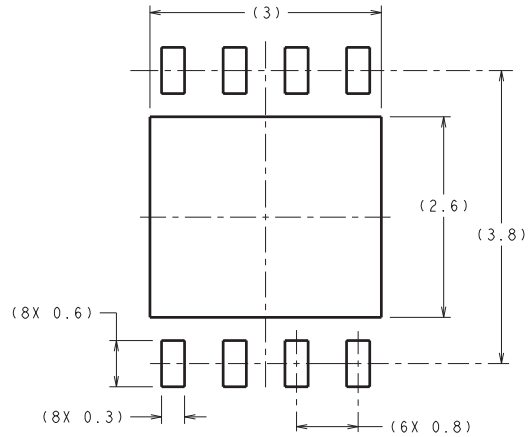
TAPE AND REEL BOX DIMENSIONS



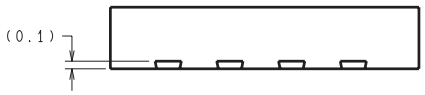
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5109AMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5109ASD	WSON	NGT	8	1000	210.0	185.0	35.0
LM5109ASD/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LM5109ASDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

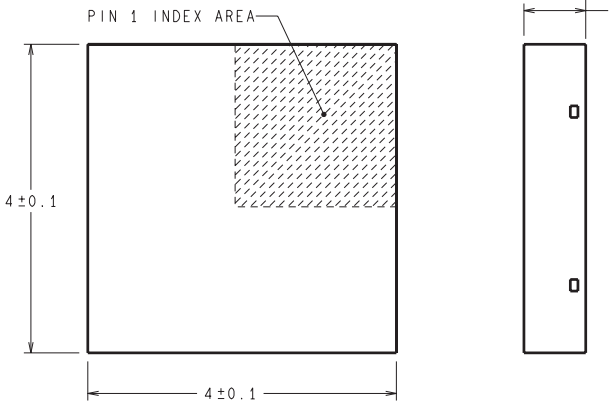
NGT0008A

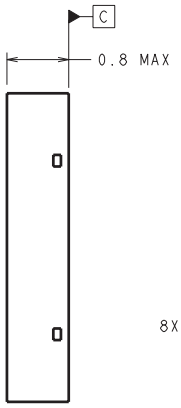


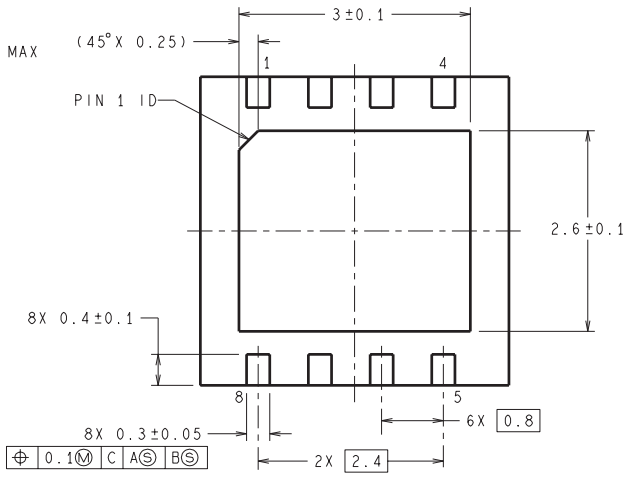
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

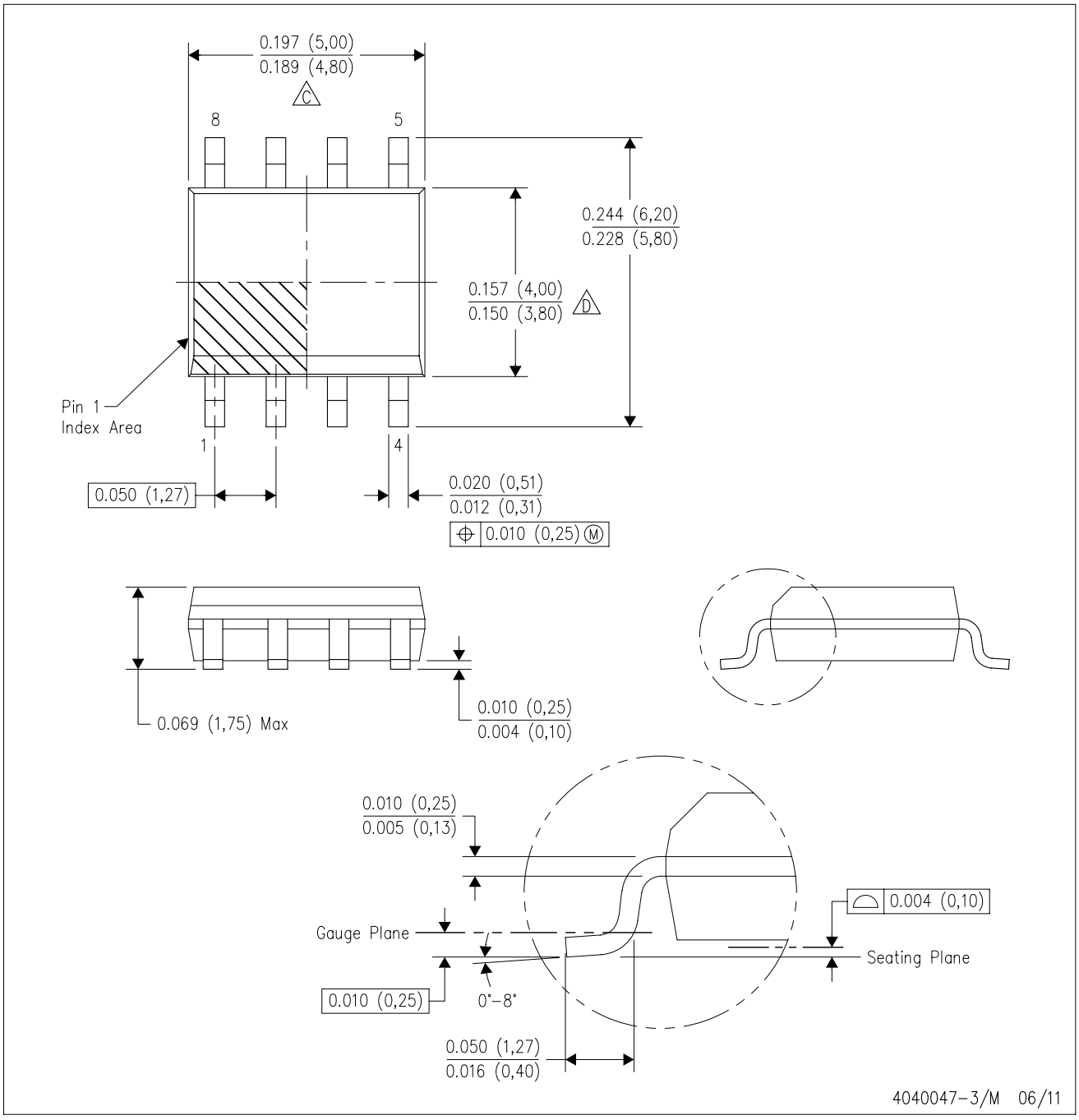






SDC08A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265