16-Bit, 100 kSPS, Differential ADC

AD7675

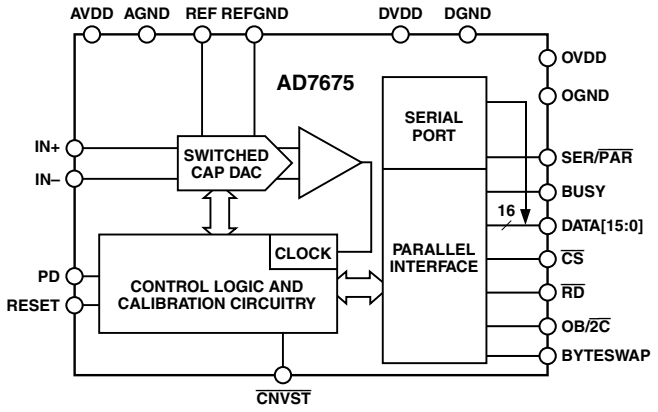
FEATURES

Throughput: 100 kSPS
INL: ±1.5 LSB Max (±0.0015% of Full Scale)
16 Bits Resolution with No Missing Codes
S/(N+D): 94 dB Typ @ 45 kHz
THD: –110 dB Typ @ 45 kHz
Differential Input Range: ±2.5 V
Both AC and DC Specifications
No Pipeline Delay
Parallel (8 Bits/16 Bits) and Serial 5 V/3 V Interface
SPI™/QSPI™/MICROWIRE™/DSP Compatible
Single 5 V Supply Operation
15 mW Typical Power Dissipation, 15 µW @ 100 SPS
Power-Down Mode: 7 µW Max
Packages: 48-Lead Quad Flatpack (LQFP),
46-Lead Frame Chip Scale (LFCSP)
Pin-to-Pin Compatible with the AD7660
Replacement of AD676, AD677

APPLICATIONS

CT Scanners
Data Acquisition
Instrumentation
Spectrum Analysis
Medical Instruments
Battery-Powered Systems
Process Control

FUNCTIONAL BLOCK DIAGRAM



PulSAR Selection

Type/kSPS	100–250	500–570	1000
Pseudo Differential	AD7660	AD7650 AD7664	
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677

GENERAL DESCRIPTION

The AD7675 is a 16-bit, 100 kSPS, charge redistribution SAR, fully differential analog-to-digital converter that operates from a single 5 V power supply. The part contains a high speed 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports.

The AD7675 is hardware factory calibrated and is comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

It is fabricated using Analog Devices' high performance, 0.6 micron CMOS process and is available in a 48-lead LQFP or a tiny 48-lead LFCSP with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Excellent INL
   The AD7675 has a maximum integral nonlinearity of 1.5 LSB with no missing 16-bit code.
2. Superior AC Performances
   The AD7675 has a minimum dynamic of 92 dB, 94 dB typical.
3. Fast Throughput
   The AD7675 is a 100 kSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
4. Single-Supply Operation
   The AD7675 operates from a single 5 V supply and typically dissipates only 17 mW. Its power dissipation decreases with the throughput to, for instance, only 15 µW at a 100 SPS throughput. It consumes 7 µW maximum when in power-down.
5. Serial or Parallel Interface
   Versatile parallel (8 bits or 16 bits) or 2-wire serial interface arrangement compatible with either 3 V or 5 V logic.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD7675—SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	–0.1		+3	V
Analog Input CMRR	f_{IN} = 10 kHz		79		dB
Input Current	100 kSPS Throughput		1		µA
Input Impedance		See Analog Input Section			
THROUGHPUT SPEED					
Complete Cycle				10	µs
Throughput Rate		0		100	kSPS
DC ACCURACY					
Integral Linearity Error		–1.5		+1.5	LSB[1]
No Missing Codes		16			Bits
Transition Noise			0.35		LSB
+Full-Scale Error[2]		–22		+22	LSB
–Full-Scale Error[2]		–22		+22	LSB
Zero Error[2]		–8		+8	LSB
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.5		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz	92	94		dB[3]
	f_{IN} = 45 kHz		94		dB[3]
Spurious Free Dynamic Range	f_{IN} = 20 kHz	104.5	110		dB[3]
	f_{IN} = 45 kHz		110		dB[3]
Total Harmonic Distortion	f_{IN} = 20 kHz		–110	–103.5	dB[3]
	f_{IN} = 45 kHz		–110		dB[3]
Signal-to-(Noise+Distortion)	f_{IN} = 20 kHz	92	94		dB[3]
	f_{IN} = 45 kHz		94		dB[3]
	f_{IN} = 45 kHz, –60 dB Input		34		dB[3]
–3 dB Input Bandwidth			3.9		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			8.75	µs
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD – 1.85	V
External Reference Current Drain	100 kSPS Throughput		35		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format		Parallel or Serial 16-Bit Conversion Results Available			
Pipeline Delay		Immediately After Completed Conversion			
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –100 µA	OVDD – 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[4]	V
Operating Current	300 kSPS Throughput				
AVDD			3		mA
DVDD[5]			750		µA
OVDD[5]			7.5		µA
Power Dissipation[5]	100 kSPS Throughput		17	25	mW
	100 SPS Throughput		15		µW
In Power-Down Mode[5]				7	µW
TEMPERATURE RANGE[7]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means Least Significant Bit. With the ±2.5 V input range, one LSB is 76.3 µV.
[2]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[4]The max should be the minimum of 5.25 V and DVDD + 0.3 V.
[5]Tested in Parallel Reading Mode.
[6]With OVDD below DVDD + 0.3 V and all digital inputs forced to DVDD or DGND, respectively.
[7]Contact factory for extended temperature range.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

	Symbol	Min	Typ	Max	Unit
Refer to Figures 11 and 12					
Convert Pulsewidth	t_1	5			ns
Time Between Conversions	t_2	10			µs
$\overline{\text{CNVST}}$ LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read After Convert Mode	t_4			1.25	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time	t_7			1.25	µs
Acquisition Time	t_8	8.75			µs
RESET Pulsewidth	t_9	10			ns
Refer to Figures 13, 14, and 15 (Parallel Interface Modes)					
$\overline{\text{CNVST}}$ LOW to DATA Valid Delay	t_{10}			1.25	µs
DATA Valid to BUSY LOW Delay	t_{11}	45			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figures 16 and 17 (Master Serial Interface Modes)[1]					
$\overline{\text{CS}}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{\text{CS}}$ LOW to Internal SCLK Valid Delay	t_{15}			10	ns
$\overline{\text{CS}}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{\text{CNVST}}$ LOW to SYNC Delay	t_{17}		525		ns
SYNC Asserted to SCLK First Edge Delay[2]	t_{18}	3			ns
Internal SCLK Period[2]	t_{19}	25		40	ns
Internal SCLK HIGH[2]	t_{20}	12			ns
Internal SCLK LOW[2]	t_{21}	7			ns
SDOUT Valid Setup Time[2]	t_{22}	4			ns
SDOUT Valid Hold Time[2]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{24}	3			ns
$\overline{\text{CS}}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{\text{CS}}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{\text{CS}}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read After Convert[2]	t_{28}		See Table I		µs
$\overline{\text{CNVST}}$ LOW to SYNC Asserted Delay	t_{29}		1.25		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figures 18 and 19 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES

[1]In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

[2]In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

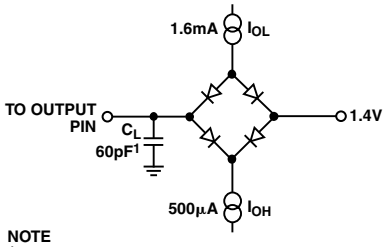
Table I. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]		0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Typical	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
Busy High Width Maximum	t_{28}	2	2.5	3.5	5.75	µs

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
IN+[2], IN–[2], REF, REFGND . . . . . AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences
AGND, DGND, OGND . . . . . ±0.3 V
Supply Voltages
AVDD, DVDD, OVDD . . . . . –0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD . . . . . ±7 V
DVDD to OVDD . . . . . –0.3 V to +7 V
Digital Inputs . . . . . –0.3 V to DVDD + 0.3 V
Internal Power Dissipation[3] . . . . . 700 mW
Internal Power Dissipation[4] . . . . . 2.5 W
Junction Temperature . . . . . 150° C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for device in free air: 48-Lead LQFP: θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[4]Specification is for device in free air: LFCSP: θ_{JA} = 26°C/W



NOTE
[1]IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

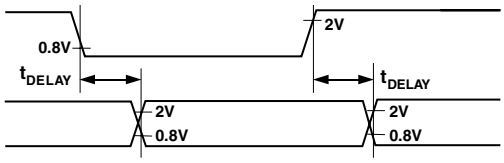


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7675AST	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7675ASTRL	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7675ACP	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7675ACPRL	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7675CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES
[1]This board can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7675 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1	AGND	P	Analog Power Ground Pin
2	AVDD	P	Input Analog Power Pins. Nominally 5 V.
3, 6, 7, 40–42, 44–48	NC		No Connect
4	BYTESWAP	DI	Parallel Mode Selection (8-Bit/16-Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/$\overline{2C}$	DI	Straight Binary/Binary Two's Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	DATA[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	DATA[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW and RDC/SDIN is LOW, which is the serial master read after convert mode. These inputs, part of the serial port, are used to slow down, if desired, the internal serial clock that clocks the data output. In the other serial modes, these pins are high impedance outputs.
13	DATA[4] or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	DATA[5] or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	DATA[6] or INVSCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 6 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	DATA[7] or RDC/SDIN	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 7 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data is output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply of the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground

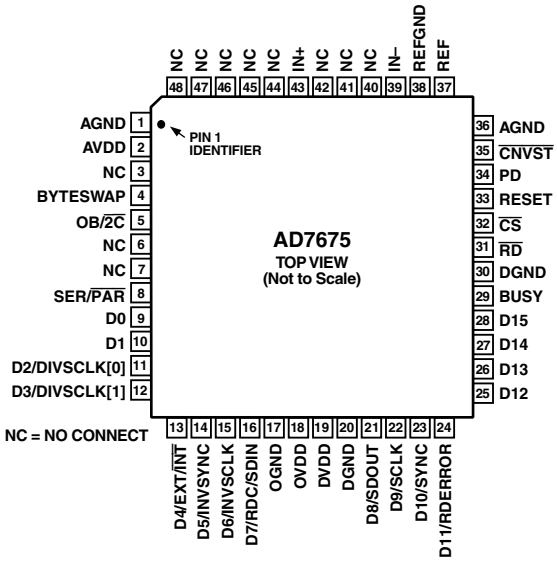
PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Type	Description
21	DATA[8] or SDOUT	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 8 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7675 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/$\overline{2C}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	DATA[9] or SCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 9 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ Pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK Pin.
23	DATA[10] or SYNC	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 10 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	DATA[11] or RDERROR	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 11 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH and EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	DATA[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data output bus. These pins are always outputs regardless of the state of SER/$\overline{PAR}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7675. Current conversion if any is aborted.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	$\overline{DI}$	Start Conversion. If $\overline{CNVST}$ is HIGH when the acquisition phase (t_8) is complete, the next falling edge on $\overline{CNVST}$ puts the internal sample/hold into the hold state and initiates a conversion. This mode is the most appropriate if low sampling jitter is desired. If $\overline{CNVST}$ is LOW when the acquisition phase (t_8) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must Be Tied to Analog Ground
37	REF	AI	Reference Input Voltage
38	REFGND	AI	Reference Input Analog Ground
39	IN–	AI	Differential Negative Analog Input
43	IN+	AI	Differential Positive Analog Input

NOTES
AI = Analog Input
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

PIN CONFIGURATION

48-Lead LQFP
(ST-48)



DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Integral Nonlinearity is the maximum deviation of a straight line drawn through the transfer function of the actual ADC. The deviation is measured from the middle of each code.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

+FULL-SCALE ERROR

The last transition (from 011 . . . 10 to 011 . . . 11 in two's complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal +full scale (+2.499886 V for the ±2.5 V range). The +full-scale error is the deviation of the actual level of the last transition from the ideal level.

–FULL-SCALE ERROR

The first transition (from 100 . . . 00 to 100 . . . 01 in two's complement coding) should occur for an analog voltage 1/2 LSB above the nominal –full scale (–2.499962 V for the ±2.5 V range). The –full-scale error is the deviation of the actual level of the last transition from the ideal level.

BIPOLAR ZERO ERROR

The bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = \left(S / \left[N + D\right]_{dB} - 1.76\right) / 6.02$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL-TO-(NOISE + DISTORTION) RATIO (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

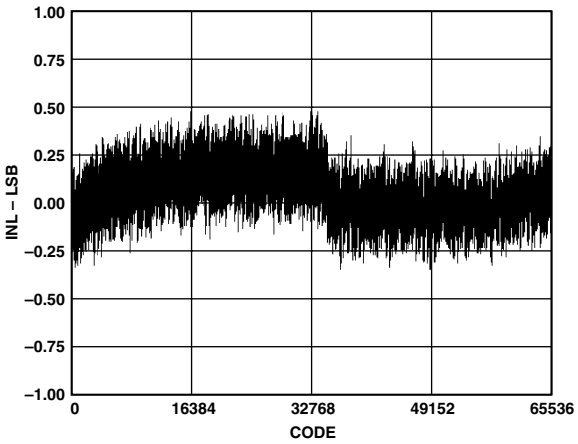
APERTURE DELAY

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

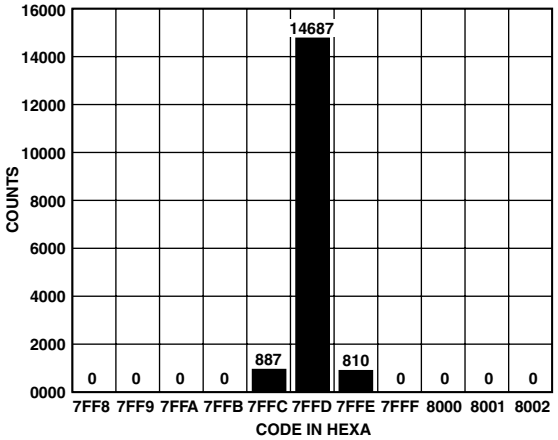
TRANSIENT RESPONSE

The time required for the AD7675 to achieve its rated accuracy after a full-scale step function is applied to its input.

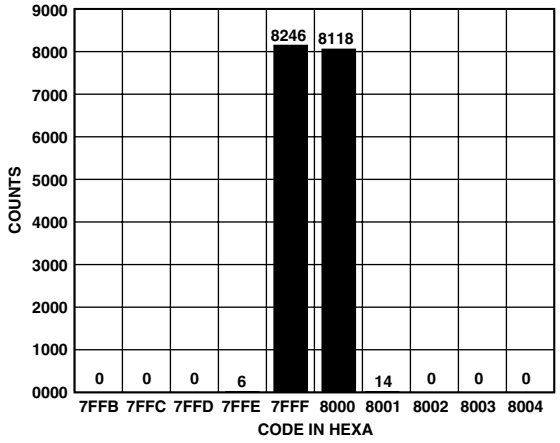
AD7675–Typical Performance Characteristics



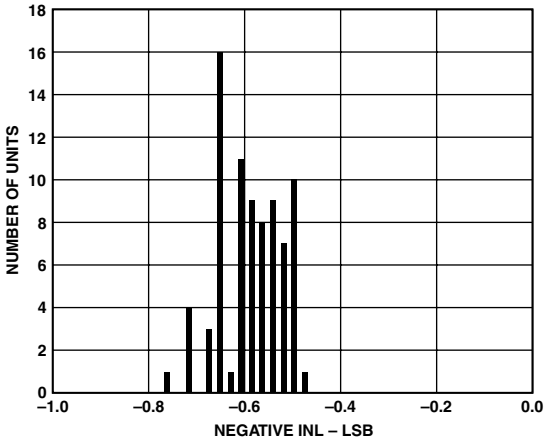
TPC 1. Integral Nonlinearity vs. Code



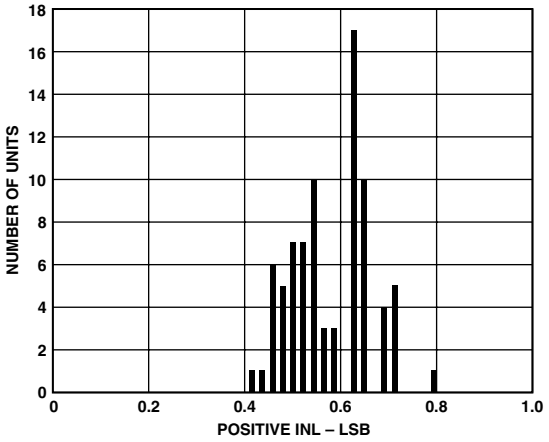
TPC 4. Histogram of 16,384 Conversions of a DC Input at the Code Center



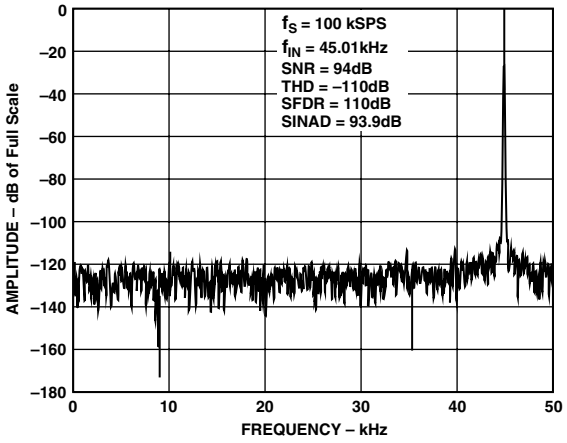
TPC 2. Histogram of 16,384 Conversions of a DC Input at the Code Transition



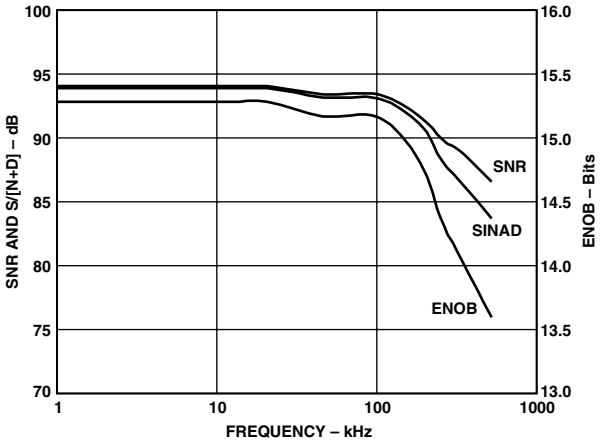
TPC 5. Typical Negative INL Distribution (40 Units)



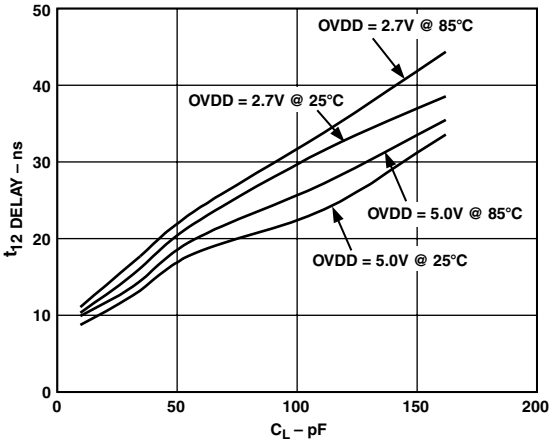
TPC 3. Typical Positive INL Distribution (40 Units)



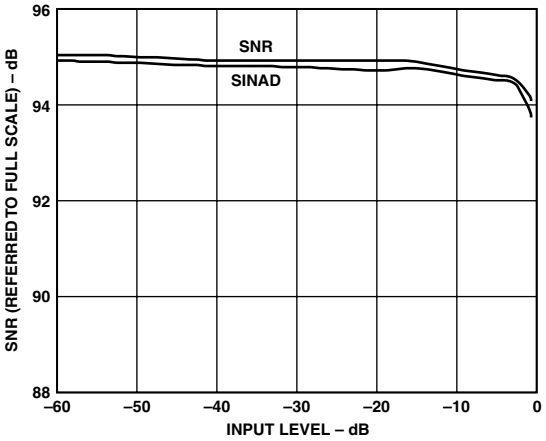
TPC 6. FFT Plot



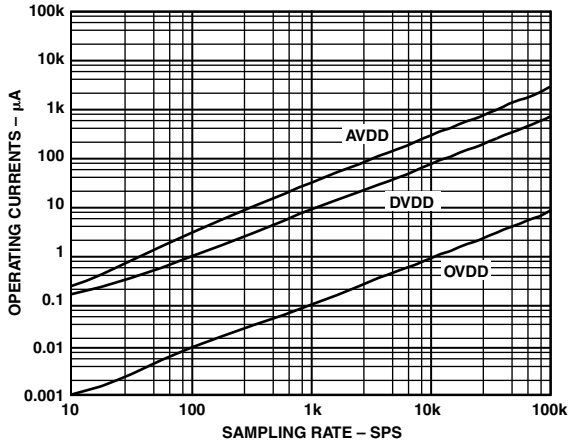
TPC 7. SNR, S/(N+D), and ENOB vs. Frequency



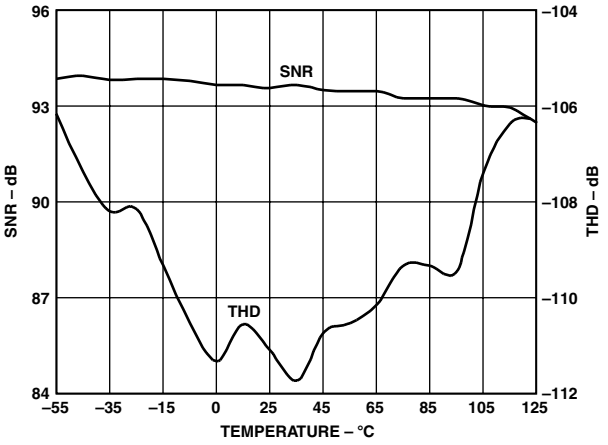
TPC 10. Typical Delay vs. Load Capacitance C_L



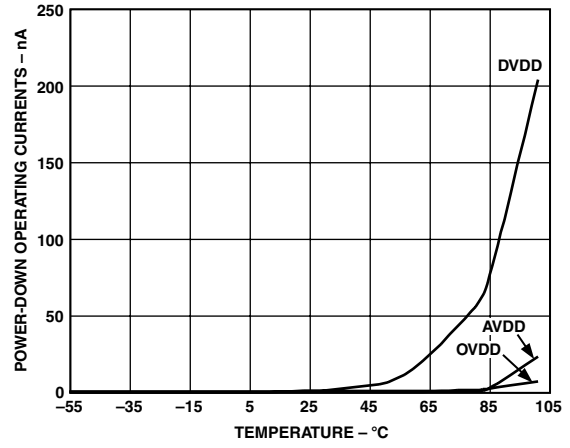
TPC 8. SNR and S/(N+D) vs. Input Level



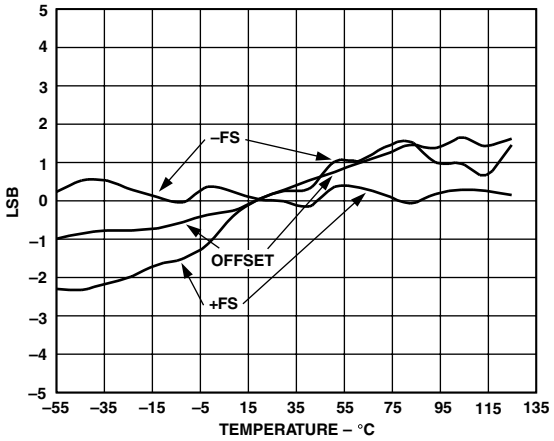
TPC 11. Operating Currents vs. Sample Rate



TPC 9. SNR, THD vs. Temperature



TPC 12. Power-Down Operating Currents vs. Temperature



TPC 13. Drift vs. Temperature

CIRCUIT INFORMATION

The AD7675 is a fast, low power, single-supply, precise 16-bit analog-to-digital converter (ADC). The AD7675 is capable of converting 100,000 samples per second (100 kSPS) and allows power saving between conversions. When operating at 100 SPS, for example, it consumes typically only 15 µW. This feature makes the AD7675 ideal for battery-powered applications.

The AD7675 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7675 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP package that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7675 is pin-to-pin compatible with the AD7660.

CONVERTER OPERATION

The AD7675 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW_+ and SW_-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire both analog signals.

When the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes or is low, a conversion phase is initiated. When the conversion phase begins, SW_+ and SW_- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the output of IN+ and IN– captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced.

By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

Transfer Functions

Using the OB/$\overline{\text{2C}}$ digital input, the AD7675 offers two output codings: straight binary and two's complement. The ideal transfer characteristic for the AD7675 is shown in Figure 4.

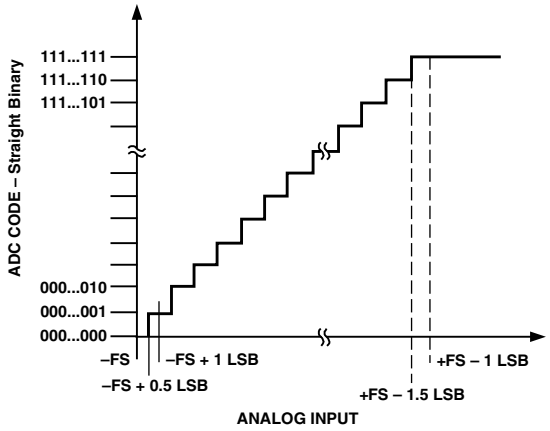


Figure 4. ADC Ideal Transfer Function

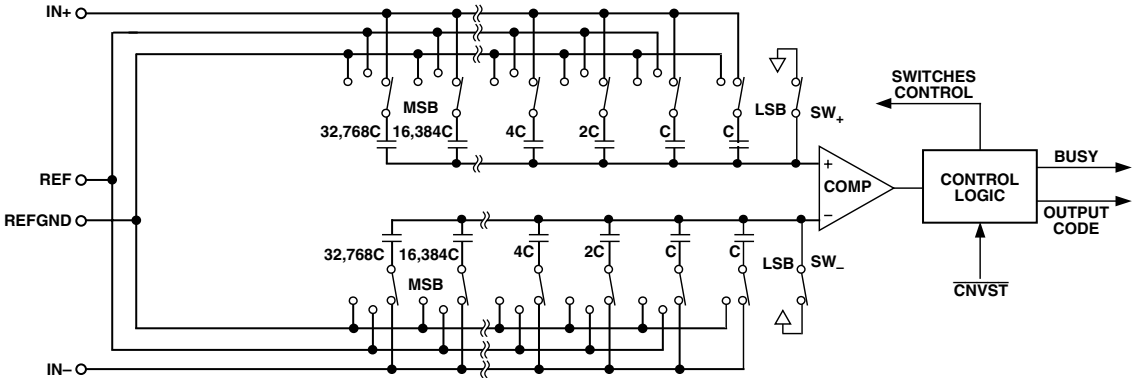
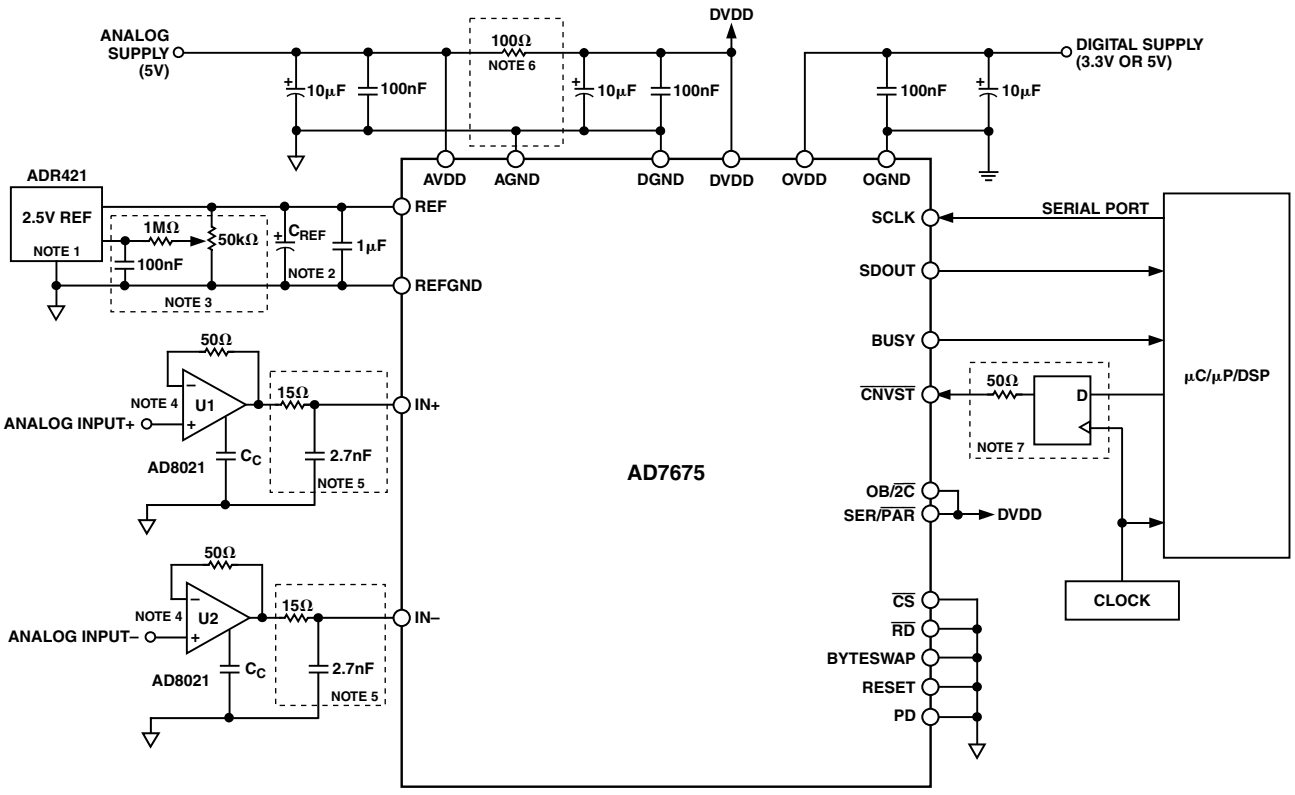


Figure 3. ADC Simplified Schematic



NOTES
1. SEE VOLTAGE REFERENCE INPUT SECTION.
2. WITH THE RECOMMENDED VOLTAGE REFERENCES, C_{REF} IS 47µF. SEE CHAPTER VOLTAGE REFERENCE INPUT SECTION
3. OPTIONAL CIRCUITRY FOR HARDWARE GAIN CALIBRATION.
4. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
5. SEE ANALOG INPUT SECTION.
6. OPTION, SEE POWER SUPPLY SECTION
7. OPTIONAL LOW JITTER $\overline{CNVST}$, SEE CONVERSION CONTROL SECTION.

Figure 5. Typical Connection Diagram. (±2.5 V Range Shown)

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7675. Different circuitry shown on this diagram is optional and is discussed below.

Analog Inputs

Figure 6 shows a simplified analog input section of the AD7675.

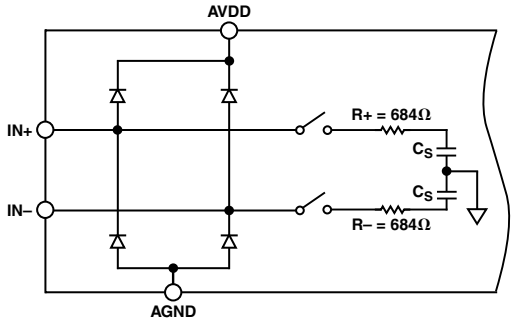


Figure 6. Simplified Analog Input

The diodes shown in Figure 6 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. This condition could eventually occur when the input buffer's (U1) or (U2) supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure is a true differential structure. By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 7, which represents the typical CMRR over frequency.

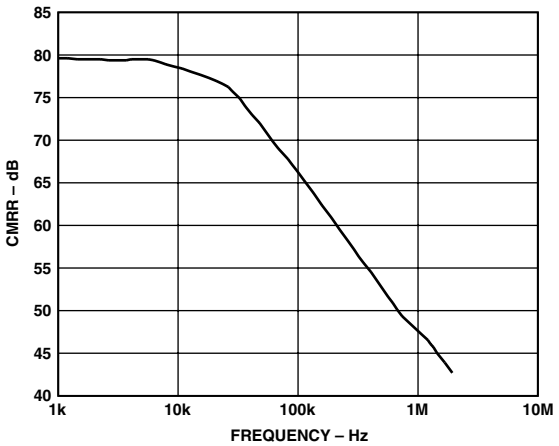


Figure 7. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the AD7675 behaves like a one-pole RC filter consisting of the equivalent resistance R+, R–, and C_S. The resistors R+ and R– are typically 684 Ω and are lumped components made up of some serial resistors and the on resistance of the switches. The capacitor C_S is typically 60 pF and is mainly the ADC sampling capacitor. This one pole filter with a typical –3 dB cutoff frequency of 3.9 MHz reduces undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7675 is very high, the AD7675 can be driven directly by a low impedance source without gain error. That allows users to put, as shown in Figure 5, an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7675 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades proportionally to the source impedance.

Single to Differential Driver

For applications using unipolar analog signals, a single-ended to differential driver will allow for a differential input into the part. The schematic is shown in Figure 8.

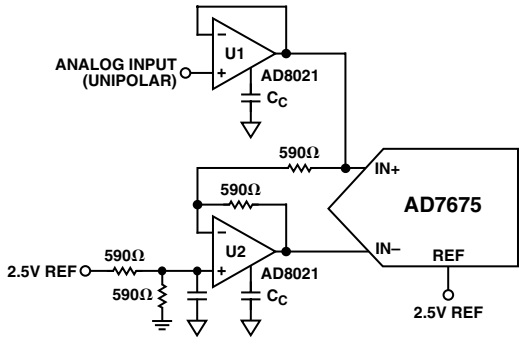


Figure 8. Single-Ended-to-Differential Driver Circuit

This configuration, when provided an input signal of 0 to V_{REF}, will produce a differential ±2.5 V with a common mode at 1.25 V.

If the application can tolerate more noise, the AD8138 can be used.

Driver Amplifier Choice

Although the AD7675 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7675 analog input circuit have to be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at 16-bit level and, therefore, it should be verified prior to the driver selection. The tiny op amp AD8021, which combines ultra low noise and a high gain bandwidth, meets this settling time requirement even when used with a high gain up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7675. The noise coming from the driver is filtered by the AD7675 analog input circuit one-pole, low-pass filter made by R+, R–, and C_S. The SNR degradation due to the amplifier is:

$$SNR_{LOSS} = 20LOG\left(\frac{28}{\sqrt{784 + \frac{\pi}{4} f_{-3\,dB}\,(N\,e_N)^2}}\right)$$

where

$f_{-3\,dB}$ is the –3 dB input bandwidth of the AD7675 (3.9 MHz) or the cutoff frequency of the input filter if any is used.

N is the noise factor of the amplifier (1 if in buffer configuration)

e_N is the equivalent input noise voltage of the op amp in nV/(Hz)$^{1/2}$.

For instance, in the case of a driver with an equivalent input noise of 2 nV/$\sqrt{\text{Hz}}$ like the AD8021 and configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.04 dB with the filter in Figure 5, and 0.07 dB without.

- The driver needs to have a THD performance suitable to that of the AD7675.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where dual version is needed and gain of 1 is used.

The AD8132 or the AD8138 could also be used to generate a differential signal from a single-ended signal. When using the AD8138 with the filter in Figure 5, the SNR degrades by only 0.9 dB.

The AD829 is another alternative where high frequency (above 100 kHz) performances are not required. In gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is also another option where low bias current is needed in low frequency applications.

The AD8519, OP162, or the OP184 could also be used.

Voltage Reference Input

The AD7675 uses an external 2.5 V voltage reference.

The voltage reference input REF of the AD7675 has a dynamic input impedance. Therefore, it should be driven by a low impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a 1 µF ceramic capacitor and a low ESR tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance. 47 µF is an appropriate value for the tantalum capacitor when used with one of the recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780 voltage references
- The low power ADR291 voltage reference
- The low cost AD1582 voltage reference

For applications using multiple AD7675s, it is more effective to buffer the reference voltage with a low noise, very stable op amp like the AD8031.

Care should also be taken with the reference temperature coefficient of the voltage reference which directly affects the full-scale accuracy if this parameter matters. For instance, a ±15 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

V_{REF}, as mentioned in the specification table, could be increased to AVDD – 1.85 V. The benefit here is the increased SNR obtained as a result of this increase. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to make it a ±3 V input range with an AVDD above 4.85 V. The theoretical improvement as a result of this increase in reference is 1.58 dB (20 log [3/2.5]). Due to the theoretical quantization noise, however, the observed improvement is approximately 1 dB. The AD780 can be selected with a 3 V reference voltage.

Power Supply

The AD7675 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7675 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V, and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 9.

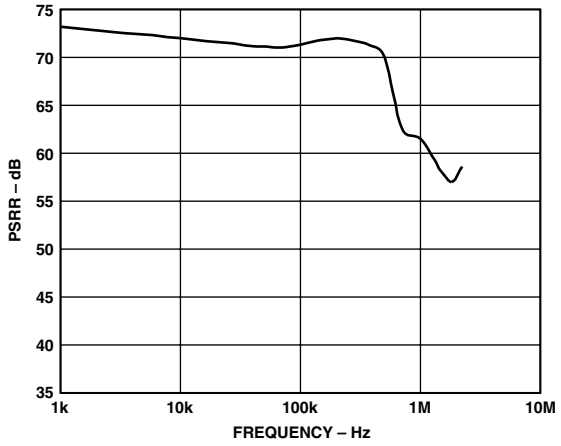


Figure 9. PSRR vs. Frequency

POWER DISSIPATION

The AD7675 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power saving when the conversion rate is reduced as shown in Figure 10. This feature makes the AD7675 ideal for very low power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3 V.

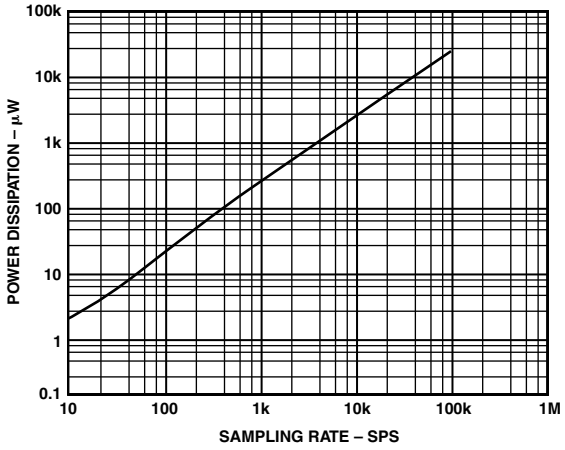


Figure 10. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 11 shows the detailed timing diagrams of the conversion process. The AD7675 is controlled by the signal $\overline{CNVST}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{CNVST}$ signal operates independently of $\overline{CS}$ and $\overline{RD}$ signals.

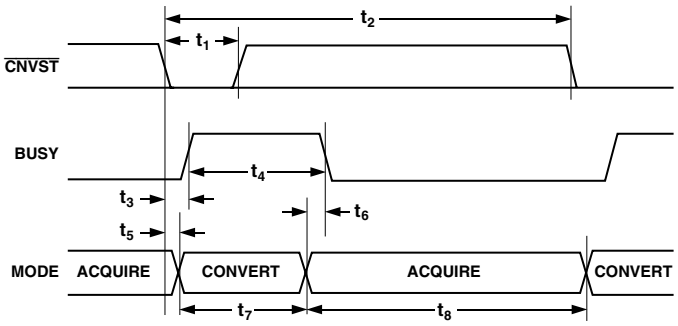


Figure 11. Basic Conversion Timing

For true sampling applications, the recommended operation of the $\overline{CNVST}$ signal is as follows:

$\overline{CNVST}$ must be held high from the previous falling edge of BUSY, and during a minimum delay corresponding to the acquisition time t_8; then, when $\overline{CNVST}$ is brought low, a conversion is initiated and BUSY signal goes high until the completion of the conversion. Although $\overline{CNVST}$ is a digital signal, it should be designed with this special care with fast, clean edges and levels, with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{CNVST}$ signal should have a very low jitter. Some solutions to achieve that are to use a dedicated oscillator for $\overline{CNVST}$ generation or, at least, to clock it with a high frequency low jitter clock, as shown in Figure 5.

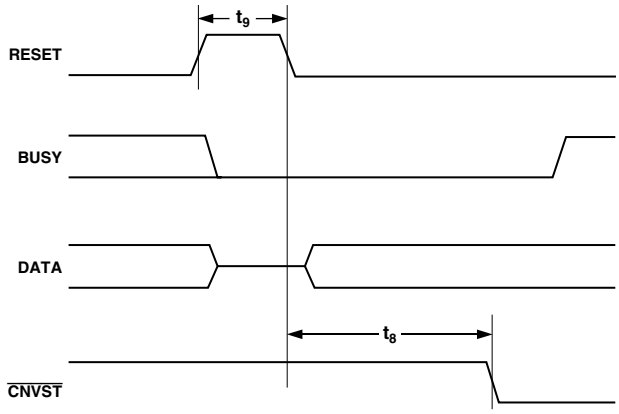


Figure 12. RESET Timing

For other applications, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held low when BUSY is low, the AD7675 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ low, the AD7675 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought low once to initiate the conversion process. In this mode, the AD7675 could sometimes run slightly faster than the guaranteed limit of 100 kSPS.

DIGITAL INTERFACE

The AD7675 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7675 digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7675 to the host system interface digital supply. Finally, by using the OB/$\overline{\text{2C}}$ input pin, either two's complement or straight binary coding can be used.

The two signals $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7675 in multicircuits applications and is held low in a single AD7675 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the data bus.

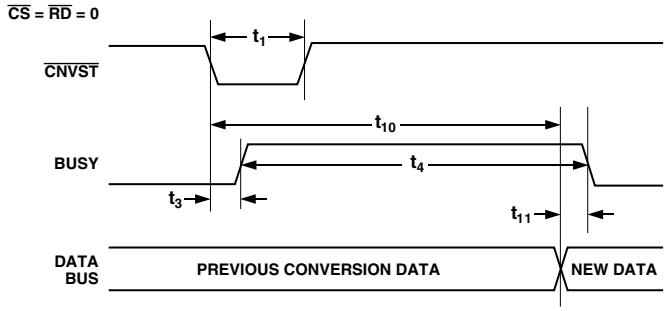


Figure 13. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7675 is configured to use the parallel interface (Figure 13) when the SER/$\overline{\text{PAR}}$ is held low. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 14 and Figure 15. When the data is read during the conversion, however, it is recommended that it be read-only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

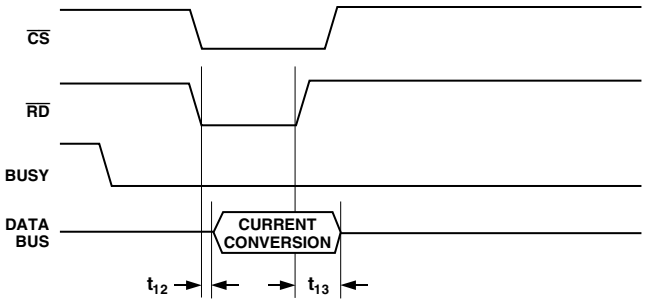


Figure 14. Slave Parallel Data Timing for Reading (Read after Convert)

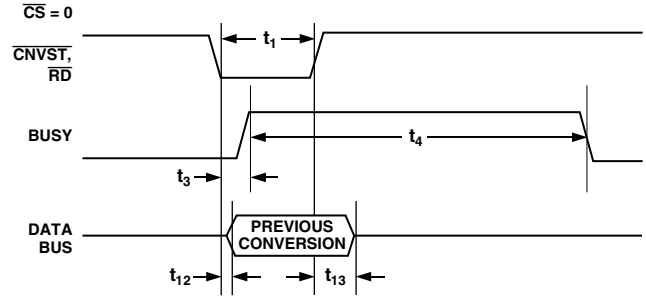


Figure 15. Slave Parallel Data Timing for Reading (Read During Convert)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 16, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0].

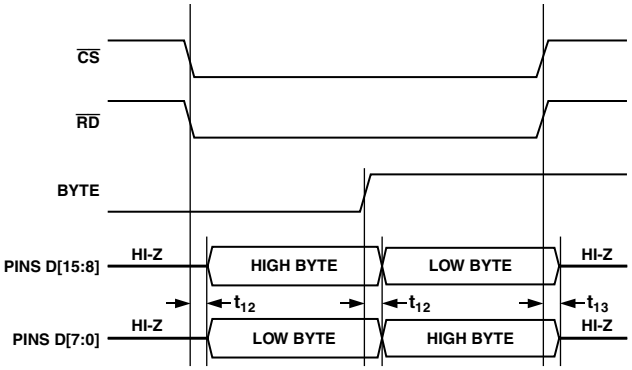


Figure 16. 8-Bit Parallel Interface

SERIAL INTERFACE

The AD7675 is configured to use the serial interface when the SER/$\overline{PAR}$ is held high. The AD7675 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin.

MASTER SERIAL INTERFACE

Internal Clock

The AD7675 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{INT}$ pin is held low. The AD7675 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. The output data is valid on both the rising and falling edge of the data clock. Depending on RDC/SDIN input, the data can be read after each conversion, or during the following conversion. Figure 17 and Figure 18 show the detailed timing diagrams of these two modes.

Usually, because the AD7675 has a longer acquisition phase than the conversion phase, the data is read immediately after conversion. That makes the mode master, read after conversion, the most recommended serial mode when it can be used.

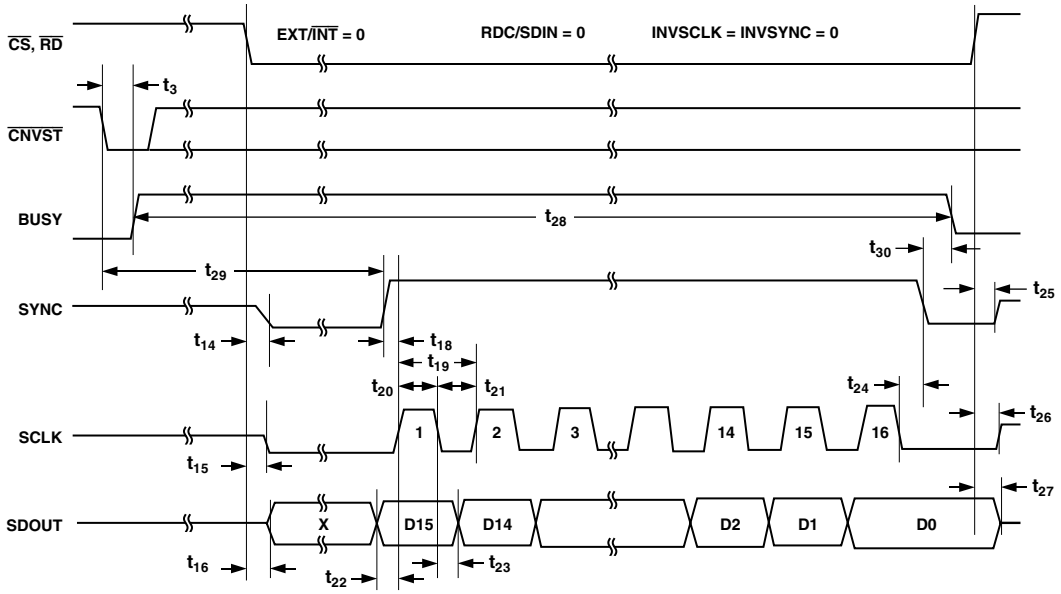


Figure 17. Master Serial Data Timing for Reading (Read after Convert)

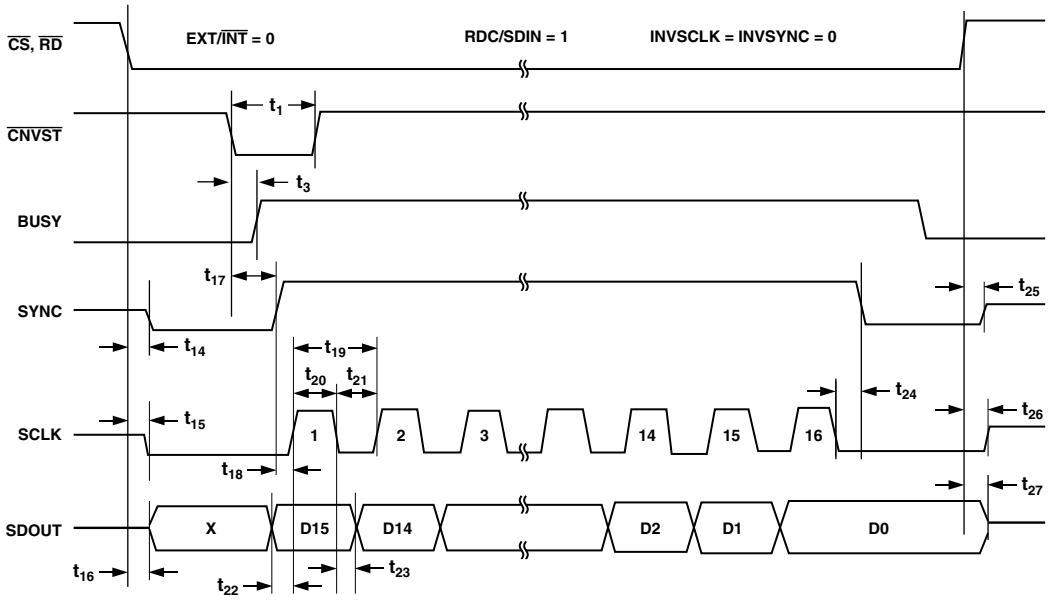


Figure 18. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

In read-after-conversion mode, unlike in other modes, it should be noted that the signal BUSY returns low after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

In read-during-conversion mode, the serial clock and data toggle at appropriate instances, which minimizes potential feedthrough between digital activity and the critical conversion decisions.

To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

SLAVE SERIAL INTERFACE

External Clock

The AD7675 is configured to accept an externally supplied serial data clock on the SCLK Pin when the EXT/$\overline{\text{INT}}$ Pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$ and the data are output when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Thus, depending on $\overline{\text{CS}}$, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 19 and Figure 20 show the detailed timing diagrams of these methods. Usually, because the AD7675 has a longer acquisition phase than the conversion phase, the data are read immediately after conversion.

While the AD7675 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7675 provides error-correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read after Conversion

This mode is the most recommended of the serial slave modes. Figure 19 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock.

One of the advantages of this method is that the conversion performance is not degraded because there are no voltage transient on the digital interface during the conversion process.

Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7675 provides a "daisy chain" feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when it is desired as it is, for instance, in isolated multiconverters applications.

An example of the concatenation of two devices is shown in Figure 21. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Hence, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

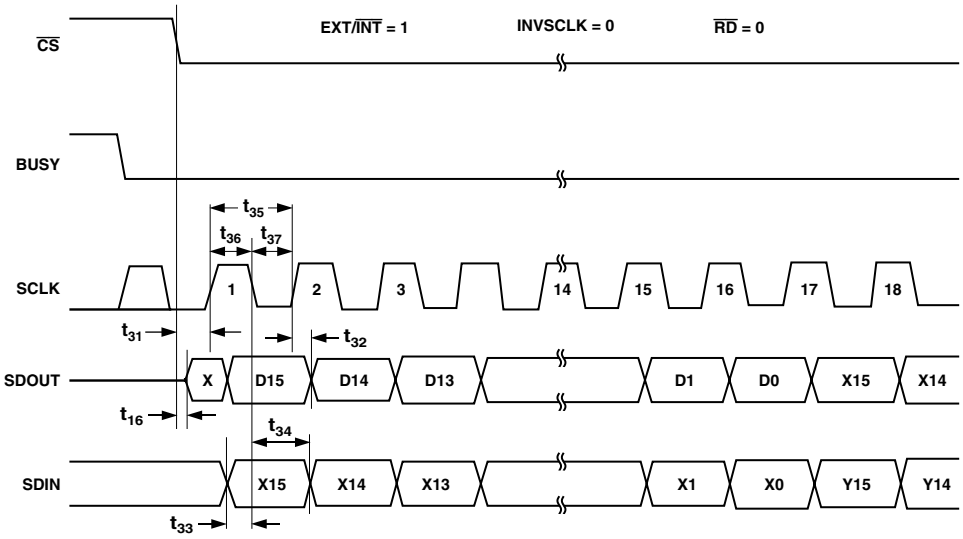


Figure 19. Slave Serial Data Timing for Reading (Read after Convert)

External Clock Data Read During Conversion

Figure 20 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses, and is valid on both rising and falling edges of the clock. The 16 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode, and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of 18 MHz at least is recommended to ensure that all the bits are read during the first half of the conversion phase. For this reason, this mode is more difficult to use.

MICROPROCESSOR INTERFACING

The AD7675 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7675 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7675 to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the AD7675 with an SPI-equipped microcontroller, and the ADSP-21065L and ADSP-218x signal processors.

SPI Interface (MC68HC11)

Figure 22 shows an interface diagram between the AD7675 and an SPI-equipped microcontroller like the MC68HC11. To accommodate the slower speed of the microcontroller, the AD7675 acts as a slave device and data must be read after conversion. This mode also allows the "daisy chain" feature. The convert command could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time if necessary, could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the microcontroller. The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI interrupt enable (SPIE) = 1 by writing to the SPI Control Register (SPCR). The IRQ is configured for edge-sensitive-only operation (IRQE = 1 in OPTION register).

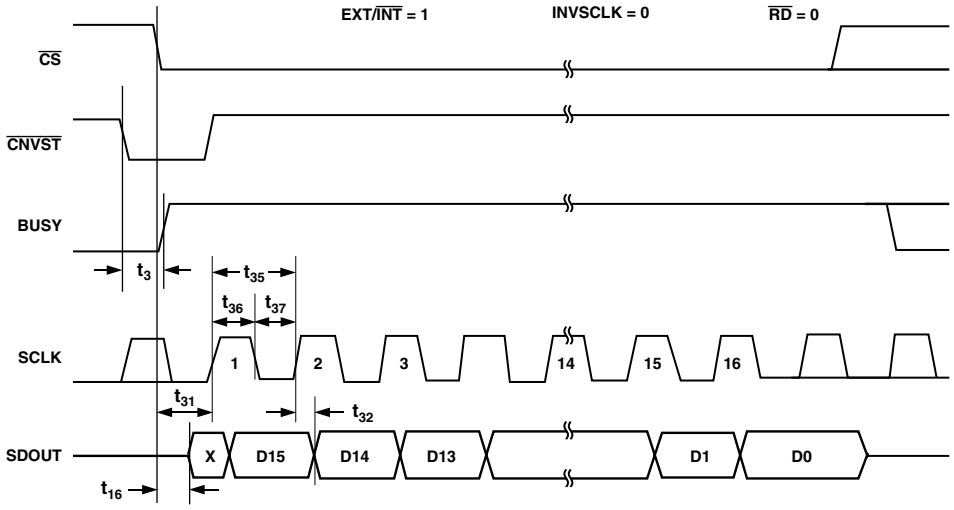


Figure 20. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

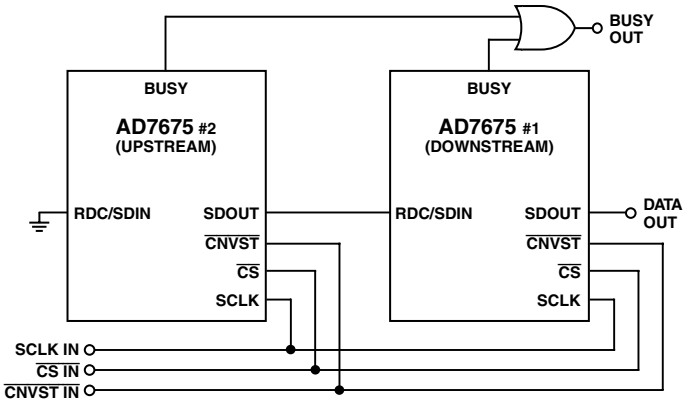


Figure 21. Two AD7675s in a "Daisy Chain" Configuration

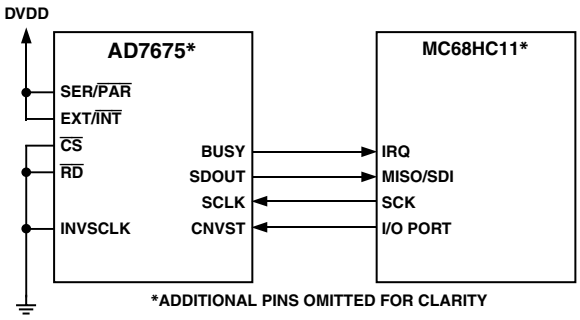


Figure 22. Interfacing the AD7675 to SPI Interface

ADSP-21065L in Master Serial Interface

As shown in Figure 23, the AD7675 can be interfaced to the ADSP-21065L using the serial interface in master mode without any glue logic required. This mode combines the advantages of reducing the wire connections and the ability to read the data during or after conversion maximum speed transfer (DIVSCLK[0:1] both low).

The AD7675 is configured for the internal clock mode (EXT/$\overline{\text{INT}}$ low) and acts, therefore, as the master device. The convert command can be generated by either an external low jitter oscillator or, as shown, by a FLAG output of the ADSP-21065L or by a frame output TFS of one serial port of the ADSP-21065L that can be used like a timer. The serial port on the ADSP-21065L is configured for external clock (IRFS = 0), rising edge active (CKRE = 1), external late framed sync signals (IRFS = 0, LAFS = 1, RFSR = 1) and active high (LRFS = 0). The serial port of the ADSP-21065L is configured by writing to its receive control register (SRCTL)—see ADSP-2106x SHARC User's Manual. Because the serial port within the ADSP-21065L will be seeing a discontinuous clock, an initial word reading has to be done after the ADSP-21065L has been reset to ensure that the serial port is properly synchronized to this clock during each following data read operation.

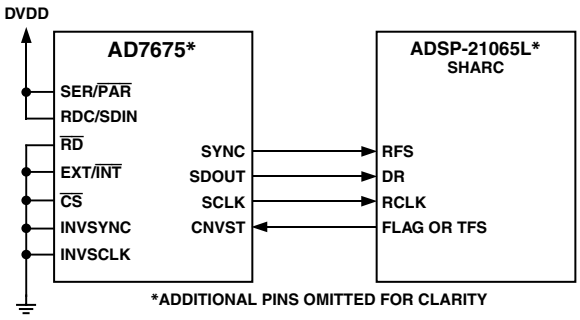


Figure 23. Interfacing to the ADSP-21065L Using the Serial Master Mode

APPLICATION HINTS

Layout

The AD7675 has very good immunity to noise on the power supplies as can be seen in Figure 21. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7675 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7675, or, at least, as close as possible to the AD7675. If the AD7675 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7675.

It is recommended that running digital lines under the device should be avoided as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7675 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supply lines to the AD7675 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply's impedance presented to the AD7675 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply's pins, AVDD, DVDD, and OVDD, close to and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low-frequency ripple.

The DVDD supply of the AD7675 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply is available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 5, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7675 has four different ground pins: REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

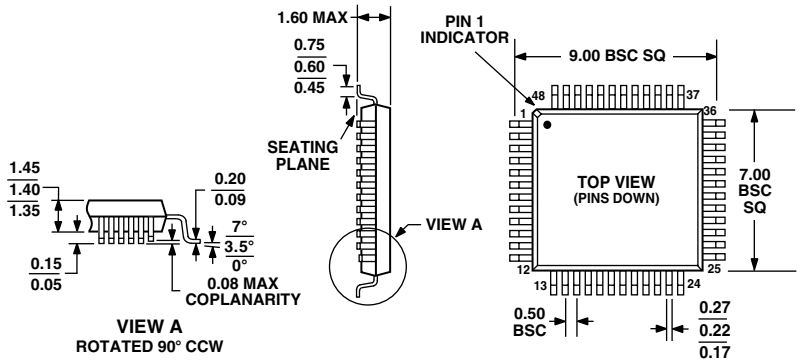
Evaluating the AD7675 Performance

A recommended layout for the AD7675 is outlined in the evaluation board for the AD7675. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD2.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

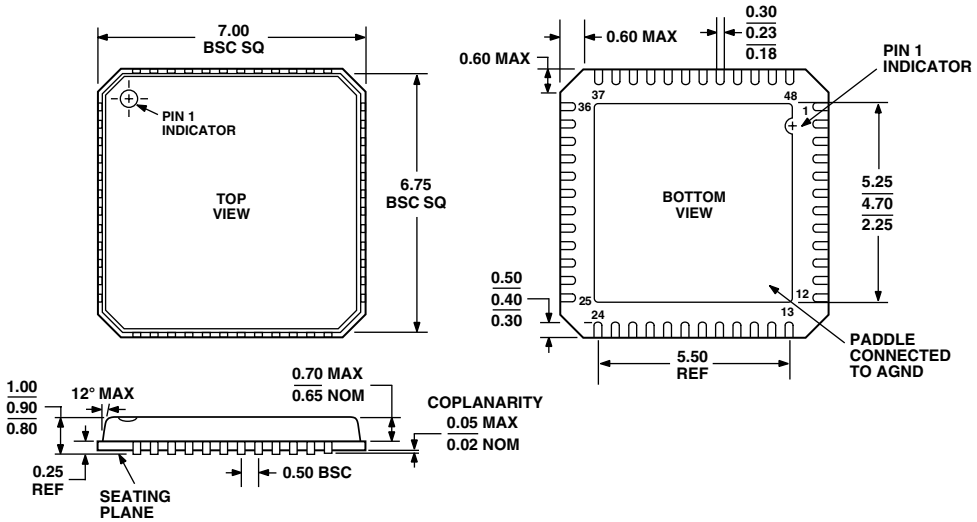
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

48-Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body
(CP-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Revision History

Location	Page
7/02—Data Sheet changed from REV. 0 to REV. A.	
Added 48-Lead LFCSP to FEATURES and GENERAL DESCRIPTION	1
Added PulSAR Selection table	1
Edits to NOTES	2
Changes to ABSOLUTE MAXIMUM RATINGS	4
Additions to ORDERING GUIDE	4
Edits to PIN FUNCTION DESCRIPTIONS	5
Changes to Power Supply section	13
Added 48-Lead Frame Chip Scale Package (LFCSP)	19

C02689–0–7/02(A)

PRINTED IN U.S.A.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD7675ASTZRL AD7675ASTZ