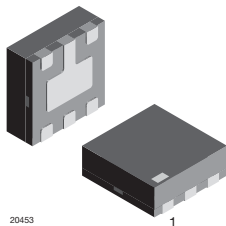
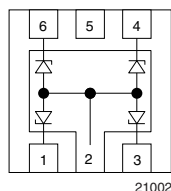


4-Line (Quad) ESD Protection Diode Array in LLP75-6L



MARKING (example only)



Dot = pin 1 marking

XX = date code

YY = type code (see table below)

DESIGN SUPPORT TOOLS

[click logo to get started](#)



FEATURES

- Compact LLP75-6L package
- Low package height < 0.6 mm
- 4-line ESD protection (quad)
- Low leakage current < 0.1 μ A
- Low load capacitance $C_D = 6$ pF
- ESD immunity acc. IEC 61000-4-2
± 8 kV contact discharge
± 10 kV air discharge
- Surge current acc. IEC 61000-4-5 $I_{PP} > 1.5$ A
- Soldering can be checked by standard vision inspection. No X-ray necessary
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD09A4A-HSF	VESD09A4A-HSF-GS08	3000	15 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD09A4A-HSF	LLP75-6L	49	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VESD09A4A-HSF

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	BiAs-mode: each input (pin 1, 3 - 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	I_{PPM}	1.5	A
Peak pulse power	BiAs-mode: each input (pin 1, 3 - 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	P_{PP}	30	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 8	kV
	BiAs-mode: each input (pin 1, 3 - 5) to ground (pin 2 and 6)	V_{ESD}	± 8	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 10	kV
Operating temperature	Junction temperature	T_J	-40 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

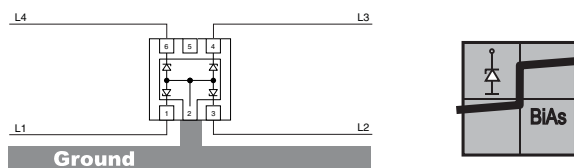
BiAs-MODE (4-line bidirectional asymmetrical protection mode)

With the VESD09A4A-HSF up to 4 signal- or data-lines (L1 to L4) can be protected against voltage transients. With pin 2 connected to ground and pin 1, 3, 4 and 6 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage (V_{RWM}) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage (V_C) is defined by the breakthrough voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD09A4A-HSF clamping behaviour is bidirectional and asymmetrical (BiAs).



21003

ELECTRICAL CHARACTERISTICS VESD09A4A-HSF (Pin 1, 3, 4, or 5 to pin 2)

($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

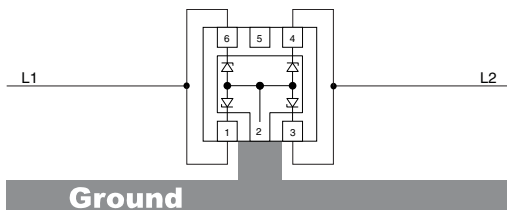
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	9	V
Reverse voltage	at $I_R = 0.1\text{ }\mu\text{A}$	V_R	9	-	-	V
Reverse current	at $V_R = V_{RWM} = 9\text{ V}$	I_R	-	< 0.01	0.1	μA
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	V_{BR}	11.2		13	V
Reverse clamping voltage	at $I_{PP} = 1.5\text{ A}$, acc. IEC 61000-4-5	V_C	-		23	V
Forward clamping voltage	at $I_F = 1.5\text{ A}$, acc. IEC 61000-4-5	V_F	-		2	V
Capacitance	at $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	6.2	10	pF
	at $V_R = 4.5\text{ V}$; $f = 1\text{ MHz}$	C_D	-	3.2	4	pF

Note

- BiAs mode (between pin 1 and pin 2).

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the VESD09A4A-HSF can also be used in parallel in order to "multiply" the performance. If two diodes are switched in parallel you get

- double surge power = double peak pulse current ($2 \times I_{PPM}$)
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line capacitance ($2 \times C_D$)
- double reverse leakage current ($2 \times I_R$)



21004

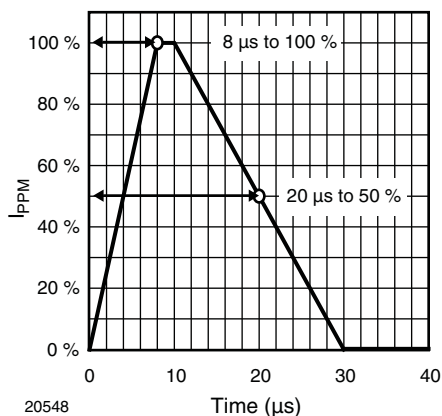
TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

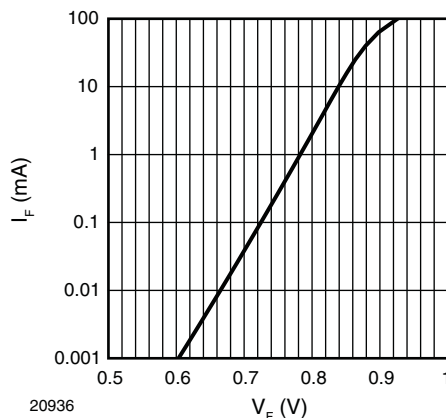


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

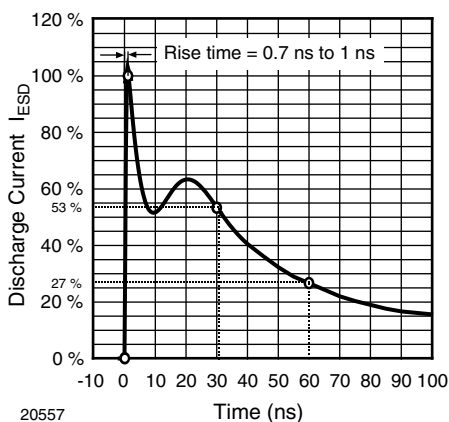


Fig. 2 - 8/20 μ s Peak Pulse Current Wave Form
acc. IEC 61000-4-5

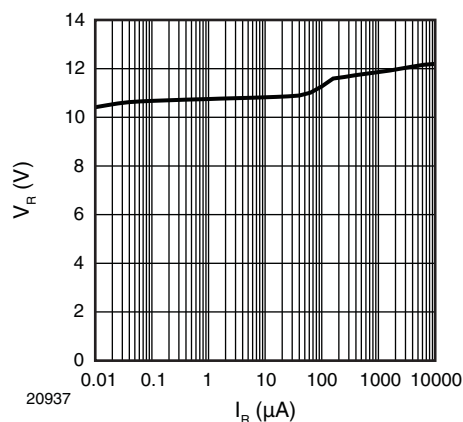


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

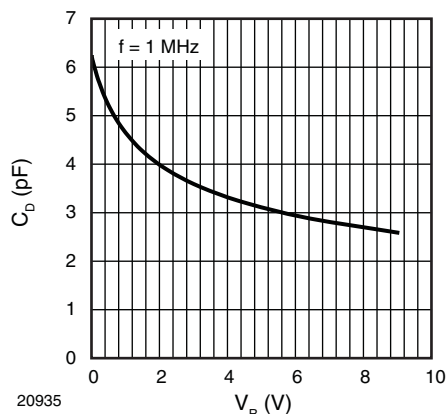


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

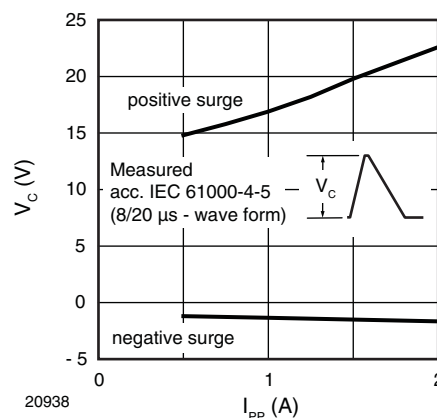


Fig. 6 - Typical Peak Clamping Voltage V_C vs.
Peak Pulse Current I_{PP}

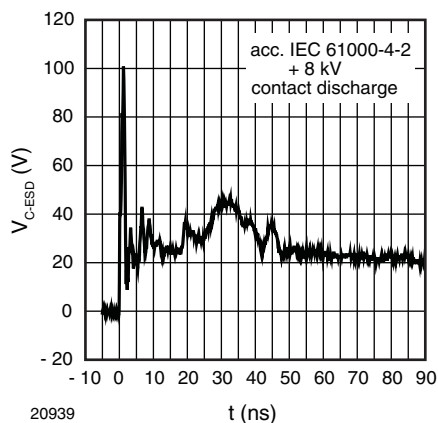


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

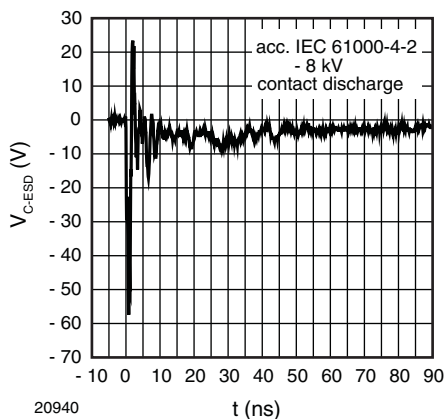


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

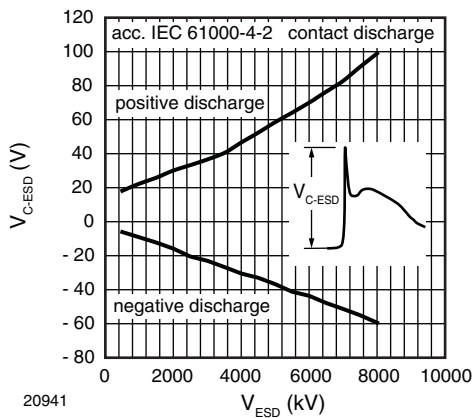
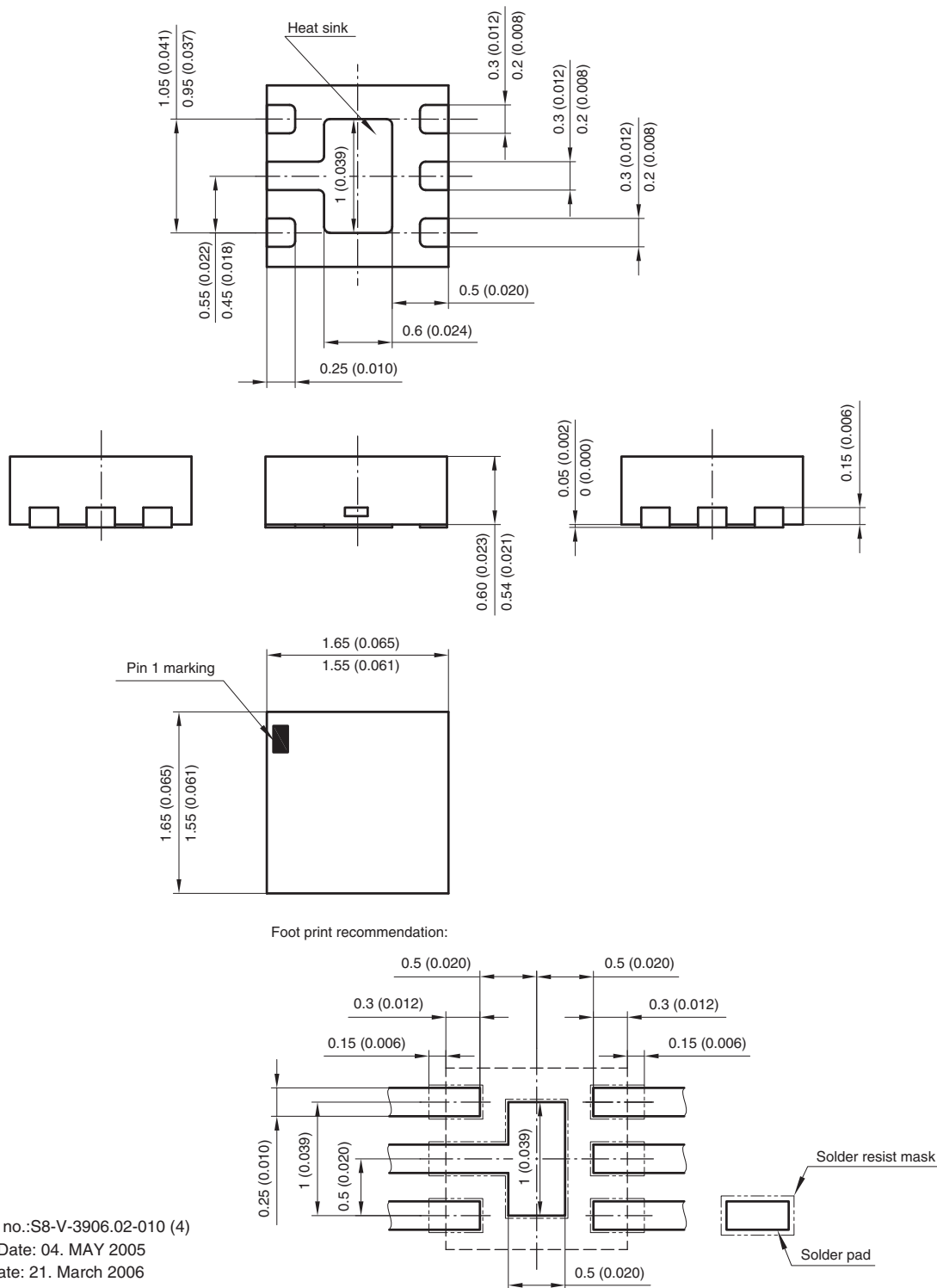
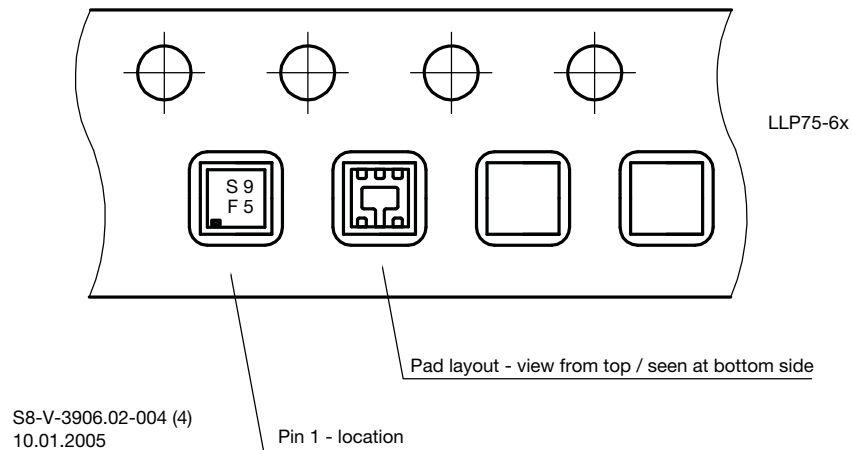


Fig. 9 - Typical Peak Clamping Voltage at ± ESD Contact Discharge (acc. IEC 61000-4-2)

PACKAGE DIMENSIONS in millimeters (Inches): **LLP75-6L**

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Rev. 4 - Date: 21. March 2006
20454





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