DeviceNet™ CAN Transceivers

Check for Samples: SN65HVD252, SN65HVD253

FEATURES

- **DeviceNet Compliant Supporting 64 DeviceNet Nodes**
- **Loopback Function (HVD253)**
- **Bus-Fault Protection of –36 V to 40 V**
- **Power-Up/Down Glitch-Free Bus I/O**
- **3.3-V Compatible Receiver Output**

APPLICATIONS

- **DeviceNet Networks (Vendor ID # 806)**
- **Industrial Automation**
- **HVAC Networks**
- **Security Systems**
- **Telecom Base Station Status and Control**
- **CANopen Data Bus**
- **SDS Data Bus**
- **CAN Kingdom Data Bus**

DESCRIPTION

The SN65HVD252 and SN65HVD253 CAN transceivers meet or exceed the specifications of DeviceNet and are compatible to the ISO 11898-2:2003 standard for use in applications employing a controller area network (CAN). This device provides differential transmit and receive capability at signaling rates up to 1 megabit per second (Mbps).

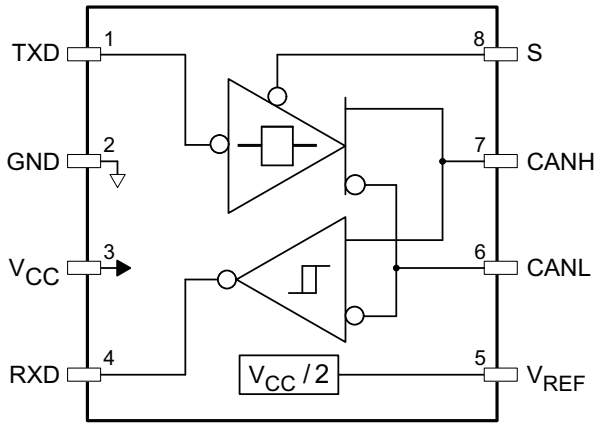
Designed for operation in harsh industrial environments, these devices feature bus-pin voltage protection from –36 V to 40 V, driver output current limiting, and overtemperature driver shutdown.

Pin 8 provides for two different modes of operation: normal and silent mode. The normal mode of operation is selected by connecting S (pin 8) to ground. If a high logic level is applied to the S pin, the device enters a listen-only silent mode during which the driver is inactive while the receiver remains fully functional.

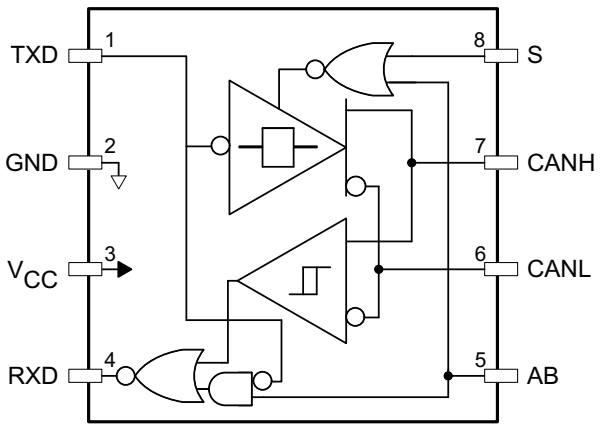
The Vref pin 5 of the SN65HVD252 is a $V_{CC}/2$ voltage reference for systems which use split termination.

The AB pin of the SN65HVD253 implements a listen-only loopback feature which allows the local node controller to synchronize its baud rate with that of the CAN bus. In loopback mode, the driver differential outputs are placed in high-impedance state while the receiver bus inputs remain active. For more information on the loopback mode, see the *Application Information* section.

The SN65HVD252 and SN65HVD253 are characterized for operation from –40°C to 85°C.



SN65HVD252



SN65HVD253

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DeviceNet is a trademark of Open DeviceNet Vendor Association .

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. DRIVER (SN65HVD252)

INPUTS		OUTPUTS		BUS STATE
TXD	S	CAN_H	CAN_L	
L	L or OPEN	H	L	Dominant
H or OPEN		Z	Z	Recessive
X	H	Z	Z	Recessive

Table 2. RECEIVER (SN65HVD252)

INPUTS		OUTPUT
BUS STATE	$V_{ID} = V_{CANH} - V_{CANL}$	RXD
Dominant	$V_{ID} \geq 0.9$ V	L
?	0.5 V < V_{ID} < 0.9 V	?
Recessive	$V_{ID} < 0.5$ V	H
OPEN	$V_{ID} \approx 0$ V	H

Table 3. DRIVER (SN65HVD253)

INPUTS			OUTPUTS		BUS STATE
TXD	AB	S	CAN_H	CAN_L	
X	X	H	Z	Z	Recessive
L	L or open	L or OPEN	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H		Z	Z	Recessive

Table 4. RECEIVER (SN65HVD253)

INPUTS				OUTPUT
AB	BUS STATE	$V_{ID} = V_{CANH} - V_{CANL}$	TXD	RXD
L or open	Dominant	$V_{ID} \geq 0.9$ V	X	L
	?	0.5 V < V_{ID} < 0.9 V		?
	Recessive	$V_{ID} \leq 0.5$ V		H
	Open	$V_{ID} \approx 0$ V		H
H	Dominant	$V_{ID} \geq 0.9$ V	X	L
	?	0.5 V < V_{ID} < 0.9 V	L	L
			H	?
	Recessive	$V_{ID} \leq 0.5$ V or open	H	H
X	X	X	L	L

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
Supply voltage (2), V_{CC}	–0.3 to 6	V
Voltage range at CANH, CANL, V_{REF}	–36 to 40	V
Voltage at CANH, CANL, transient pulse per ISO 7637, pulse 1, 2, 3a, 3b, 5, 6, 7	–200 to 200	V
Voltage input range at logic inputs, V_I (TXD, AB, RXD, S)	–0.5 to 6	V
ESD, human-body model (HBM) per JEDEC Standard 22, test method A114, CANH, CANL vs GND	±12	kV
ESD, human-body model (HBM) per JEDEC Standard 22, test method A114, all pins	±5	kV
ESD, charged-device model (CDM) per JEDEC Standard 22, test method C101, all pins	±2	kV
ESD, machine model (MM) per JEDEC Standard 22, test method A115 CANH, CANL vs GND	±200	V
Receiver output current, I_O	±20	mA
Junction temperature, T_J	170	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
	Voltage at any bus terminal (separately or common mode)		–5(1)	10	V
V_{IH}	High-level input voltage	TXD, S, AB inputs	2	5.5	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{ID}	Differential input voltage		–7	7	V
I_{OH}	Output current	Driver	–70	70	mA
		Receiver	–2	2	
T_A	Operating ambient free-air temperature	See Thermal Information Table	–40	85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

THERMAL INFORMATION

THERMAL METRIC			HVD252/53 8 PINS SOIC	UNITS
θ_{JA}	Junction-to-ambient thermal resistance (1)		124.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (2)		55.9	
θ_{JB}	Junction-to-board thermal resistance (3)		50.2	
ψ_{JT}	Junction-to-top characterization parameter (4)		4.9	
ψ_{JB}	Junction-to-board characterization parameter (5)		46	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (6)		n/a	
P_D	Device power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave	189.1	mW
		V_{CC} = 5.25 V, T_J = 150°C, R_L = 50Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave	274.8	mW

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	See Figure 1, TXD = 0 V, S = 0 V, AB = 0 V (HVD253), R_{CM} = open, C_L = open, R_L = 60 Ω		2.75	3.5	4.5	V
		CANL			0.5	1.5	2.25	
$V_{O(R)}$	Bus output voltage (recessive)		TXD = 3 V, S = 0 V	No Load	2	2.5	3	V
$V_{OD(D)}$	Differential output voltage (dominant)		See Figure 1, TXD = 0 V, S = 0 V, R_{CM} = open, C_L = open, 45 Ω ≤ R_L ≤ 60 Ω		1.5	2.4	3.4	V
			See Figure 1, TXD = 0 V, S = 0 V, R_L = 60 Ω, R_{CM} = 330 Ω, C_L = open, –5 V < V_{CM} < 10 V		1.2	2.6	3.3	
$V_{OD(R)}$	Differential output voltage (recessive)		See Figure 1, TXD = 3 V, S = 0 V, R_{CM} = open, C_L = 100 pF	R_L = 60 Ω	–12		12	mV
				No load	–100		50	
V_{SYM}	Output symmetry (dominant or recessive)		See Figure 1, S = 0 V, AB = 0 V (HVD253), R_{CM} = open, C_L = open, R_L = 60 Ω, V_{SYM} = V_{CC} – V_{CANH} – V_{CANL}		–400	0	400	mV
$I_{OS(ss)}$	Short-circuit steady-state output current		–5 V < V_{CANH} < 10 V, CANL open		–350		2.5	mA
			–5 V < V_{CANL} < 10 V, CANH open		–2.5		350	

(1) All typical values are at 25°C with V_{CC} = 5 V.

DRIVER SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHR}	Propagation delay time, high input to recessive output	See Figure 1, S = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		50	70	ns
t_{pLD}	Propagation delay time, low input to dominant output			40	70	
t_r	Differential output signal rise time, 10% to 90%			15	30	
t_f	Differential output signal fall time, 90% to 10%			17	30	
t_{en}	Enable time from silent mode to dominant	R_L = 60 Ω, C_L = 15 pF, C_{LD} = 100 pF			200	ns

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	–5 V < V_{CM} < 10 V			800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})			140	160		
V_{OH}	High-level output voltage	I_O = –2 mA		2.4	3.3	3.7	V
		I_O = –20 µA		2.7	3.3	3.7	
V_{OL}	Low-level output voltage	I_O = 2 mA			0.1	0.2	V
$I_{BL(off)}$	Bus leakage current, with power off	CANH or CANL, Other bus pin at 0 V	Vcc at 0 V	–600		600	µA
I_{BL}	Bus leakage current, in silent mode or recessive state		TXD or S pin at V_{CC}	–600		600	
C_I	Input capacitance to ground, (CANH or CANL)	V_I = 0.4 sin (4E6πt) + 2.5 V			20		pF
C_{ID}	Differential input capacitance	V_I = 0.4 sin (4E6πt)			7		pF
R_{ID}	Differential input resistance	TXD at 3 V, S at 0 V		30	60	80	kΩ
R_{IN}	Input resistance, (CANH or CANL)			15	30	40	kΩ
$R_{I(M)}$	Input resistance matching $[1 – (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	V_{CANH} = V_{CANL}		–3%	0%	3%	

(1) All typical values are at 25°C with V_{CC} = 5 V.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pRH}	Propagation delay time, recessive input to high output	See Figure 2, C_L = 15 pF, AB = 0 V or V_{CC} (HVD253)		55	80	ns
t_{pDL}	Propagation delay time, dominant input to low output			50	80	
t_r	Output signal rise time, 10% to 90%				20	
t_f	Output signal fall time, 90% to 10%				20	

DRIVER-TO-RECEIVER LOOP-SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output	Recessive to dominant	See Figure 4, S at 0 V, AB at 0 V, R_L = 60 Ω, C_{LD} = 100 pF, C_L = 15 pF	40	90	140	ns
t_{loop2}		Dominant to recessive		40	105	140	
t_{AB1}	Loopback delay, driver input to receiver output (HVD253 only)		See Figure 5, S at 0 V, AB = V_{CC}, R_L = 60 Ω, C_{LD} = 100 pF, C_L = 15 pF		20	40	ns

LOGIC INPUT PIN CHARACTERISTICS (D, S, AND AB INPUTS)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current	0 V < V_{IN} < V_{CC}	–100		100	µA
$I_{OP(off)}$	Power-off leakage current	V_{CC} at 0 V, 0 < V_{IN} < $V_{CC(MAX)}$	–100		100	µA

V_{REF} PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	–100 µA < I_O < 100 µA	0.4 V_{CC}	0.5V_{CC}	0.6V_{CC}	V
		–50 µA < I_O < 50 µA	0.43 V_{CC}	0.5V_{CC}	0.57 V_{CC}	
		–5 µA < I_O < 5 µA	0.45 V_{CC}	0.5V_{CC}	0.55 V_{CC}	

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	HVD252	Silent	S at V_{CC}, TXD at V_{CC}		13	17	mA
		HVD253		S at V_{CC}, AB at 0 V or V_{CC}		13	17	
		All	Dominant	TXD at 0 V, 50-Ω load, S at 0 V		60	80	
			Recessive	TXD at V_{CC}, no load, S at 0 V		13	17	

PARAMETER MEASUREMENT INFORMATION

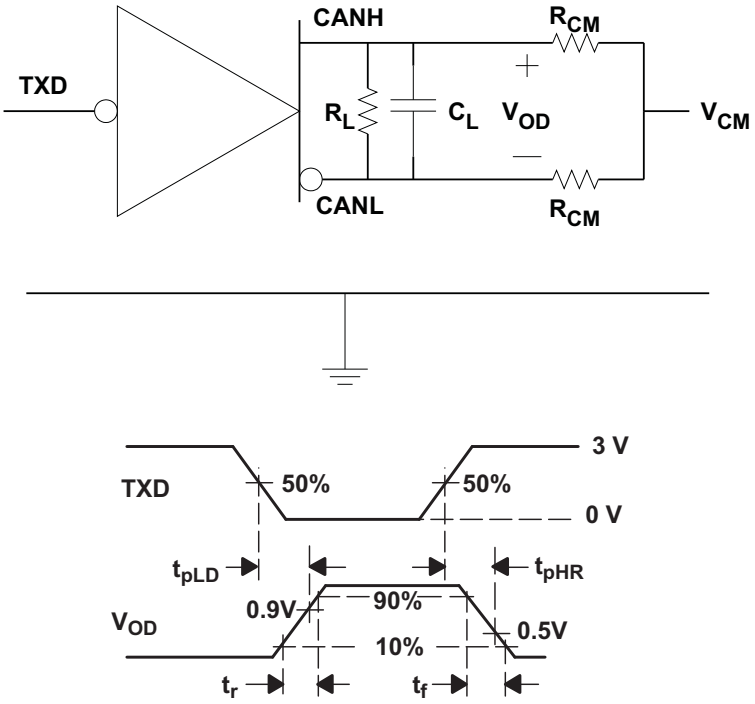


Figure 1. Driver Test Circuit

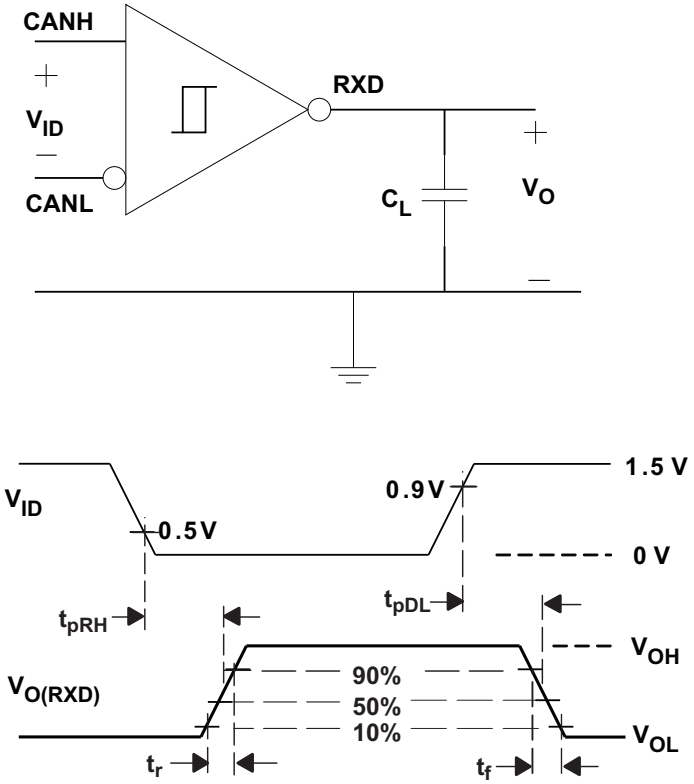


Figure 2. Receiver Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

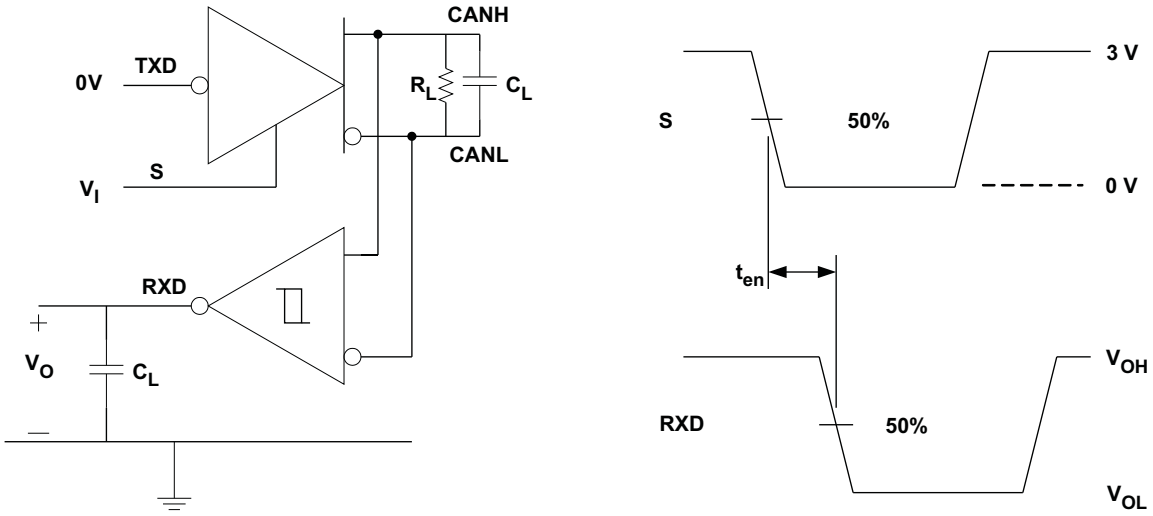


Figure 3. Enable Test Circuit

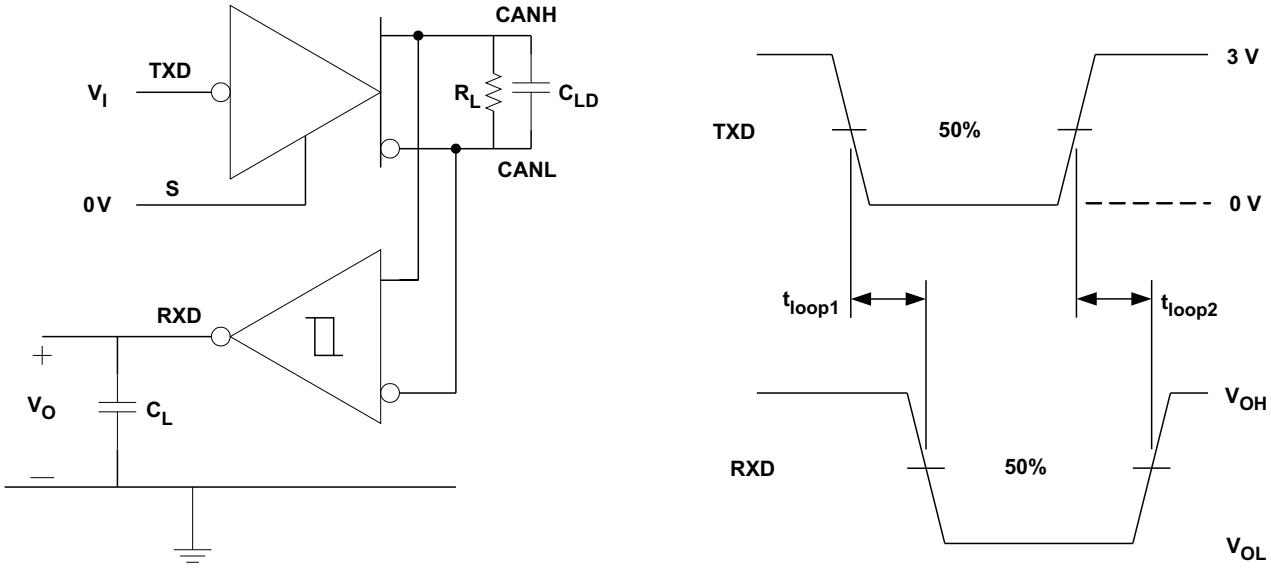


Figure 4. Loop Time Measurements

PARAMETER MEASUREMENT INFORMATION (continued)

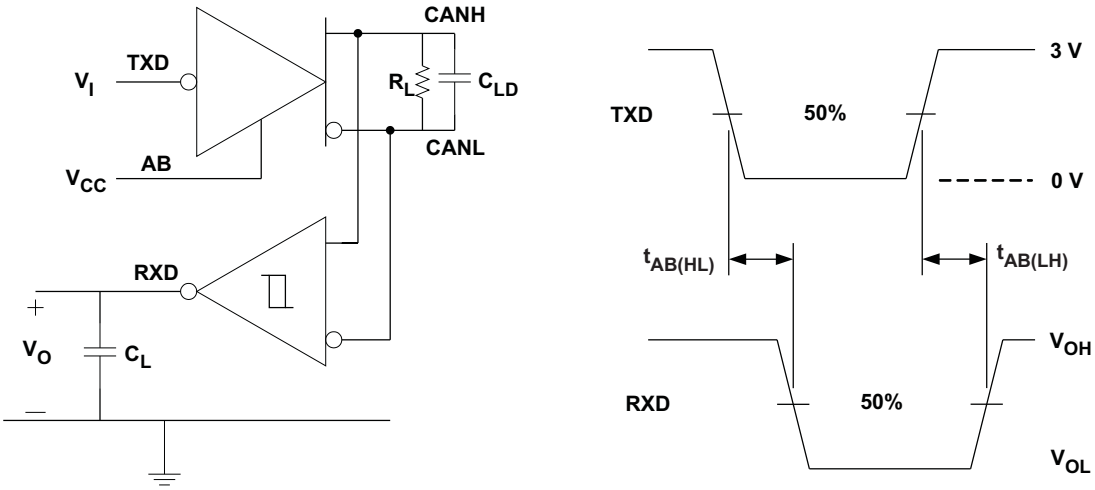
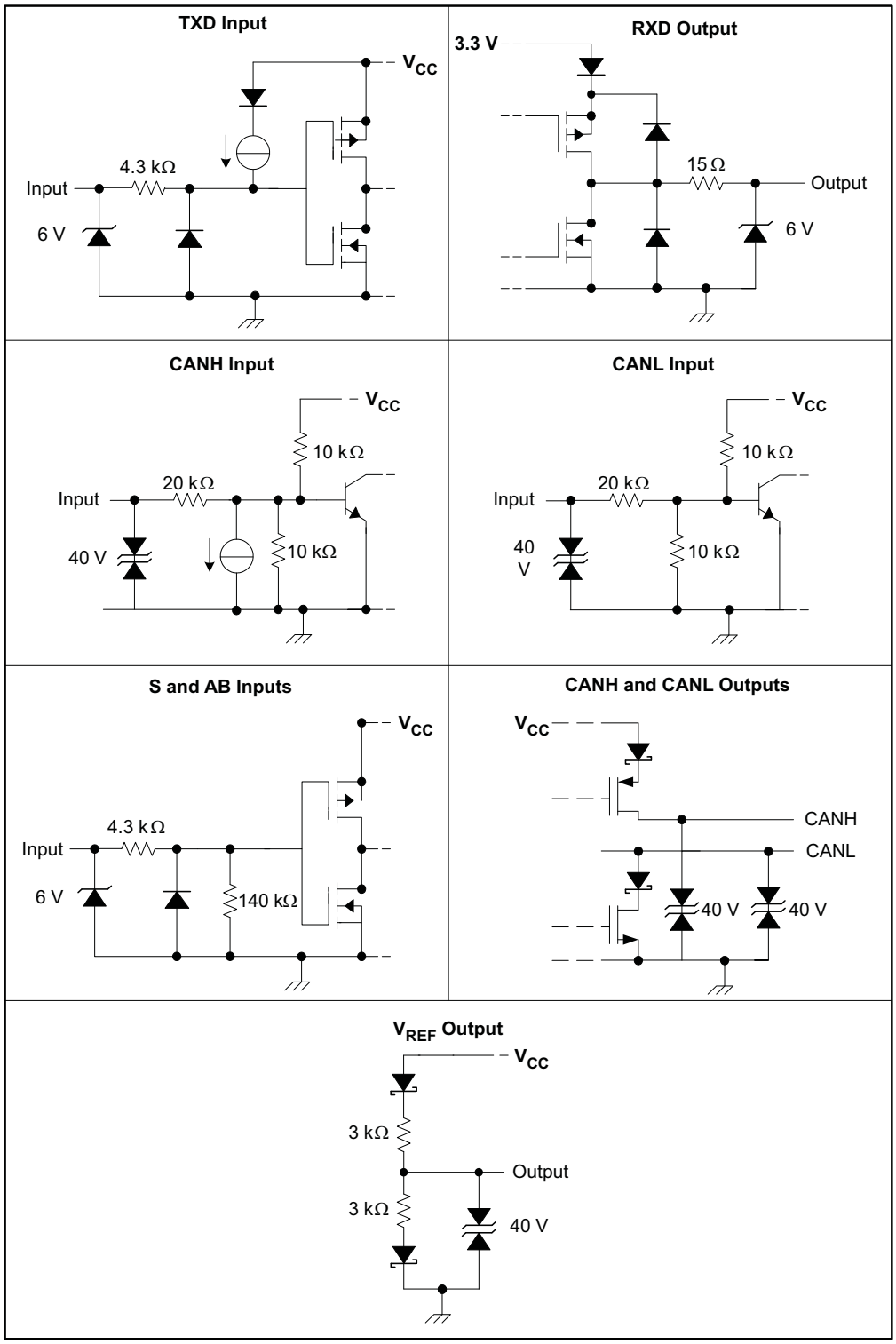


Figure 5. Loopback Timing Measurement

PARAMETER MEASUREMENT INFORMATION (continued)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



APPLICATION INFORMATION

USING THE SILENT MODE

The silent mode is selected by setting a logic high on pin 8 (S). In silent mode, the driver function of the transceiver is disabled, whereas the receiver function remains active. This silent mode may be used to implement *babbling idiot* protection, to ensure that the driver does not disrupt the entire network in case of a local fault. The silent mode may also be used in redundant systems to select or de-select the redundant transceiver until needed.

USING THE AUTOBAUD FEATURE OF THE SN65HVD253

The autobaud feature of the HVD253 is selected by placing a logic high on pin 5 (AB). In autobaud mode, the normal *bus-transmit* function of the transceiver is disabled, whereas the *bus-receive* function and all of the other normal operating functions of the device remain active. An internal loopback emulates the connection between the driver outputs and the receiver inputs, allowing the receiver to respond to locally-generated dominant bits as well as dominant bits from other nodes.

With the autobaud function engaged, normal bus activity, including activity from the local controller, can be monitored by the local node as received data. However, if an error frame is generated by the local CAN controller, it is not transmitted to the bus. Only the local microprocessor can detect the error frame.

Autobaud detection is well suited to applications that have a known selection of baud rates. For example, DeviceNet (a common industrial protocol) has optional signaling rates of 125 kbps, 250 kbps, or 500 kbps. Once a logic high has been applied to pin 5 (AB) of the HVD253, the local controller may assume a baud rate such as 125 kbps and then wait for a message to be transmitted by another node on the bus. If the wrong local signaling rate has been selected, an error message is generated by the local CAN controller. However, because the *bus-transmit* function of the transceiver has been disabled, no other nodes receive the error message from the local controller.

This procedure makes use of the CAN controller status-register indications of message received and error warning status to signal if the current signaling rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message-received status indicates that a good message has been received.

If an error is generated, the local CAN controller may assume another signaling rate and wait to receive another message. When an error-free message has been received, the correct baud rate has been selected. A logic low may now be applied to pin 5 (AB) of the HVD253, returning the *bus-transmit* normal operating function to the transceiver.

USING THE V_{REF} OUTPUT

The V_{REF} output provides a stable voltage of half the power supply voltage. This can be used in split-termination schemes to improve electromagnetic compatibility (EMC) of the system. It can also be used as a reference with which to compare the single-ended inputs for degraded operation in the event of a wire-break fault on either the CANH or CANL bus lines.

DeviceNet REQUIREMENTS

DeviceNet requires additional performance beyond the requirements of the ISO 11898-2 CAN standard. These additional specifications address the conditions found in rugged industrial applications. The DeviceNet specifications are maintained by ODVA. (www.odva.org) The HVD252 and HVD253 fully meet these requirements under all recommended operating conditions.

PARAMETER	DeviceNet SPECIFICATION	HVD252, HVD253
Number of nodes	64	Yes
Minimum differential input resistance	20 kΩ	Yes
Minimum differential input capacitance	24 pF	Yes
Bus pin voltage range (survivable)	–25 V to 18 V	Yes
Bus pin voltage range (operation)	–5 V to 10 V	Yes
Differential output voltage	1.5 V with 50-Ω load	Yes

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD252D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD252	Samples
SN65HVD252DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD252	Samples
SN65HVD253D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD253	Samples
SN65HVD253DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD253	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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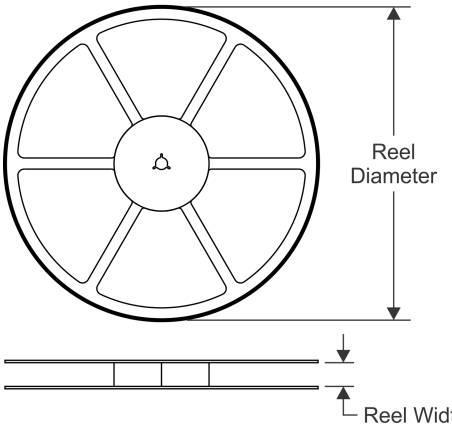
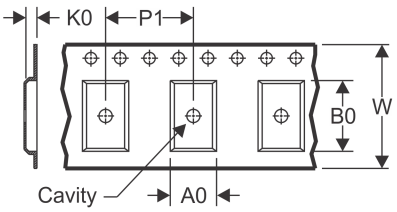
TAPE AND REEL INFORMATION

REEL DIMENSIONS

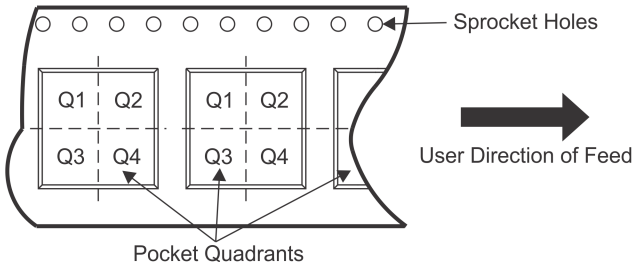


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

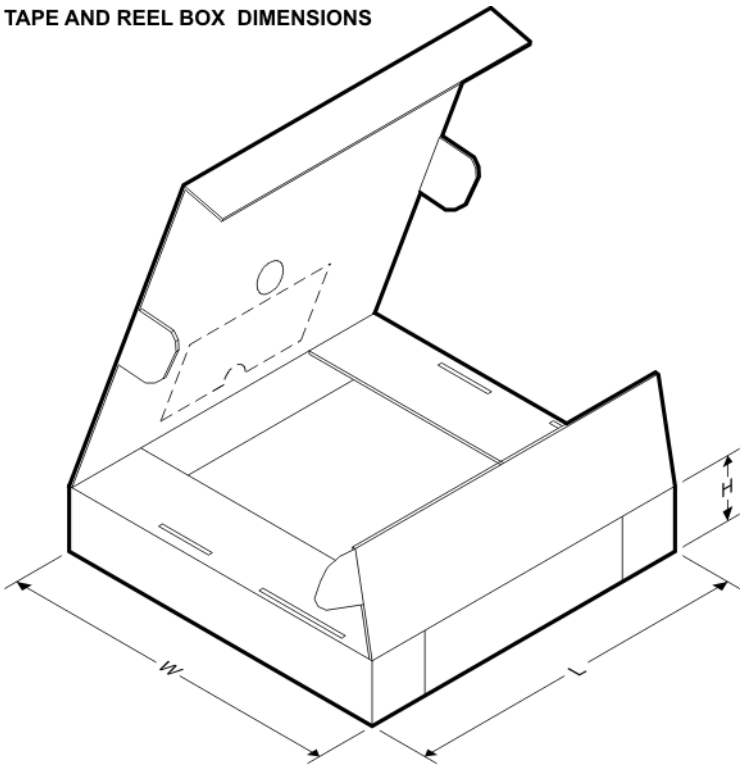
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

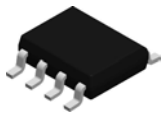
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD252DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD253DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD252DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD253DR	SOIC	D	8	2500	367.0	367.0	35.0

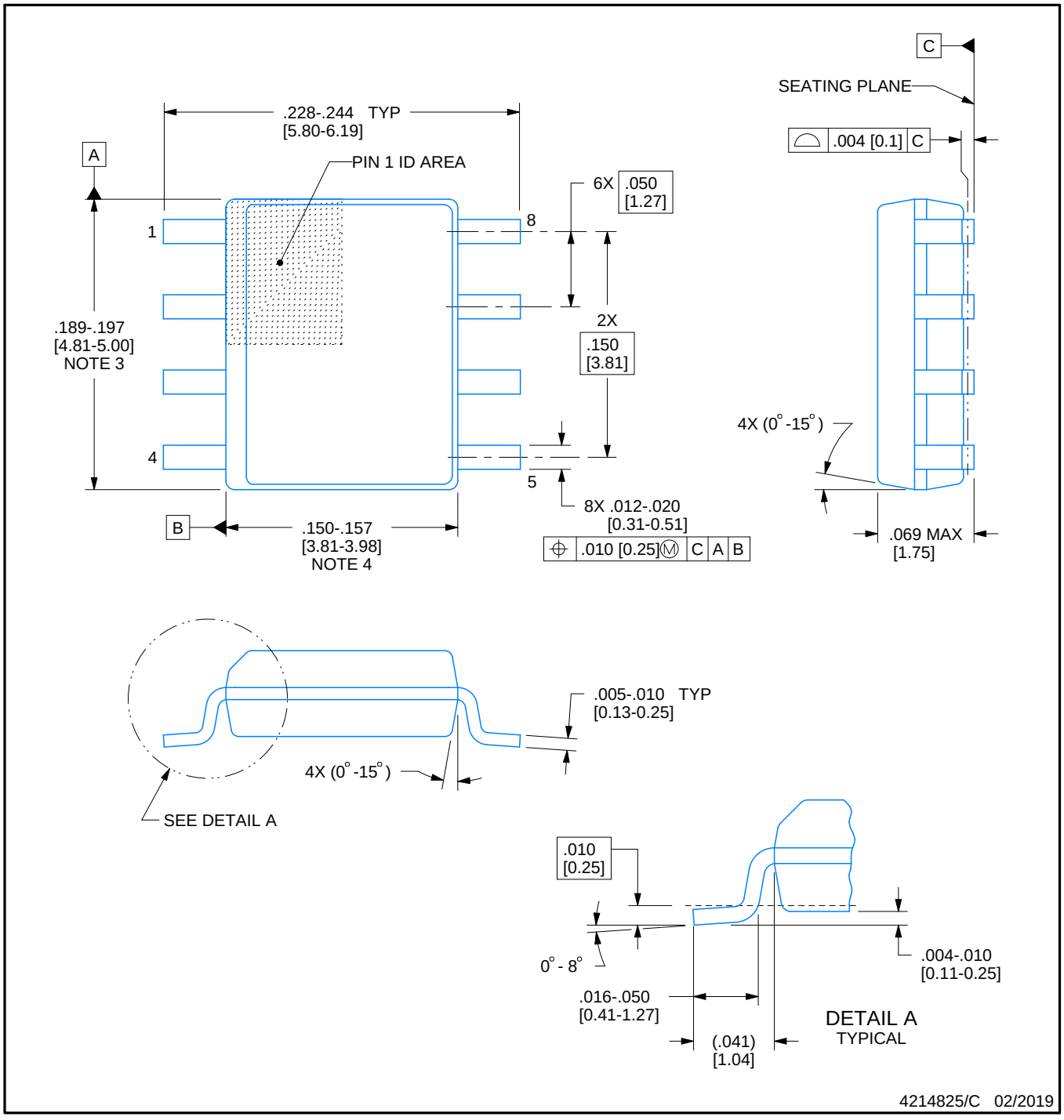


PACKAGE OUTLINE

D0008A

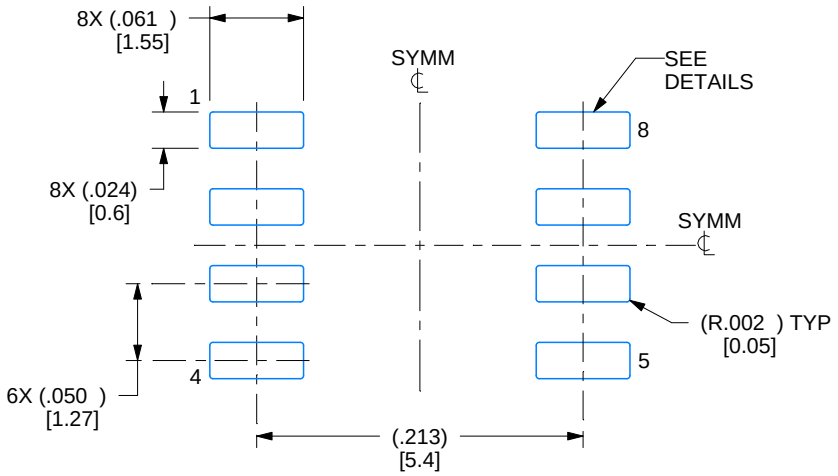
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

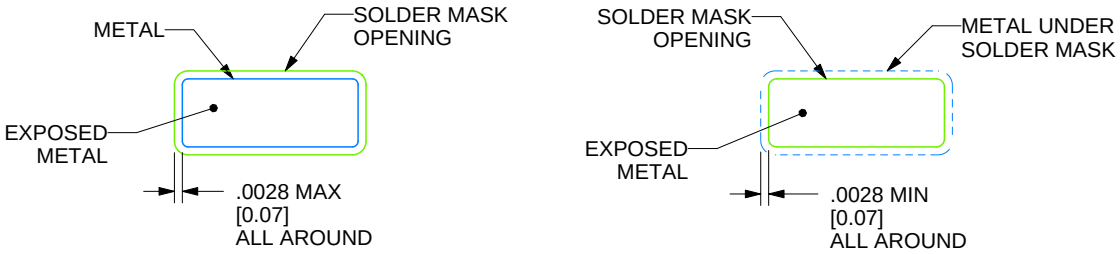


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

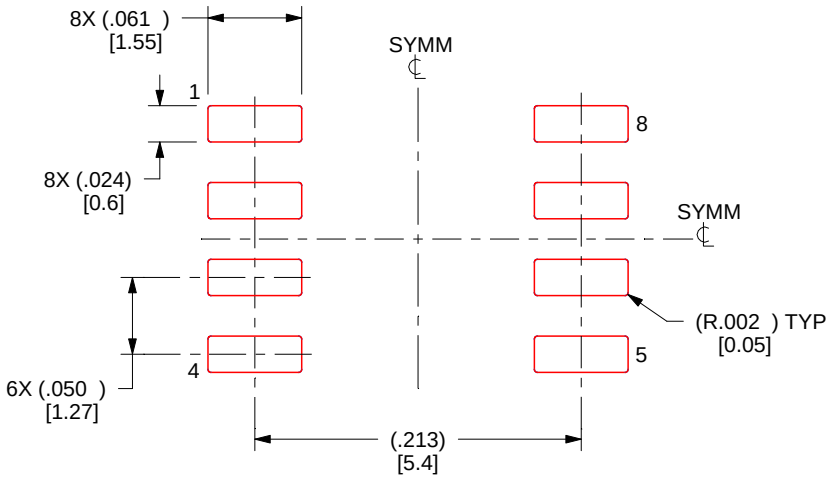
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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