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March 2013

#### FDB8443

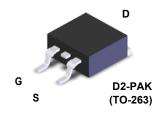
# N-Channel PowerTrench<sup>®</sup> MOSFET 40 V, 182 A, 3.0 m $\Omega$

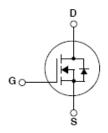
#### **Features**

- $\blacksquare$  R<sub>DS(on)</sub> = 2.3 m $\Omega$  ( Typ.)@ V<sub>GS</sub> = 10 V, I<sub>D</sub> = 80 A
- Q<sub>G(tot)</sub> = 142 nC ( Typ.)
- Low Miller Charge, Q<sub>GD</sub> = 32 nC( Typ.)
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

#### **Applications**

- Power Tools
- Motor drives and Uninterruptible Power Supplies
- Synchronous Rectification
- Battery Protection Circuit





## **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol		Parameter	FDB8443	Unit
$V_{DSS}$	Drain to Source Voltage		40	V
$V_{GS}$	Gate to Source Voltage		±20	V
		- Continuous (T <sub>C</sub> = 25°C, Silicon Limited)	182*	
	Drain Current	- Continuous (T <sub>C</sub> = 100°C, Silicon Limited)	129*	
ID		- Continuous (T <sub>C</sub> = 25°C, Package Limited)	120	Α
		- Continuous ( $T_A = 25^{\circ}C$ , $R_{\theta JA} = 43^{\circ}C/W$ )	25	
I <sub>DM</sub>	Drain Current	- Pulsed	See Figure 4	
E <sub>AS</sub>	Single Pulse Avalanche Ener	gy (Note 1)	531	mJ
D	Power Dissipation		188	W
$P_{D}$	Derate above 25°C		1.25	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temp	erature	-55 to +175	°C

<sup>\*</sup>Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

#### **Thermal Characteristics**

Symbol	Parameter	FDB8443	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case, Max.	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in <sup>2</sup> copper pad area, Max.	43	°C/W

Unit

nΑ

## **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Package	Reel Size	Tape Width	Quantity
FDB8443	FDB8443	TO-263AB	330mm	24mm	800 units

#### Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Parameter

Gate to Source Leakage Current

Off Characteristics						
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40	-	-	V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	V <sub>DS</sub> = 32V,	-	-	1	^	
	Zero Gate voltage Drain Current	$V_{GS} = 0V$ $T_C = 150^{\circ}C$	-	-	250	μΑ

 $V_{GS} = \pm 20V$ 

**Test Conditions** 

Min

Тур

Max

±100

#### **On Characteristics**

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	2.8	4	V
	I <sub>D</sub> = 80A, V <sub>GS</sub> = 10V	-	2.3	3.0		
r <sub>DS(on)</sub>	Drain to Source On Resistance	$I_D$ = 80A, $V_{GS}$ = 10V, $T_J$ = 175°C	-	4.2	5.5	mΩ

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 25V V - 4	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		9310	-	pF
C <sub>oss</sub>	Output Capacitance				800	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	- 1 - 11VII 12			510	-	pF
$R_G$	Gate Resistance	V <sub>GS</sub> = 0.5V, f = 1MHz		-	0.9	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V <sub>GS</sub> = 0 to 10V		-	142	185	nC
$Q_{g(TH)}$	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2V	V <sub>DD</sub> = 20V	-	17.5	23	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		I <sub>D</sub> = 35A	-	36	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau		I <sub>g</sub> = 1mA	-	18.8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	32	-	nC

#### **Switching Characteristics** (V<sub>GS</sub> = 10V)

t <sub>on</sub>	Turn-On Time	$V_{DD} = 20V, I_{D} = 35A$ $V_{GS} = 10V, R_{GS} = 2\Omega$	-	-	58	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	18.4	-	ns
t <sub>r</sub>	Rise Time		-	17.9	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	55	-	ns
t <sub>f</sub>	Fall Time		-	13.5	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	109	ns

#### **Drain-Source Diode Characteristics**

V <sub>SD</sub> Source to Drain Diode	Source to Drain Diade Voltage	I <sub>SD</sub> = 35A	-	0.8	1.25	\/
	Source to Drain blode voltage	I <sub>SD</sub> = 15A	-	0.8	1.0	v
t <sub>rr</sub>	Reverse Recovery Time	- I <sub>SD</sub> = 35A, dI <sub>SD</sub> /dt = 100A/μs	-	42	55	ns
Q <sub>rr</sub>	Reverse Recovery Charge	ISD - 35A, αISD/αι - 100A/μS	-	48	62	nC

#### Notes:

- **1:** Starting  $T_J = 25^{\circ}C$ , L = 0.26mH,  $I_{AS} = 64$ A. **2:** Pulse width = 100s.

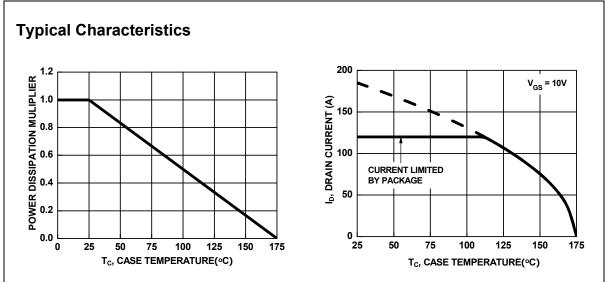


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

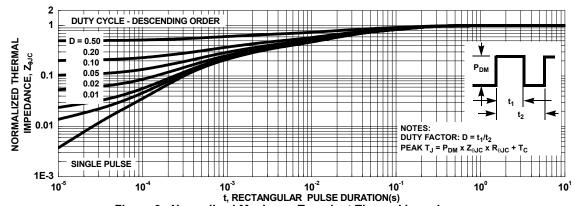


Figure 3. Normalized Maximum Transient Thermal Impedance

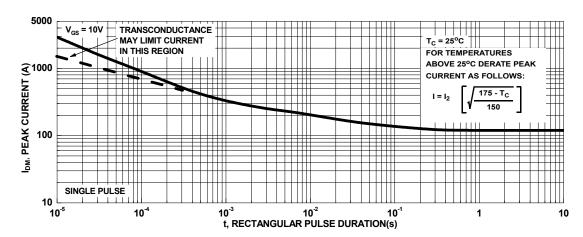
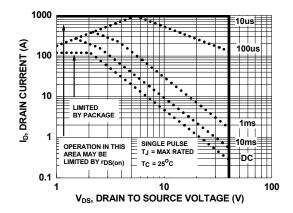


Figure 4. Peak Current Capability

#### **Typical Characteristics**



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

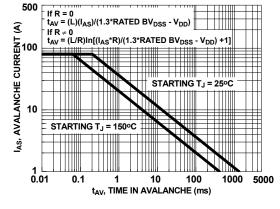
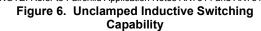
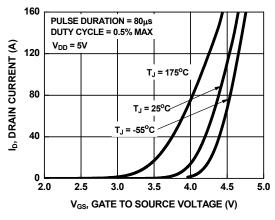


Figure 5. Forward Bias Safe Operating Area

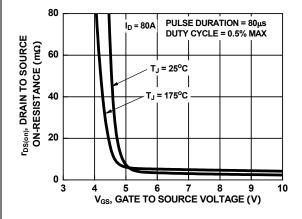




PULSE DURATION =  $80\mu s$  DUTY CYCLE = 0.5% MAX  $V_{GS} = 10V$   $V_{GS} = 4.5V$   $V_{GS} = 4V$   $V_{DS}$ , DRAIN TO SOURCE VOLTAGE (V)

Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



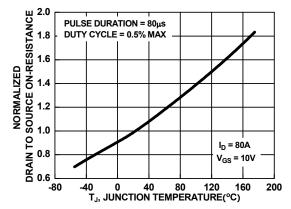


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

## **Typical Characteristics**

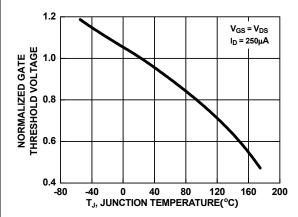


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

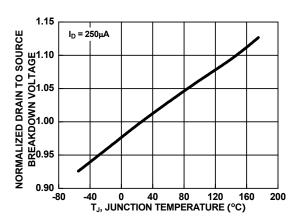


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

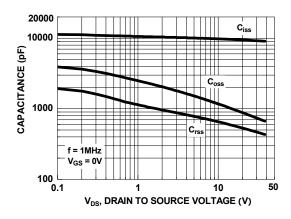


Figure 13. Capacitance vs Drain to Source Voltage

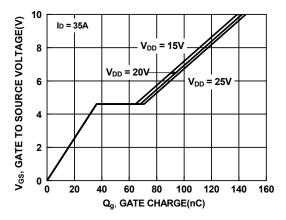


Figure 14. Gate Charge vs Gate to Source Voltage





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