



# PCF8593

## Low power clock and calendar

Rev. 04 — 6 October 2010

Product data sheet

## 1. General description

The PCF8593 is a CMOS<sup>1</sup> clock and calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I<sup>2</sup>C-bus. The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock, calendar, and counter functions. The next 8 bytes can be programmed as alarm registers or used as free RAM space.

## 2. Features and benefits

- I<sup>2</sup>C-bus interface operating supply voltage: 2.5 V to 6.0 V
- Clock operating supply voltage 1.0 V to 6.0 V at 0 °C to +70 °C
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 V to 6.0 V
- External  $\overline{\text{RESET}}$  input resets I<sup>2</sup>C interface only
- Operating current (at  $f_{\text{SCL}} = 0$  Hz, 32 kHz time base,  $V_{\text{DD}} = 2.0$  V): typical 1  $\mu\text{A}$
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 hour or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input and output bus (I<sup>2</sup>C-bus)
- Automatic word address incrementing
- Programmable alarm, timer, and interrupt function
- Space-saving SO8 package available
- Slave addresses: A3h for reading, A2h for writing

## 3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 14](#).



### 4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8593P	PCF8593P
PCF8593T	8583T

### 5. Block diagram

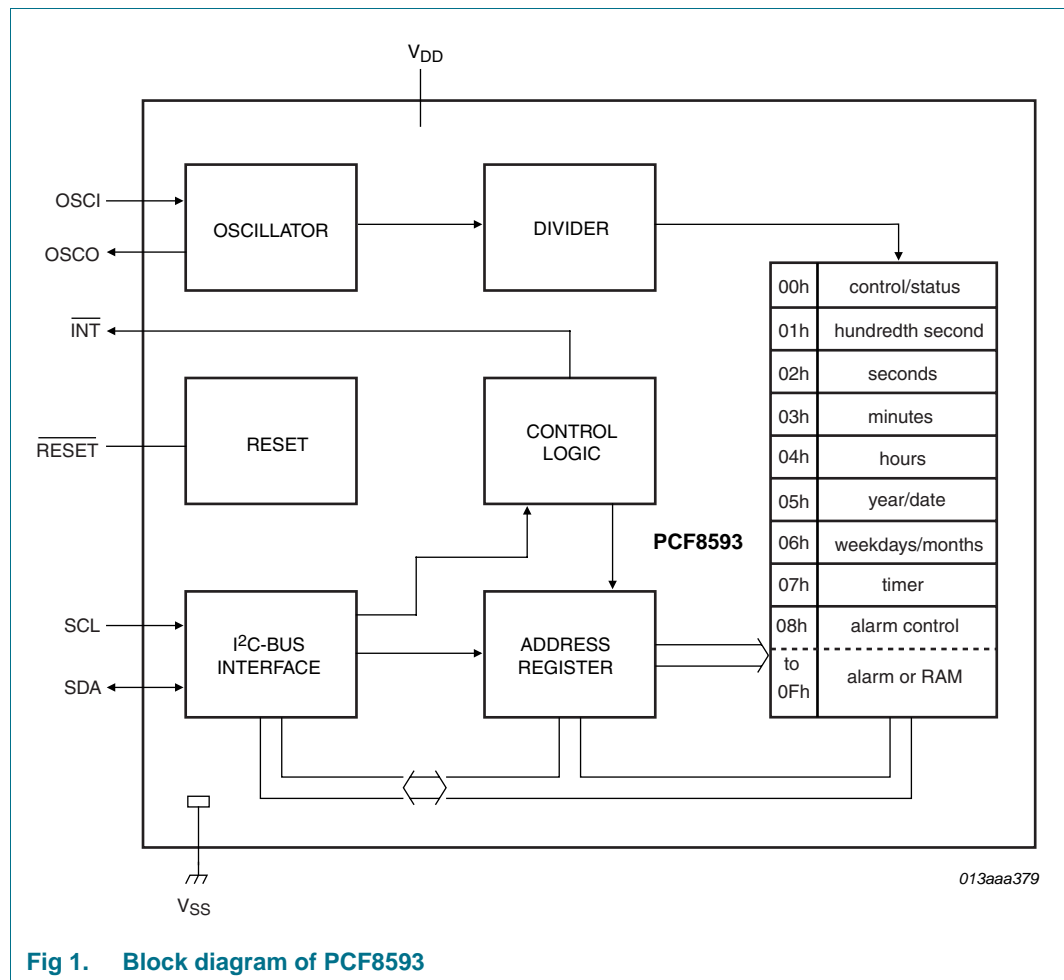
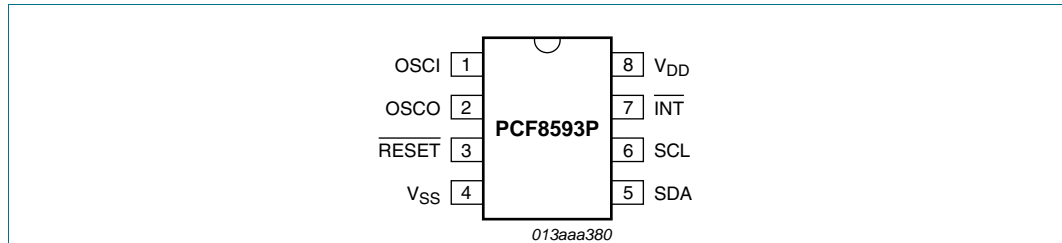


Fig 1. Block diagram of PCF8593

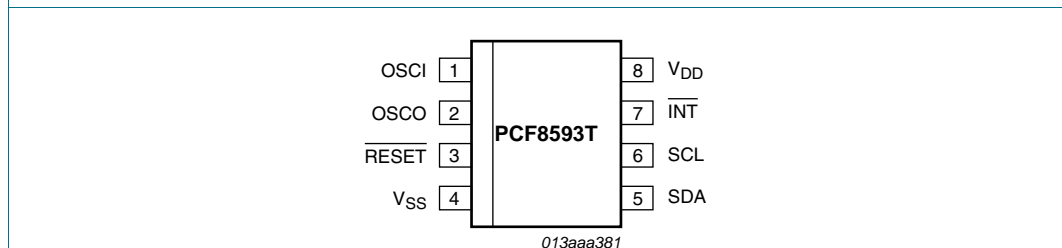
## 6. Pinning information

### 6.1 Pinning



Top view. For mechanical details, see [Figure 24](#).

**Fig 2. Pin configuration for DIP8 (PCF8593P)**



Top view. For mechanical details, see [Figure 25](#).

**Fig 3. Pin configuration for SO8 (PCF8593T)**

### 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin		Type	Description
	DIP8 (PCF8593P)	SO8 (PCF8593T)		
OSCI	1	1	input	oscillator input, 50 Hz or event-pulse input
OSCO	2	2	output	oscillator output
$\overline{\text{RESET}}$	3	3	input	reset
V <sub>SS</sub>	4	4	supply	ground supply voltage
SDA	5	5	input/output	serial data line
SCL	6	6	input	serial clock line
$\overline{\text{INT}}$	7	7	output	open-drain interrupt output (active LOW)
V <sub>DD</sub>	8	8	supply	supply voltage

## 7. Functional description

The PCF8593 contains sixteen 8 bit registers with an 8 bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I<sup>2</sup>C-bus interface.

The first 8 registers (memory addresses 00h to 07h) are designed as addressable 8 bit parallel registers. The first register (memory address 00h) is used as a control and status register. The memory addresses 01h to 07h are used as counters for the clock function. The memory addresses 08h to 0Fh may be programmed as alarm registers or used as free RAM locations.

### 7.1 Counter function modes

When the control and status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a Binary Coded Decimal (BCD) format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01h to 07h), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the counter during a carry condition is prevented. When a counter is written, other counters are not affected.

### 7.2 Alarm function modes

By setting the alarm enable bit of the control and status register the alarm control register (address 08h) is activated.

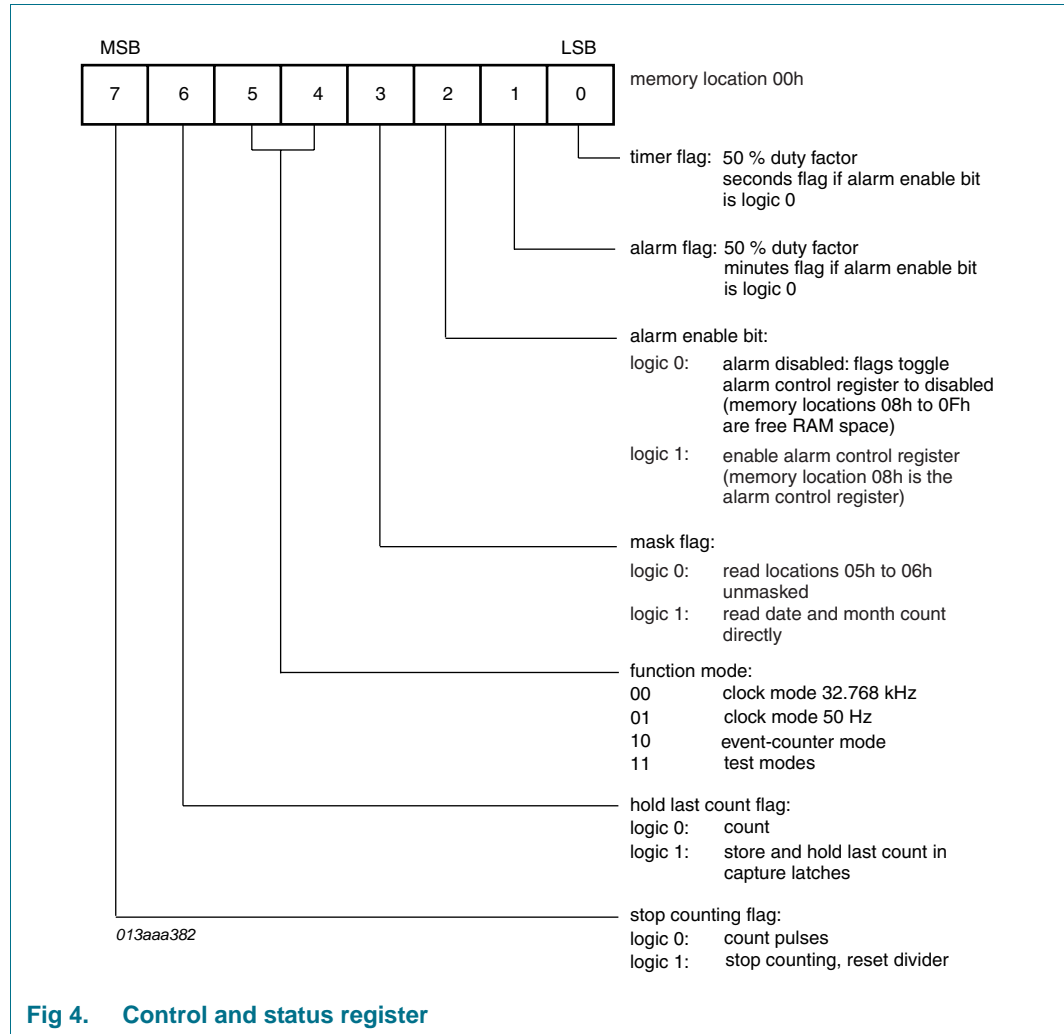
By setting the alarm control register, a dated alarm, a daily alarm, a weekday alarm, or a timer alarm may be programmed. In the clock modes, the timer register (address 07h) may be programmed to count hundredths of a second, seconds, minutes, hours, or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control and status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (bit 2 of control and status register set logic 0) the alarm registers at addresses 08h to 0Fh may be used as free RAM.

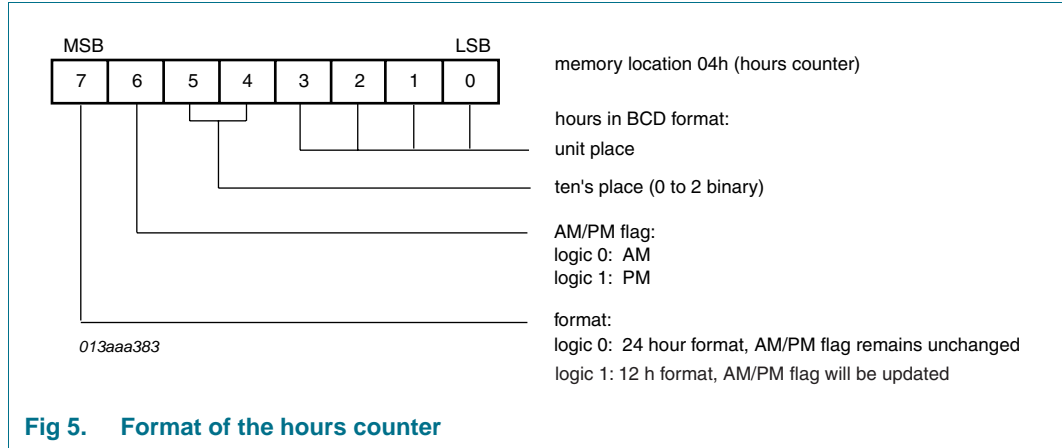
### 7.3 Control and status register

The control and status register is defined as the memory location 00h with free access for reading and writing via the I<sup>2</sup>C-bus. All functions and options are controlled by the contents of the control and status register (see [Figure 4](#)).

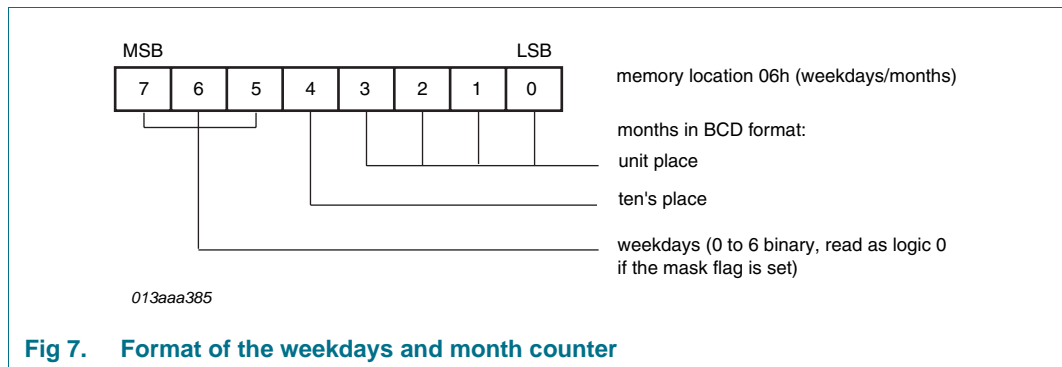
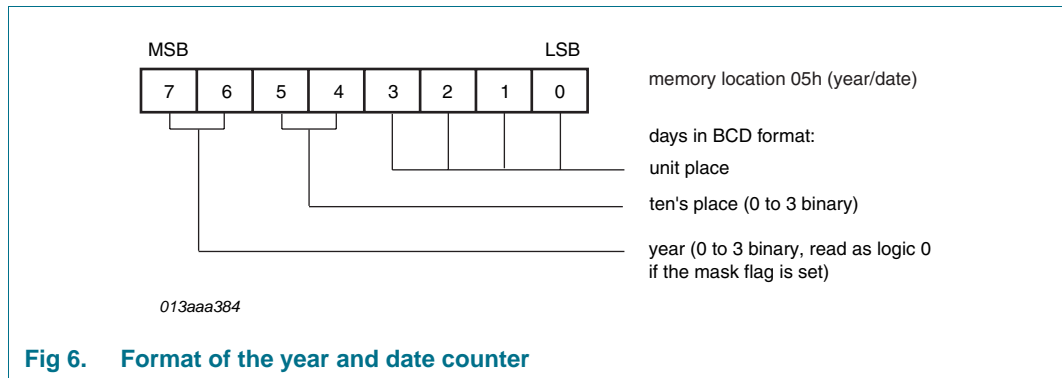


### 7.4 Counter registers

The format for 24 hour or 12 hour clock modes can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in [Figure 5](#).



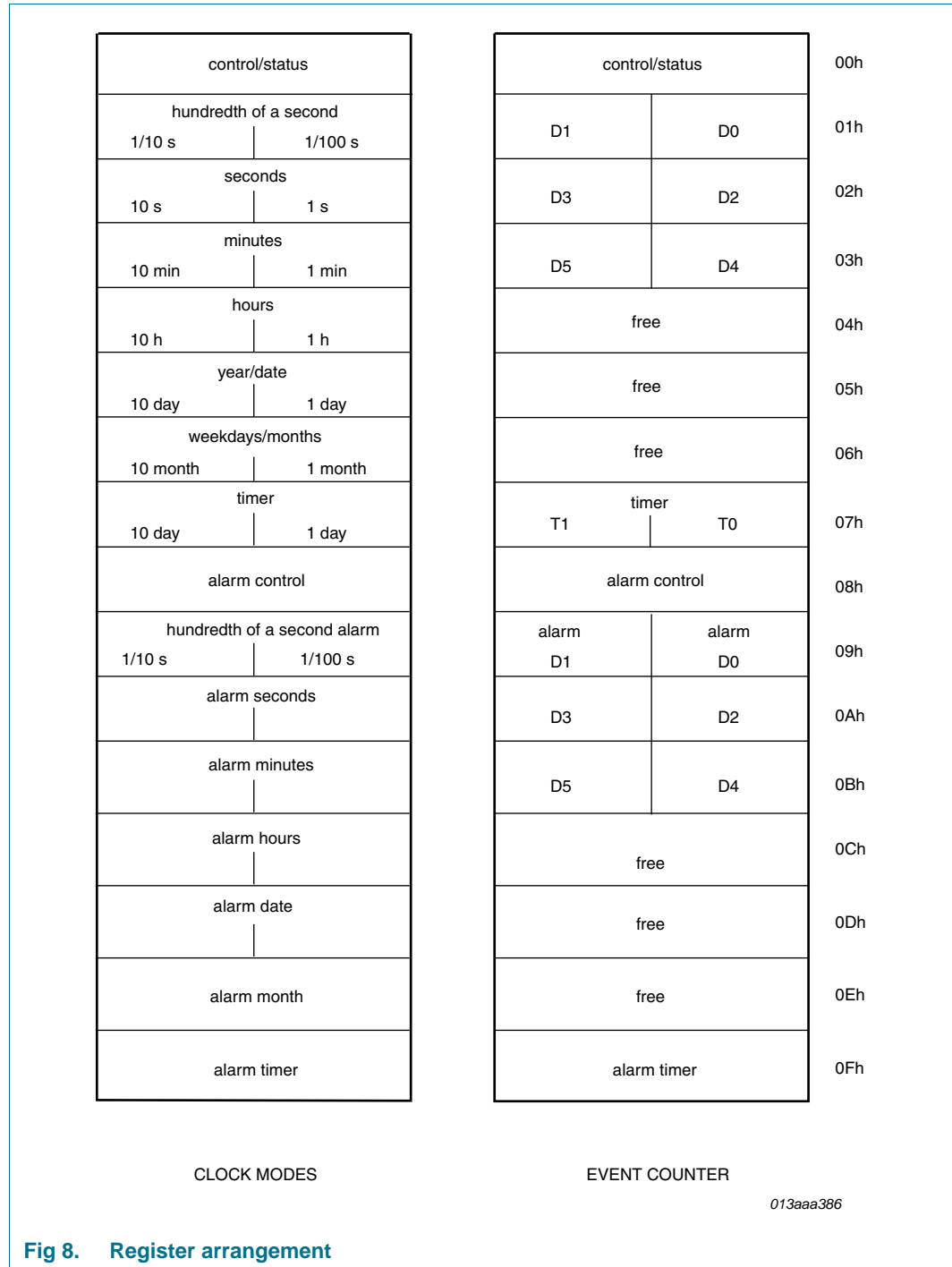
The year and date are stored in memory location 05h (see [Figure 6](#)). The weekdays and months are in memory location 06h (see [Figure 7](#)).



When reading these memory locations the year and weekdays are masked out when the mask flag of the control and status register is set. This allows the user to read the date and month count directly.

In the event-counter mode, events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in [Figure 8](#). Counter cycles are listed in [Table 4](#).



**Fig 8. Register arrangement**

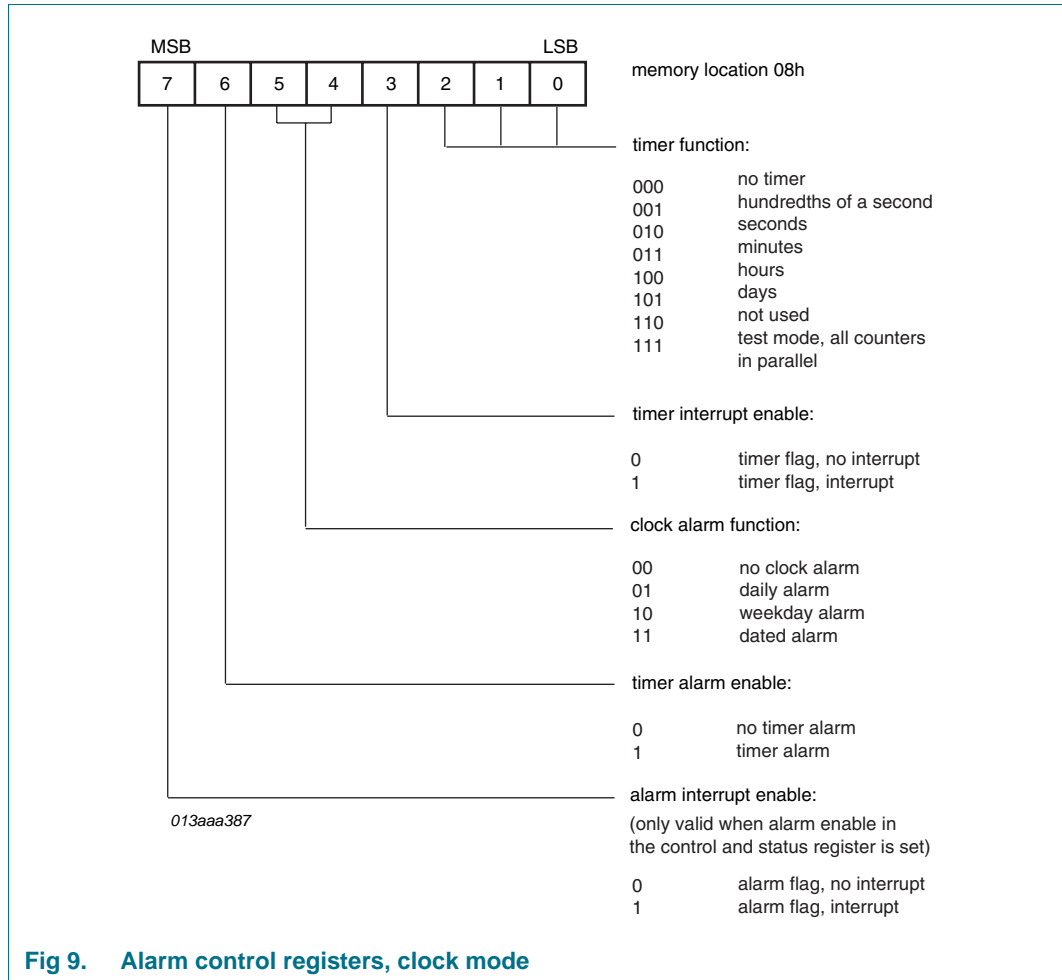
**Table 4. Cycle length of the time counters, clock modes**

Unit	Counting cycle	Carry to next unit	Contents of month calendar
hundredths of a second	00 to 99	99 to 00	-
seconds	00 to 59	59 to 00	-
minutes	00 to 59	59 to 00	-
hours (24)	00 to 23	23 to 00	-
hours (12)	12 am	-	-
	01 am to 11 am	-	-
	12 pm	-	-
	01 pm to 11 pm	11 pm to 12 am	-
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, and 12
	01 to 30	30 to 01	4, 6, 9, and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, and 3
months	01 to 12	12 to 01	-
year	0 to 3	-	-
weekdays	0 to 6	6 to 0	-
timer	00 to 99	no carry	-

## 7.5 Alarm control register

When the alarm enable bit of the control and status register is set (address 00h, bit 2) the alarm control register (address 08h) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see [Figure 9](#)).



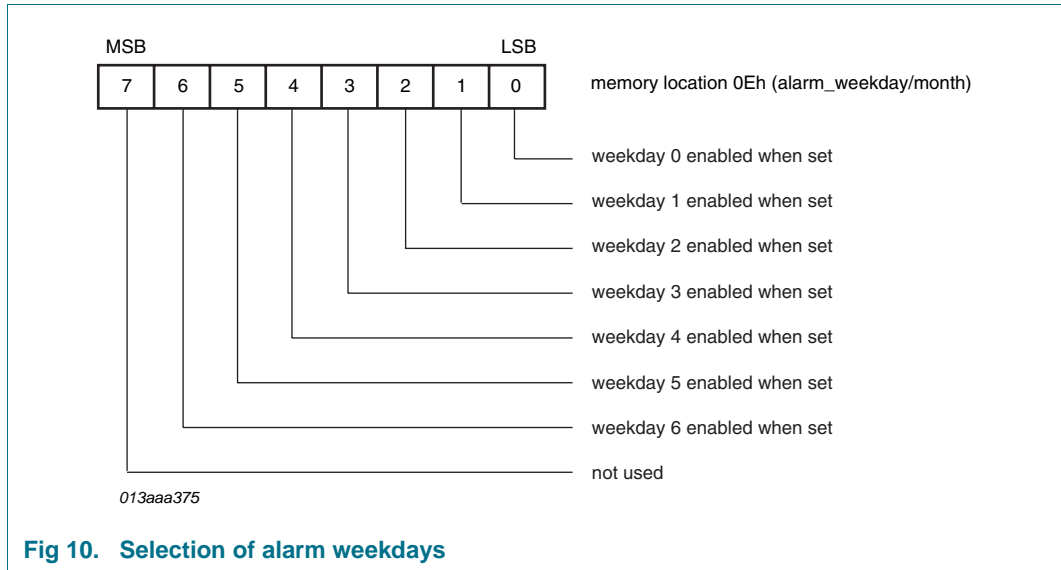


## 7.6 Alarm registers

All alarm registers are allocated with a constant address offset of 08h to the corresponding counter registers (see [Figure 8](#)).

An alarm signal is generated when the contents of the alarm registers match bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday and month register selects the weekdays on which an alarm is activated (see [Figure 10](#)).

**Remark:** In the 12 hour mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

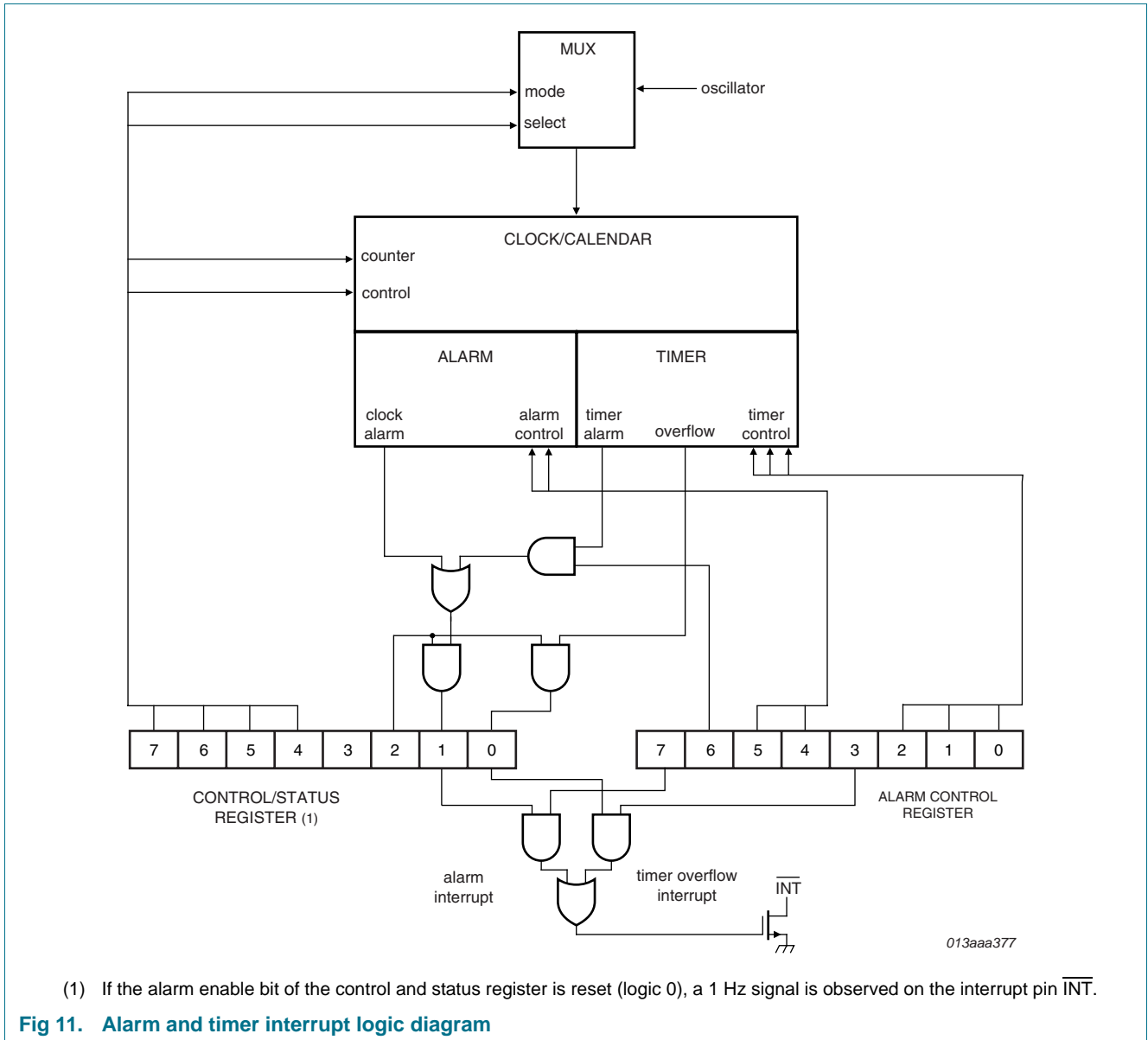


### 7.7 Timer

The timer (location 07h) is enabled by setting the control and status register to XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control and status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0Fh), the alarm flag is set (bit 1 of the control and status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see [Figure 11](#)).



### 7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 10 in the control and status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit).

The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in the registers 1h, 2h, and 3h. Therefore, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in the registers 9h, Ah, and Bh, and the event alarm is enabled (bits 4 and 5 which are logic 01 in the alarm control register). In this event, the alarm flag (bit 1 of the control and status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In

this mode, the timer (location 07h) increments once for every one, one hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0, 1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

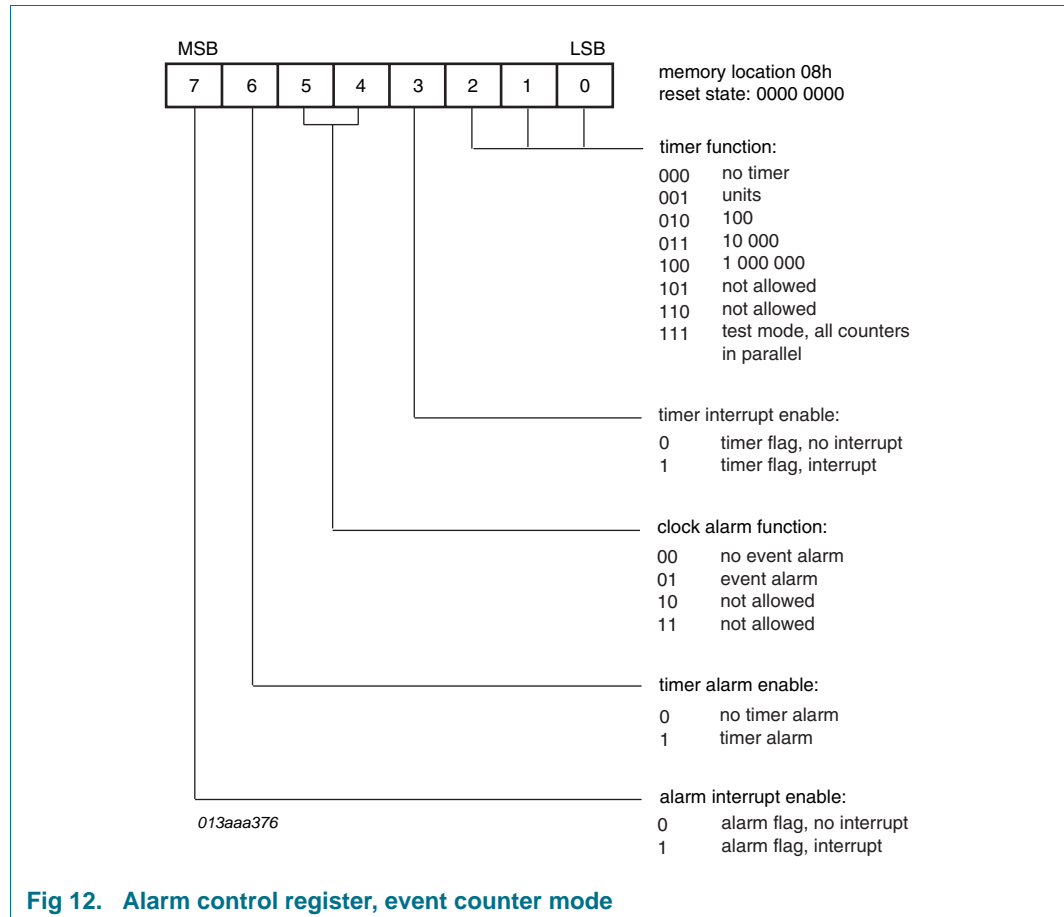


Fig 12. Alarm control register, event counter mode

### 7.9 Interrupt control

The conditions for activating the output  $\overline{\text{INT}}$  (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of the control and status register is logic 0), the interrupt output toggles at 1 Hz with a 50 % duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in [Figure 11](#).

### 7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSC1 and OSC0. A trimmer capacitor between OSC1 and  $V_{DD}$  is used for tuning the oscillator (see [Section 11.1](#)). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

**7.10.1 Designing**

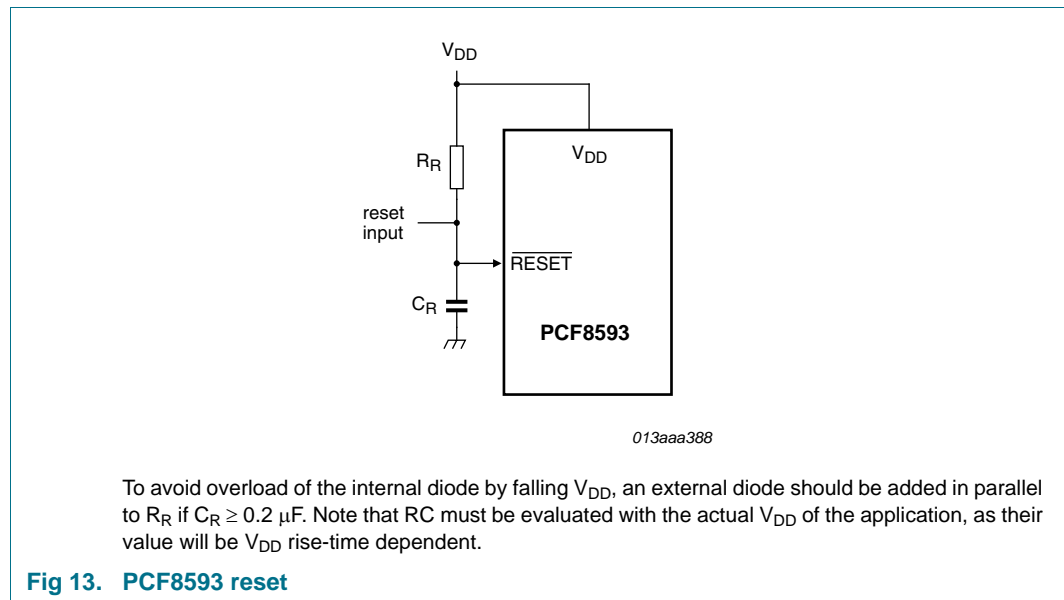
When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

**7.11 Initialization**

Note that immediately following power-on, all internal registers are undefined and, following a  $\overline{\text{RESET}}$  pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external  $\overline{\text{RESET}}$  pulse (active LOW) at pin 3. When reset occurs only the I<sup>2</sup>C-bus interface is reset. The control and status register and all clock counters are not affected by  $\overline{\text{RESET}}$ .  $\overline{\text{RESET}}$  must return HIGH during device operation.

An RC combination can also be utilized to provide a power-on  $\overline{\text{RESET}}$  signal at pin 3. In this event, the values of the PCF8593 must fulfil the following relationship to guarantee power-on reset (see [Figure 13](#)).



$\overline{\text{RESET}}$  input must be  $\leq 0.3V_{DD}$  when  $V_{DD}$  reaches  $V_{DD(\text{min})}$  (or higher).

It is recommended to set the stop counting flag of the control and status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

## 8. Characteristics of the I<sup>2</sup>C-bus

### 8.1 Characteristics

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

#### 8.1.1 Bit transfer

One data bit is transferred during each clock pulse (see [Figure 14](#)). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal.

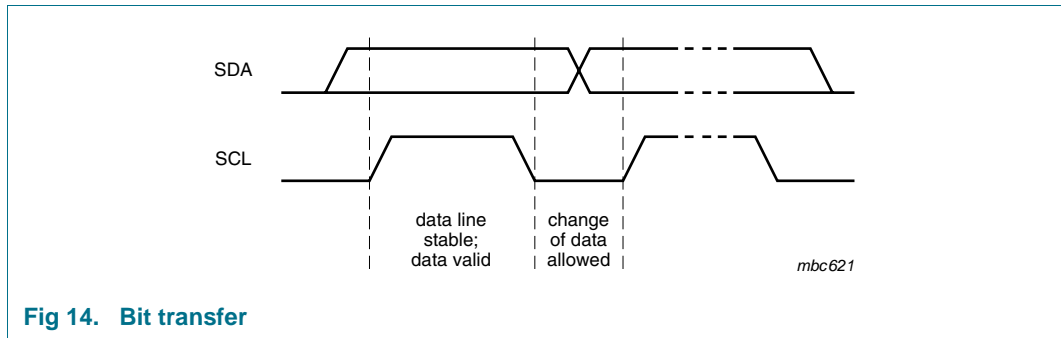


Fig 14. Bit transfer

#### 8.1.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see [Figure 15](#)).

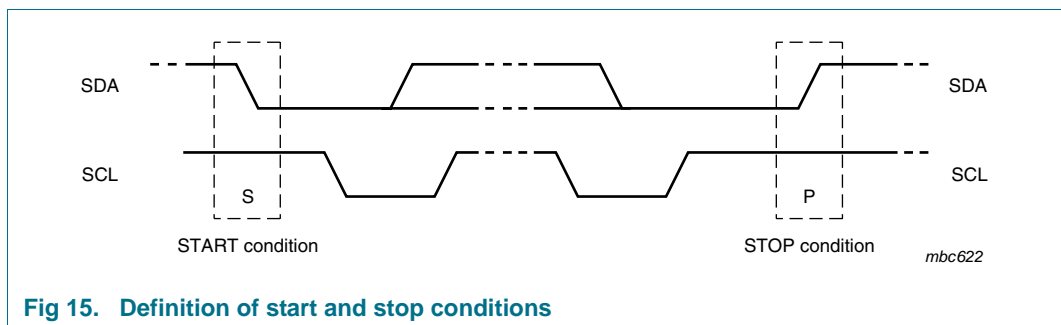


Fig 15. Definition of start and stop conditions

#### 8.1.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver (see [Figure 16](#)). The device that controls the message is the master; and the devices which are controlled by the master are the slaves.

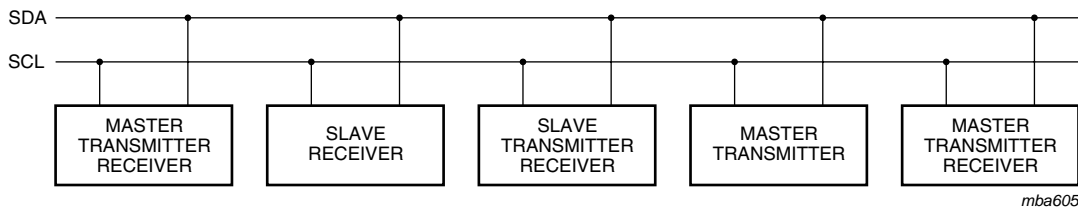


Fig 16. System configuration

### 8.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I<sup>2</sup>C-bus is illustrated in [Figure 17](#).

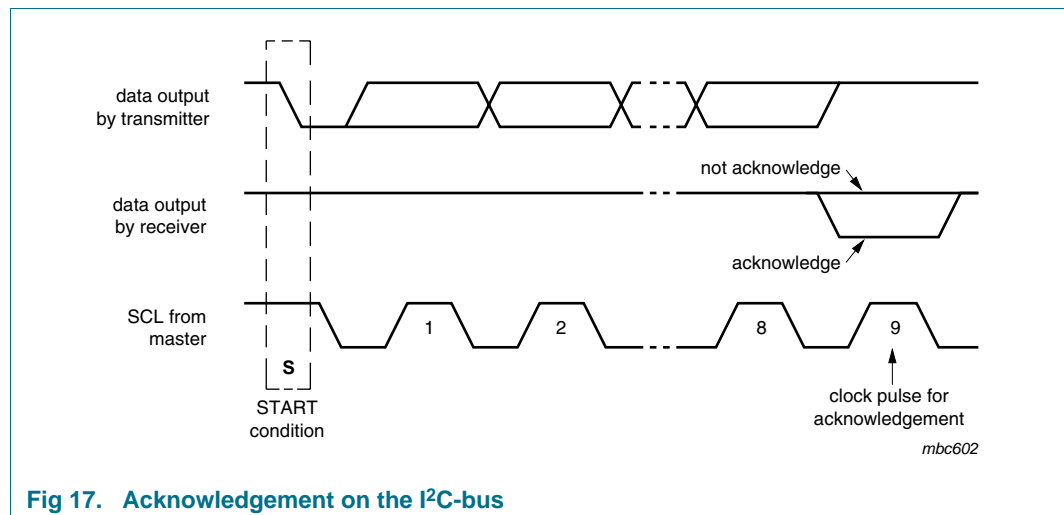


Fig 17. Acknowledgement on the I<sup>2</sup>C-bus

## 8.2 I<sup>2</sup>C-bus protocol

### 8.2.1 Addressing

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which must respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock and calendar acts as a slave receiver or slave transmitter. The clock signal SCL is only an input signal but the data signal SDA is a bidirectional line.

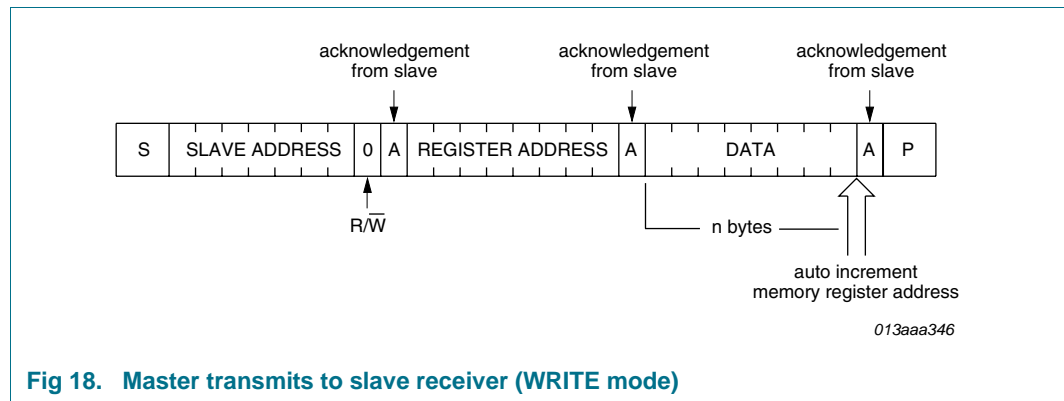
The clock and calendar slave address is shown in [Table 5](#).

**Table 5. I<sup>2</sup>C slave address byte**

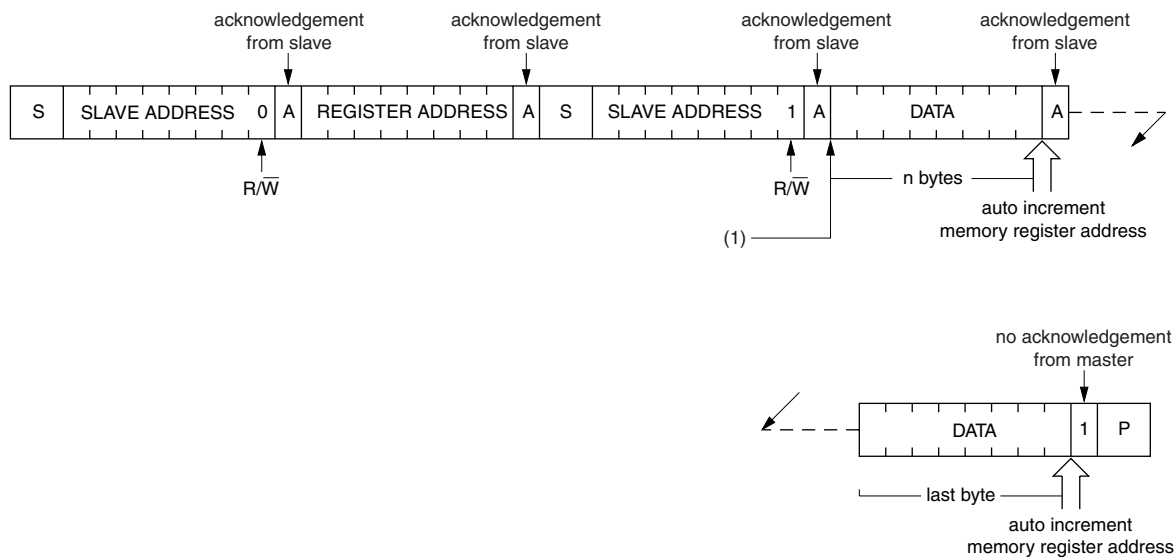
Bit	Slave address							0 LSB R/W
	7 MSB	6	5	4	3	2	1	
	1	0	1	0	0	0	1	

### 8.2.2 Clock and calendar READ or WRITE cycles

The I<sup>2</sup>C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in [Figure 18](#), [Figure 19](#) and [Figure 20](#).

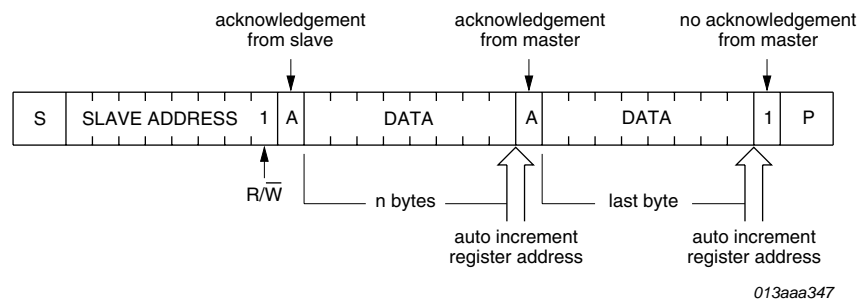






(1) At this moment master transmitter becomes master receiver and PCF8593 slave receiver becomes slave transmitter.

**Fig 19. Master reads after setting word address (write word address; READ data)**



**Fig 20. Master reads slave immediately after first byte (READ mode)**

## 9. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DD}$	supply voltage		-0.8	+0.7	V	
$I_{DD}$	supply current		-	50	mA	
$I_{SS}$	ground supply current		-	50	mA	
$V_I$	input voltage		-0.8	$V_{DD} + 0.8$	V	
$I_I$	input current		-	10	mA	
$I_O$	output current		-	10	mA	
$P_{tot}$	total power dissipation		-	300	mW	
$P_o$	output power		-	50	mW	
$V_{ESD}$	electrostatic discharge voltage	HBM	[1]	-	±3000	V
		MM	[2]	-	±300	V
$I_{lu}$	latch-up current		[3]	-	100	mA
$T_{stg}$	storage temperature		[4]	-65	+150	°C
$T_{amb}$	ambient temperature	operating device		-40	+85	°C

[1] Pass level; Human Body Model (HBM), according to [Ref. 5 "JESD22-A114"](#).

[2] Pass level; Machine Model (MM), according to [Ref. 6 "JESD22-A115"](#).

[3] Pass level; latch-up testing according to [Ref. 7 "JESD78"](#) at maximum ambient temperature ( $T_{amb(max)}$ ).

[4] According to the NXP store and transport requirements (see [Ref. 9 "NX3-00092"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

## 10. Characteristics

### 10.1 Static characteristics

**Table 7. Static characteristics**

$V_{DD} = 2.5\text{ V to }6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
$V_{DD}$	supply voltage	operating mode					
		I <sup>2</sup> C-bus active	2.5	-	6.0	V	
		I <sup>2</sup> C-bus inactive	1.0	-	6.0	V	
		quartz oscillator					
		$T_{amb} = 0\text{ °C to }+70\text{ °C}$	[2]	1.0	-	6.0	V
	$T_{amb} = -40\text{ °C to }+85\text{ °C}$	[2]	1.2	-	6.0	V	
$I_{DD}$	supply current	operating mode					
		$f_{SCL} = 100\text{ kHz}$ clock mode	[3]	-	-	200	$\mu\text{A}$
		clock mode; $f_{SCL} = 0\text{ Hz}$					
		$V_{DD} = 2.0\text{ V}$	-	1.0	8.0	$\mu\text{A}$	
		$V_{DD} = 5.0\text{ V}$	-	4	15	$\mu\text{A}$	

#### Pin SDA, SCL and INT

$V_{IL}$	LOW-level input voltage		0	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	-	-	mA
$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_I$	input capacitance		[4]	-	7	pF

#### Pins OSCI and RESET

$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$	-250	-	+250	nA
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#### Pin INT

$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	1	-	-	mA
$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$

#### Pin SCL

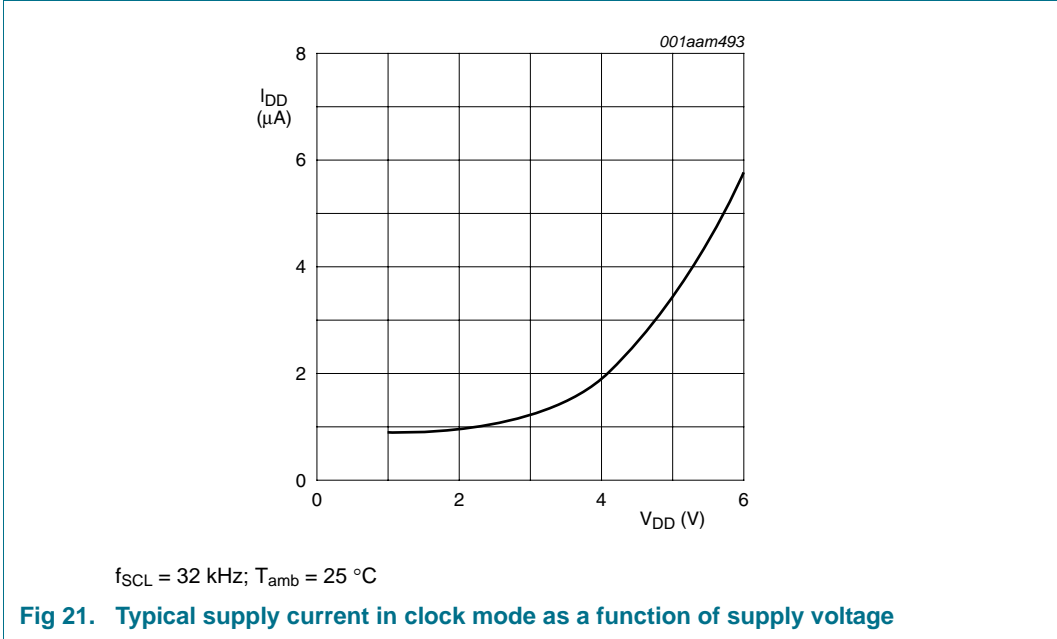
$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_I$	input capacitance		[4]	-	7	pF

[1] Typical values measured at  $T_{amb} = 25\text{ °C}$ .

[2] When the device is powered on,  $V_{DD}$  must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.

[3] Event counter mode: supply current dependant upon input frequency.

[4] Tested on a sample basis.



## 10.2 Dynamic characteristics

**Table 8. Dynamic characteristics**

$V_{DD} = 2.5\text{ V to }6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Oscillator</b>						
$C_{OSCO}$	capacitance on pin OSCO		20	25	30	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	for $\Delta V_{DD} = 100\text{ mV}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; $V_{DD} = 1.5\text{ V}$	-	0.2	-	ppm
$f_{clk(ext)}$	external clock frequency		[1]	-	1	MHz
<b>Quartz crystal parameters (f = 32.768 kHz)</b>						
$R_S$	series resistance		-	-	40	k $\Omega$
$C_L$	parallel load capacitance		-	10	-	pF
$C_{trim}$	trimmer capacitance		5	-	25	pF
<b>I<sup>2</sup>C-bus timing (see Figure 21)[2]</b>						
$f_{SCL}$	SCL clock frequency		-	-	100	kHz
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter		-	-	100	ns
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	-	$\mu\text{s}$
$t_{SU,STA}$	set-up time for a repeated START condition		4.7	-	-	$\mu\text{s}$
$t_{HD,STA}$	hold time (repeated) START condition		4.0	-	-	$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		4.7	-	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	-	$\mu\text{s}$
$t_r$	rise time of both SDA and SCL signals		-	-	1.0	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals		-	-	0.3	$\mu\text{s}$
$t_{SU,DAT}$	data set-up time		250	-	-	ns
$t_{HD,DAT}$	data hold time		0	-	-	ns
$t_{VD,DAT}$	data valid time		-	-	3.4	$\mu\text{s}$
$t_{SU,STO}$	set-up time for STOP condition		4.0	-	-	$\mu\text{s}$

[1] Event counter mode only.

[2] All timing values are valid within the operating supply voltage, ambient temperature range, reference to  $V_{IL}$  and  $V_{IH}$  and with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

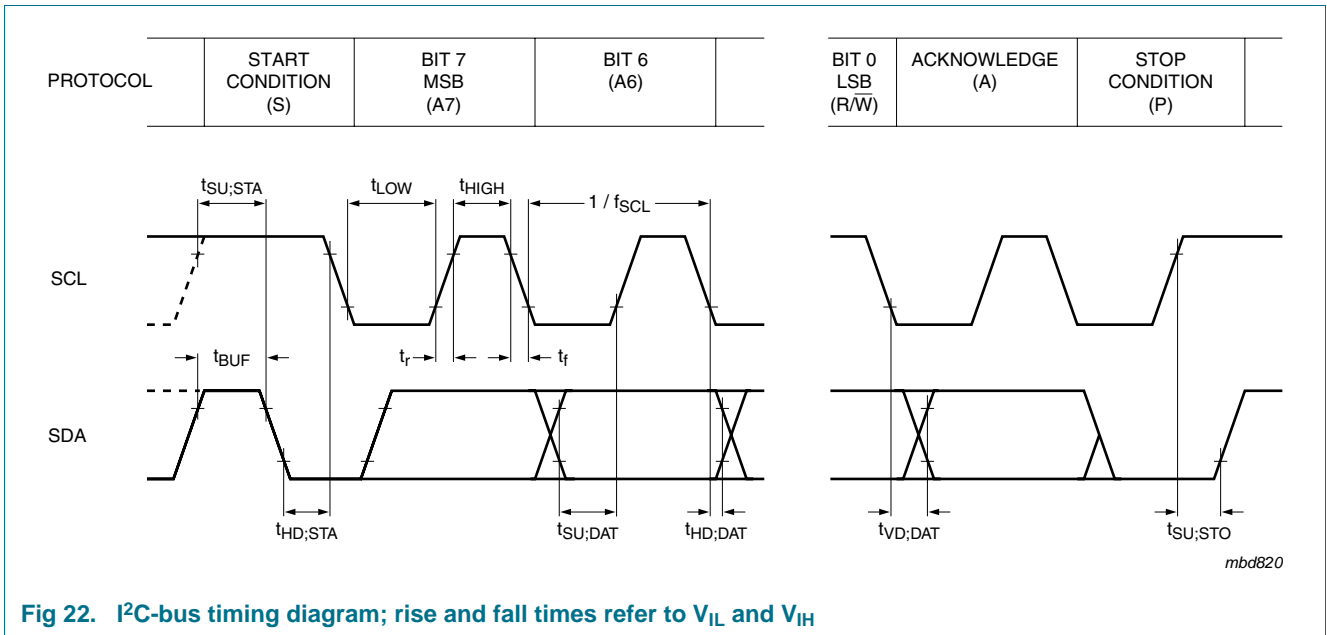


Fig 22. I<sup>2</sup>C-bus timing diagram; rise and fall times refer to  $V_{IL}$  and  $V_{IH}$

## 11. Application information

### 11.1 Oscillator frequency adjustment

#### 11.1.1 Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average  $\pm 5 \times 10^{-6}$ ). Average deviations of  $\pm 5$  minutes per year can be achieved.

#### 11.1.2 Method 2: OSCI trimmer

Using the alarm function (via the I<sup>2</sup>C-bus) a signal faster than the 1 Hz is generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power the device on
- Apply  $\overline{\text{RESET}}$ .

Routine:

- Set clock to time  $t$  and set alarm to time  $t + \Delta t$
- at time  $t + \Delta t$  (interrupt) repeat routine.

#### 11.1.3 Method 3: Direct measurement

Direct measurement of oscillator output (allowing for test probe capacitance).

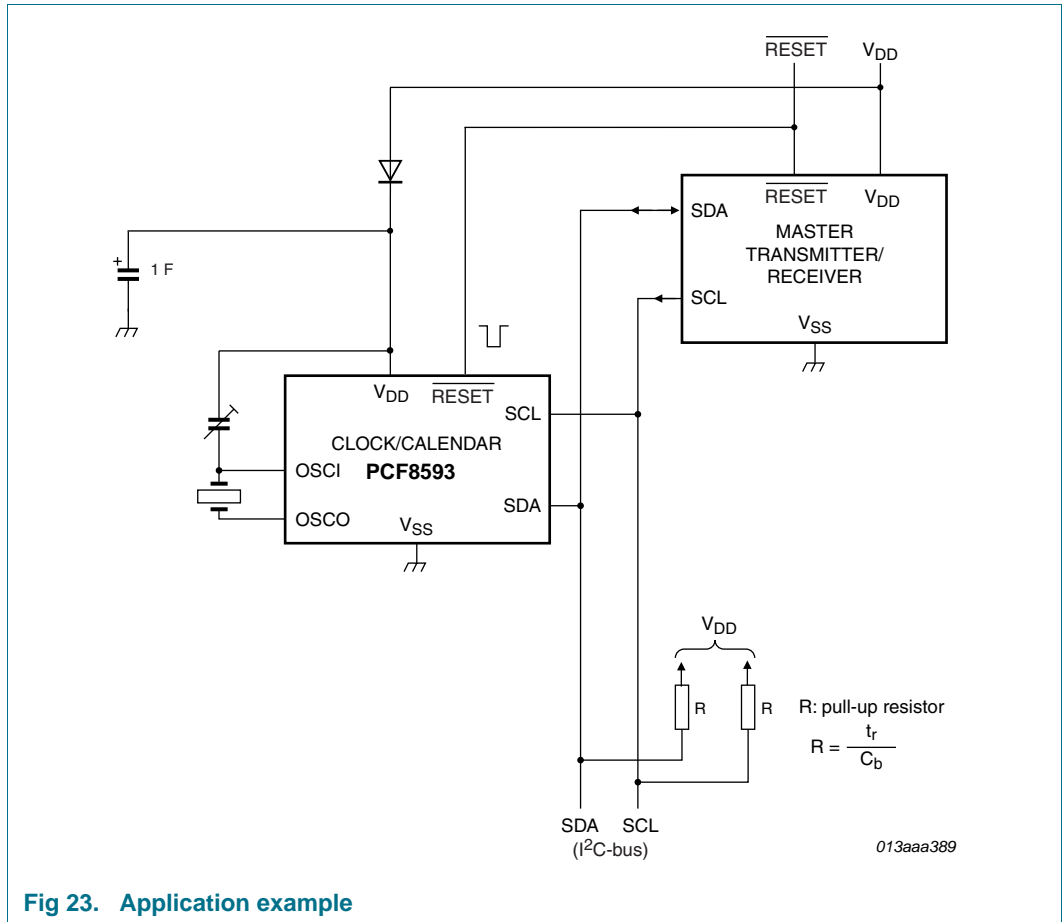


Fig 23. Application example



## 12. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

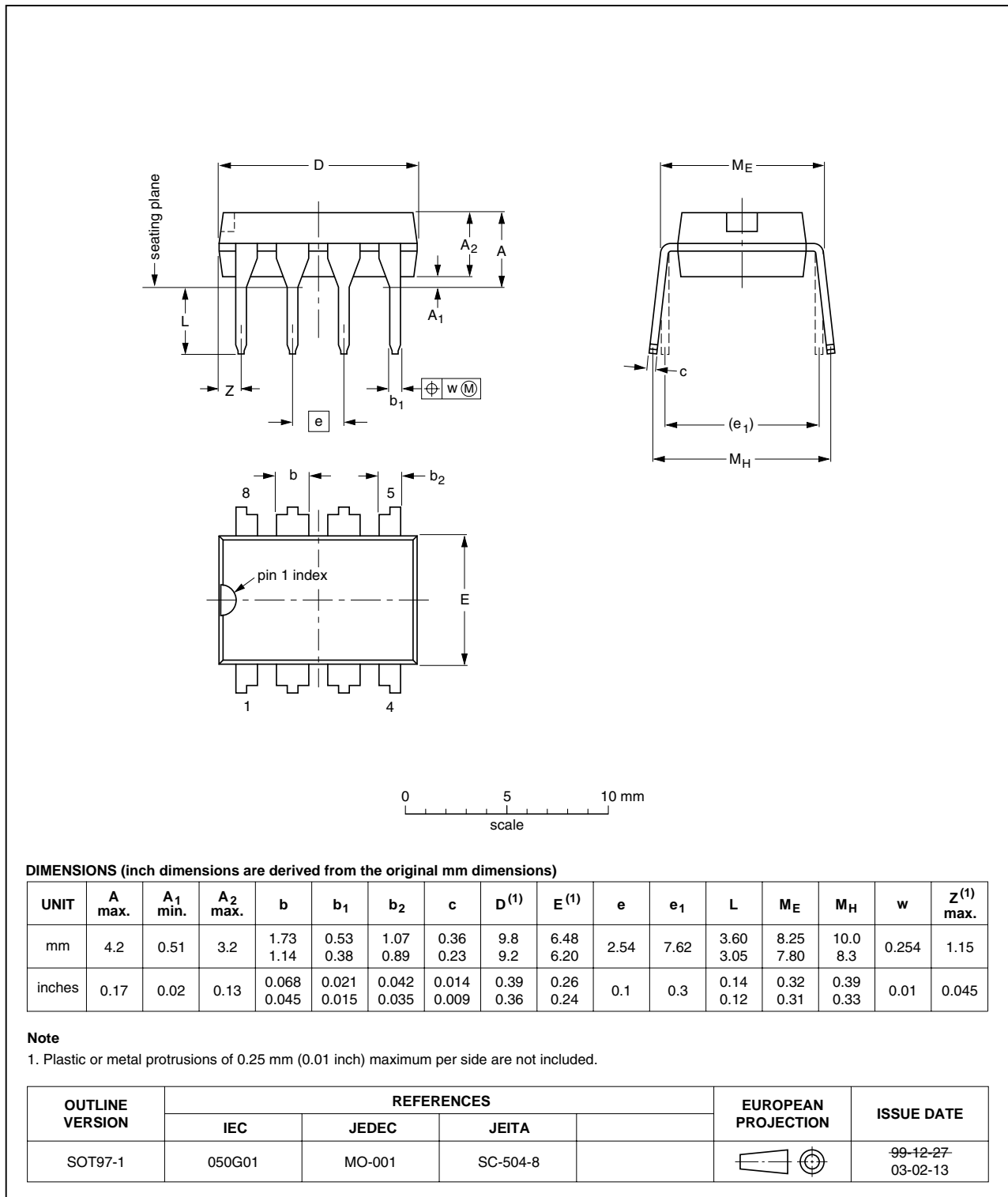


Fig 24. Package outline SOT97-1 (DIP8) of PCF8593P

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

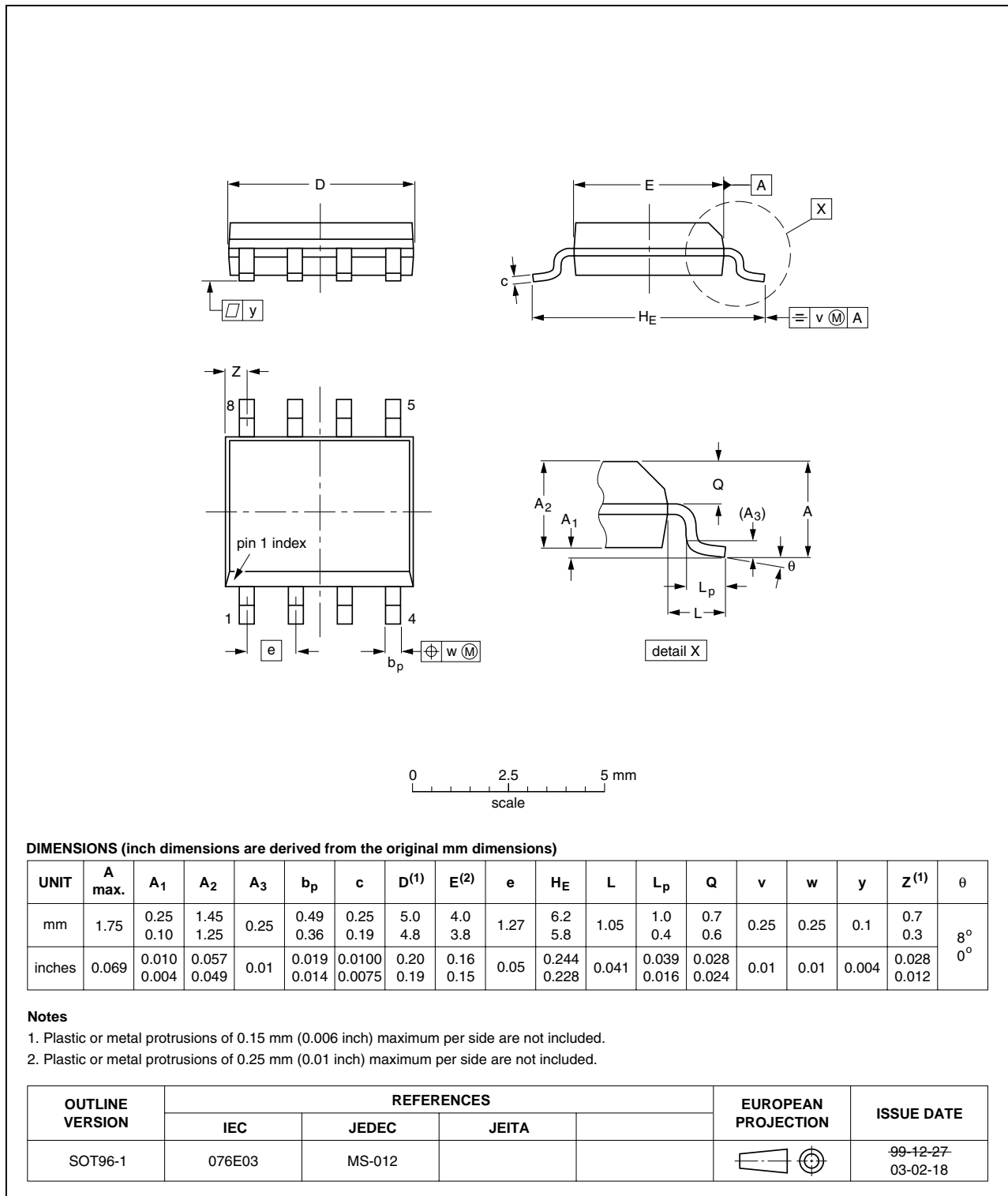


Fig 25. Package outline SOT96-1 (SO8) of PCF8593T

## 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 26](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 9](#) and [10](#)

**Table 9. SnPb eutectic process (from J-STD-020C)**

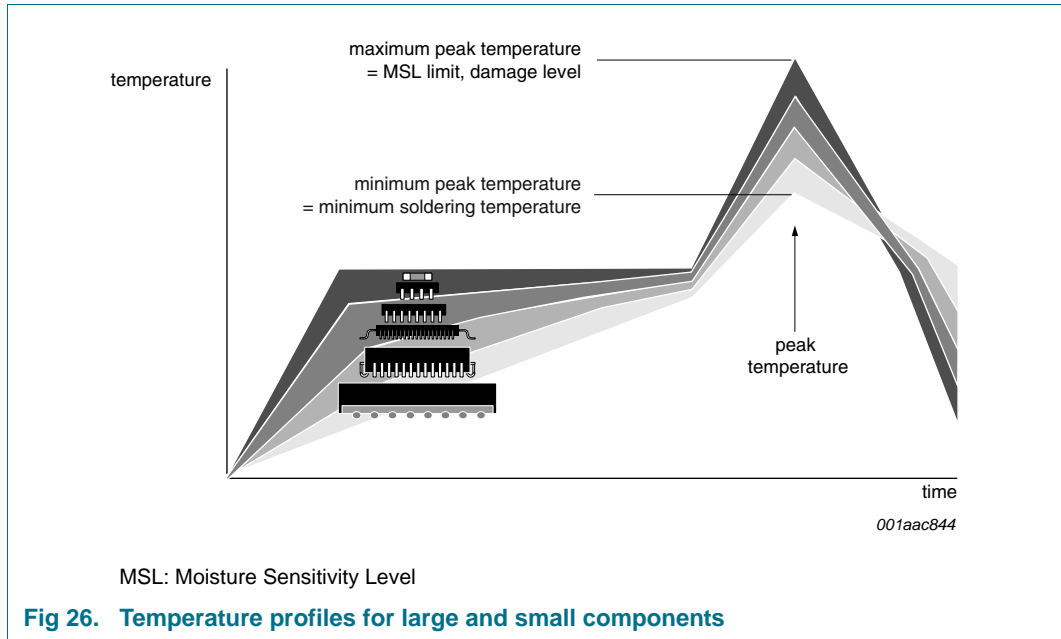
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 10. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 26](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 14. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
PCB	Printed-Circuit Board
PM	Post Meridiem
POR	Power-On Reset
PPM	Parts Per Million
RF	Radio Frequency
RAM	Random Access Memory
SCL	Serial Clock Line
SDA	Serial DATA line
SMD	Surface-Mount Device

## 15. References

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- [1] **AN10365** — Surface mount reflow soldering description
- [2] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [3] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [4] **IPC/JEDEC J-STD-020** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [5] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [6] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [7] **JESD78** — IC Latch-Up Test
- [8] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [9] **NX3-00092** — NXP store and transport requirements
- [10] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [11] **UM10204** — I<sup>2</sup>C-bus specification and user manual

## 16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8593 v.4	20101006	Product data sheet	-	PCF8593_3
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PCF8593_3	19970325	Product specification	-	PCF8593_2
PCF8593_2	19940829	Product specification	-	PCF8593_1
PCF8593_1	19940606	Product specification	-	-



## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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