3.3V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

IDTCSP2510C

FEATURES:

- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes one clock input to one bank of ten outputs**
- **Output enable bank control**
- **External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal**
- **No external RC network required for PLL loop stability**
- **Operates at 3.3V VDD**
- **tpd Phase Error at 133MHz: < ±150ps**
- **Jitter (peak-to-peak) at 133MHz: < ±75ps @ 133MHz**
- **Spread Spectrum Compatible**
- **Operating frequency 25MHz to 140MHz**
- **Available in 24-Pin TSSOP package**

APPLICATIONS:

- **SDRAM Modules**
- **PC Motherboards**
- **Workstations**

DESCRIPTION:

The CSP2510C is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2510C operates at 3.3V.

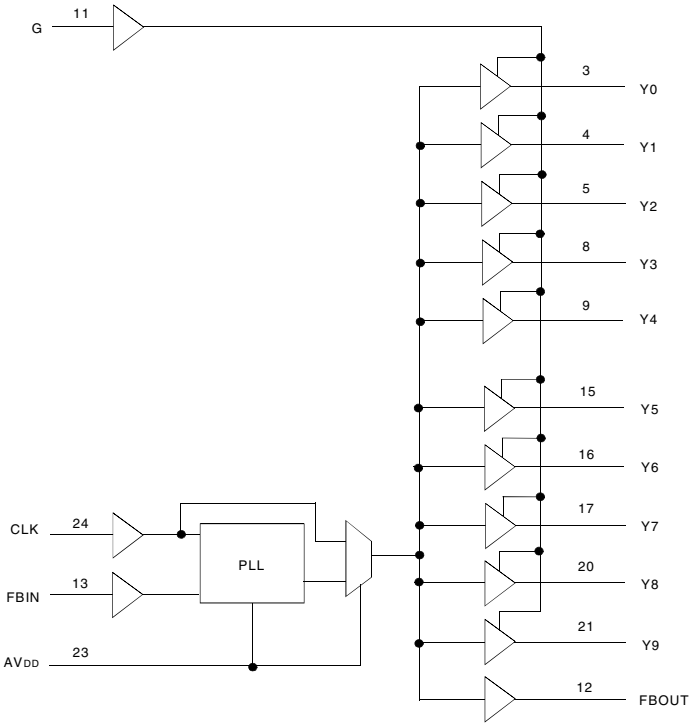
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control G input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2510C does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CSP2510C requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AVDD to ground.

The CSP2510C is specified for operation from 0°C to +85°C. This device is also available (on special order) in Industrial temperature range (-40°C to +85°C). See ordering information for details.

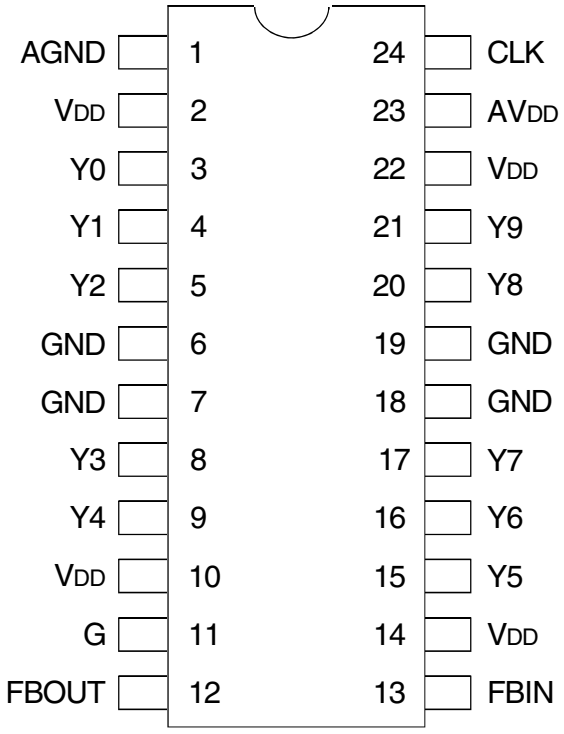
FUNCTIONAL BLOCK DIAGRAM



0ºC TO 85ºC TEMPERATURE RANGE

NOVEMBER 2008

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max	Unit
V_{DD}	Supply Voltage Range	–0.5 to +4.6	V
V_I(1)	Input Voltage Range	–0.5 to +6.5	V
V_O(1,2)	Voltage range applied to any output in the high or low state	–0.5 to V_{DD} + 0.5	V
I_{IK} (V_I <0)	Input clamp current	–50	mA
I_{OK} (V_O <0 or V_O > V_{DD})	Terminal Voltage with Respect to GND (inputs V_{IH} 2.5, V_{IL} 2.5)	±50	mA
I_O (V_O = 0 to V_{DD})	Continuous Output Current	±50	mA
V_{DD} or GND	Continuous Current	±100	mA
T_{STG}	Storage Temperature Range	– 65 to +150	° C
T_J	Junction Temperature	+150	° C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = V_{DD} or GND	——	5	——	pF
C_O	Output Capacitance V_O = V_{DD} or GND	——	6	——	pF
C_L	Load Capacitance	——	30	——	pF

NOTE:
1. Unused inputs must be held HIGH or LOW to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min.	Max.	Unit
V_{DD}, AV_{DD}	Power Supply Voltage	3	3.6	V
T_A	Operating Free-Air Temperature	0	+85	°C

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CSP2510C clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by de-asserting the G control input.
AV_{DD}	23	Power	Analog power supply. AV_{DD} provides the power reference for the analog circuitry. In addition, AV_{DD} can be used to bypass the PLL for test purposes. When AV_{DD} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{DD}	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

STATIC FUNCTION TABLE (AV_{DD} = 0V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
L	L	L	L
L	H	L	H
H	H	H	H
H	L	L	L
H	running	running	running

DYNAMIC FUNCTION TABLE (AV_{DD} = 3.3V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
X	L	L	L
L	running	L	running in phase with CLK
L	H	L	H
H	running	running in phase with CLK	running in phase with CLK
H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE(1)

Symbol	Description	Test Conditions	VDD	Min.	Typ.(2)	Max.	Unit
VIK	Input Clamp Voltage	II = -18mA	3V	—	—	–1.2	V
VIH	Input HIGH Level		—	2	—	—	V
VIL	Input LOW Level		—	—	—	0.8	V
VOH	HIGH Level Output Voltage	IOH = -100µA	Min. to Max.	VDD – 0.2	—	—	V
		IOH = -12mA	3V	2.1	—	—	
		IOH = -6mA	3V	2.4	—	—	
VOL	LOW Level Output Voltage	IOL = 100µA	Min. to Max.	—	—	0.2	V
		IOL = 12mA	3V	—	—	0.8	
		IOL = 6mA	3V	—	—	0.55	
II	Input Current	VI = VDD or GND	3.6V	—	—	±5	µA
IDD	Supply Current	VI = VDD or GND, AVDD = GND, IO = 0, Outputs: LOW or HIGH	3.6V	—	—	10	µA
ΔIDD	Change in Supply Current	One input at VDD - 0.6V, other inputs at VDD or GND	3.3V to 3.6V	—	—	500	µA
CPD	Power Dissipation Capacitance		3.6V	—	10	14	pF
IDDA(3)	AVDD Power Supply Current		AVDD = 3.3V	—	10	—	mA

NOTES:
1. For Industrial devices, operating free-air temperature = -40°C to +85°C.
2. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
3. For IDD of AVDD, see TYPICAL CHARACTERISTICS.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE(1)

		Min.	Max.	Unit
fCLOCK	Clock frequency	25	140	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time(2)	—	1	ms

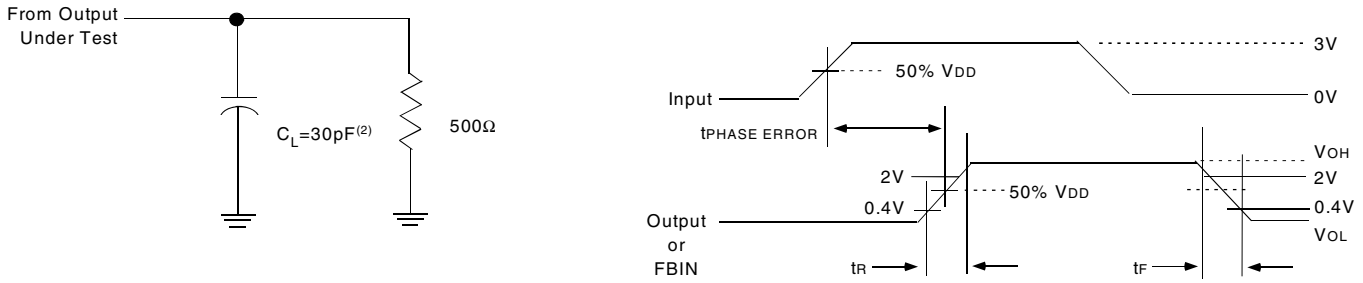
NOTES:
1. For Industrial devices, operating free-air temperature = -40°C to +85°C.
2. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF(1)

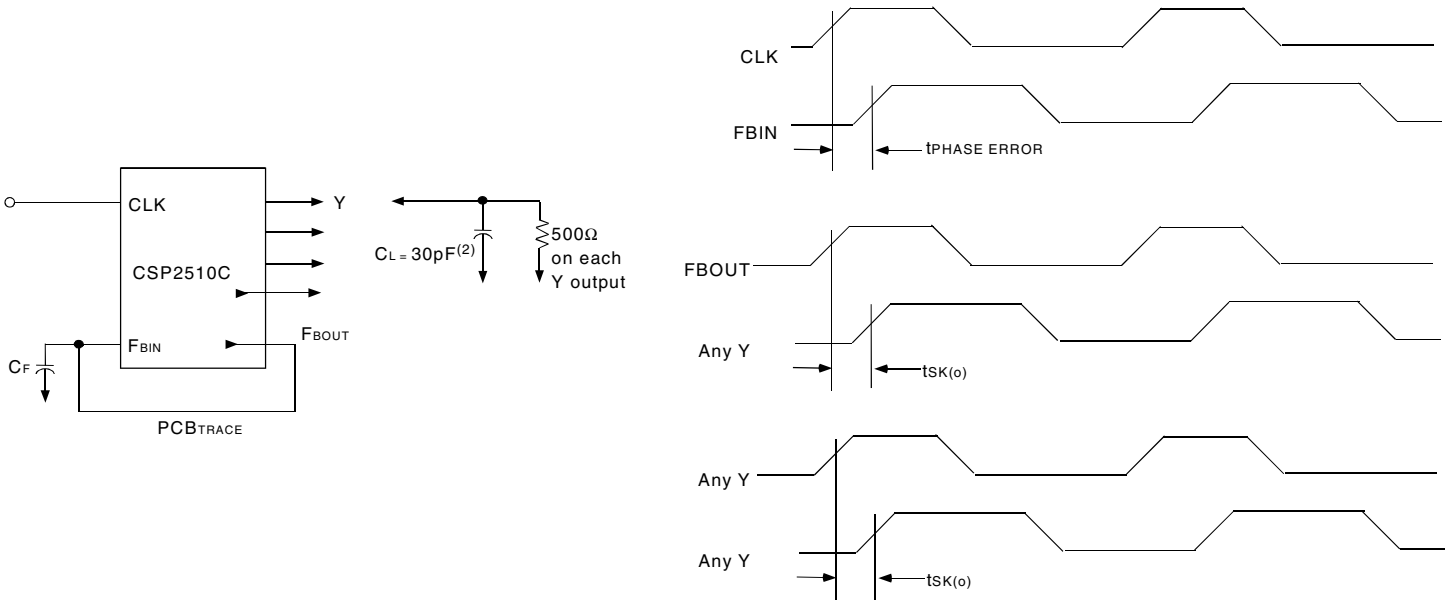
Parameter (2)	From (Input)	To (Output)	V_{DD} = 3.3V ± 0.3V			Unit
			Min.	Typ.	Max.	
t_{PHASE} error	100MHz < CLK↑ < 133MHz	FBIN↑	–150	—	150	ps
t_{PHASE} error – jitter(3)	CLK↑ = 133MHz	FBIN↑	–50	—	50	ps
$t_{SK(o)}$ (4)	Any Y (133MHz)	Any Y	—	—	150	ps
Jitter (cycle-cycle) (peak-to-peak)	CLK = 133MHz	Any Y or FBOUT	–75	—	75	ps
Duty cycle reference (5)	CLK = 133MHz	Any Y or FBOUT	45	—	55	%
t_R		Any Y or FBOUT	0.8	—	2.1	ns
t_F		Any Y or FBOUT	0.8	—	2.7	ns

NOTES:
1. For Industrial devices, operating free-air temperature = -40°C to +85°C. See PARAMETER MEASUREMENT INFORMATION.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. The $t_{SK(O)}$ specification is only valid for equal loading of all outputs.
5. See TYPICAL CHARACTERISTICS.

PARAMETER MEASUREMENT INFORMATION(1)



Load Circuit and Voltage Waveforms



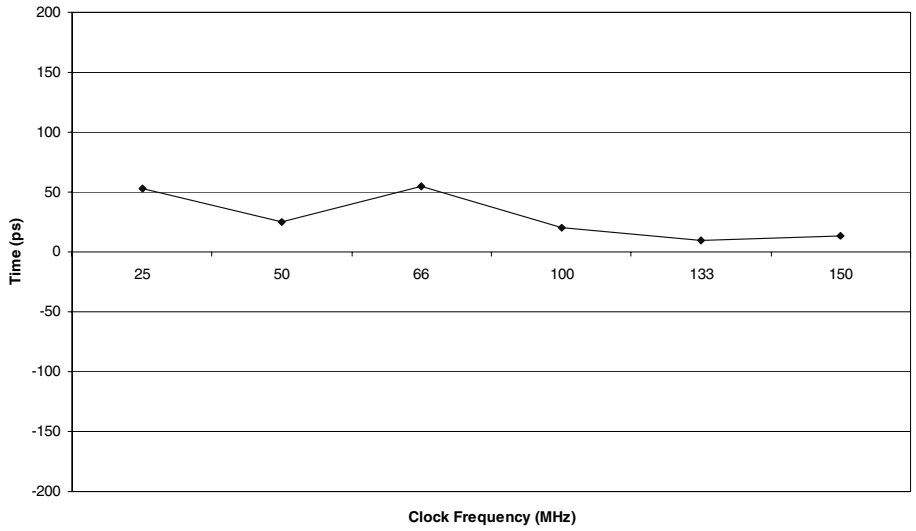
Phase ERROR and Skew Calculations (3,4)

NOTES:

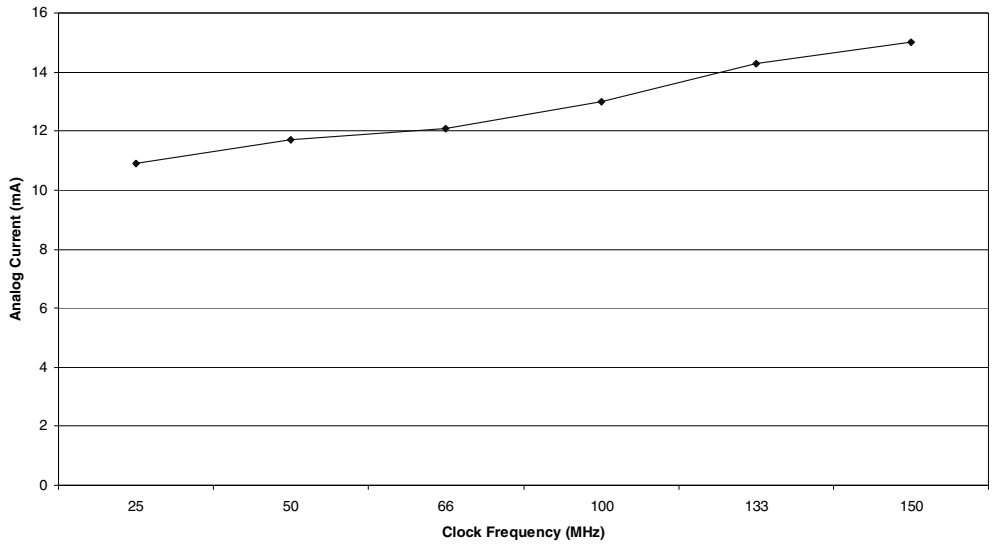
1. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz ZO = 50Ω, tR ≤ 1.2 ns, tF≤ 1.2 ns.
2. CL includes probe and jig capacitance.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. CF = CL – CFBIN – CPCBTRACE; CFBIN ≅ 6pF.

TYPICAL CHARACTERISTICS

Phase Error vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C

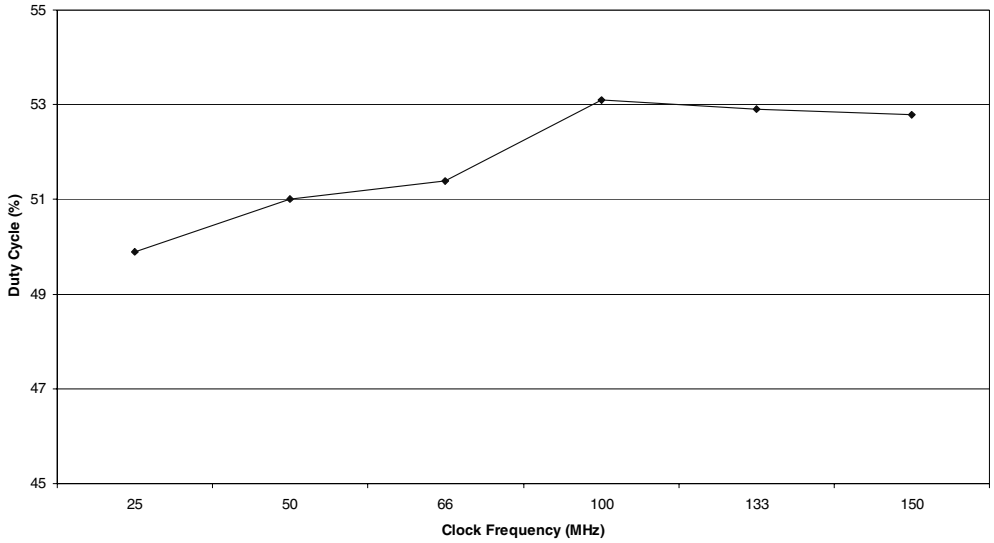


Analog Supply Current vs. Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C

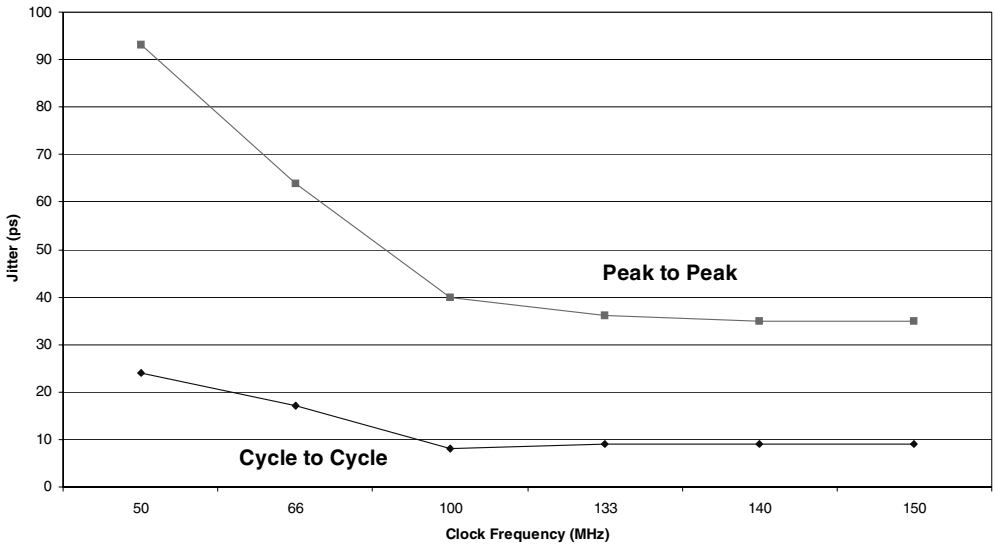


TYPICAL CHARACTERISTICS (CONT.)

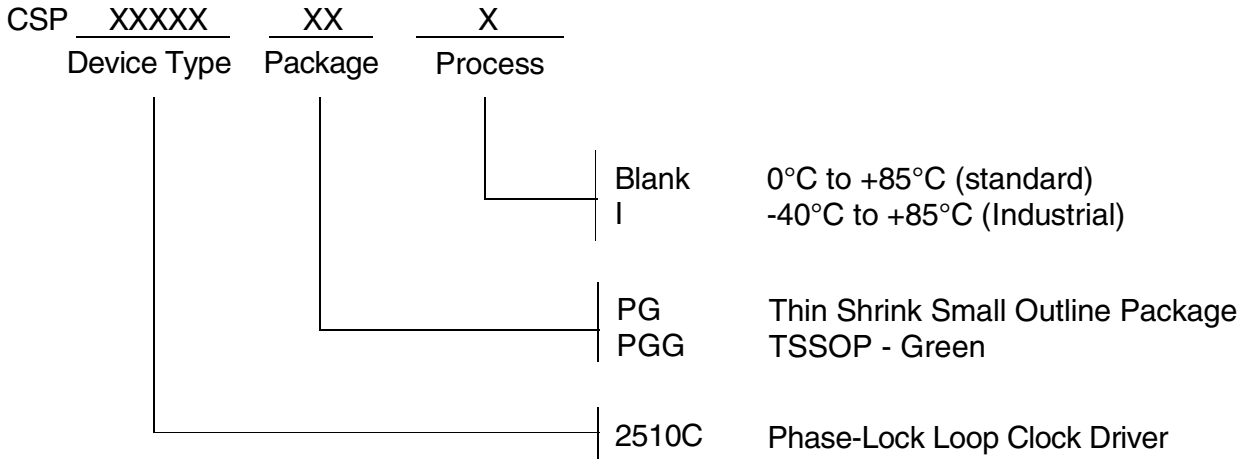
Output Duty Cycle vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C



Jitter vs Clock Frequency
Avcc and Vcc = 3.3V
Ta = 25C



ORDERING INFORMATION



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