

# PCA9557 Remote 8-Bit I<sup>2</sup>C and SMBus Low-Power I/O Expander With Reset and Configuration Registers

## 1 Features

- Low Standby Current Consumption of 1  $\mu$ A Max
- I<sup>2</sup>C to Parallel Port Expander
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I<sup>2</sup>C Bus
- Three Hardware Address Pins Allow for Use of up to Eight Devices on I<sup>2</sup>C/SMBus
- Lower-Voltage Higher-Performance Migration Path for PCA9556
- Input/Output Configuration Register
- Polarity Inversion Register
- Active-Low Reset Input
- Internal Power-On Reset
- High-Impedance Open Drain on P0
- Power Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Description

This 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.3-V to 5.5-V V<sub>CC</sub> operation. The device provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL) and serial data (SDA)].

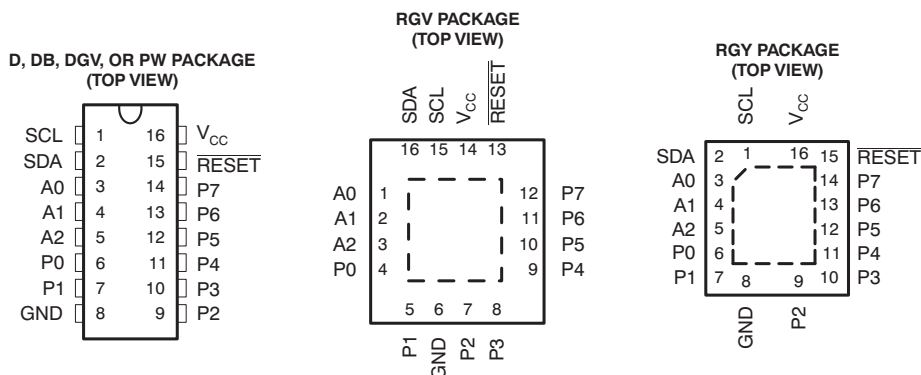
The PCA9557 consists of one 8-bit configuration (input or output selection), input port, output port, and polarity inversion (active-high) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9557	SSOP (16)	6.20 mm x 5.30 mm
	VQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Description</b> ..... 1 <b>3 Revision History</b> ..... 2 <b>4 Description (Continued)</b> ..... 3 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 4 6.1 Absolute Maximum Ratings ..... 4 6.2 Handling Ratings ..... 4 6.3 Recommended Operating Conditions ..... 4 6.4 Electrical Characteristics ..... 5 6.5 I <sup>2</sup> C Interface Timing Requirements..... 6 6.6 Reset Timing Requirements ..... 6 6.7 Switching Characteristics ..... 6 6.8 Typical Characteristics ..... 7 <b>7 Parameter Measurement Information</b> ..... 9	<b>8 Detailed Description</b> ..... 12 8.1 Functional Block Diagram ..... 12 8.2 Device Functional Modes..... 14 8.3 Programming..... 15 8.4 Bus Transactions ..... 19 <b>9 Application And Implementation</b> ..... 21 9.1 Application Information..... 21 9.2 Typical Application ..... 21 <b>10 Power Supply Recommendations</b> ..... 22 10.1 Power-On Reset Errata..... 22 <b>11 Device and Documentation Support</b> ..... 23 11.1 Trademarks ..... 23 11.2 Electrostatic Discharge Caution..... 23 11.3 Glossary ..... 23 <b>12 Mechanical, Packaging, and Orderable Information</b> ..... 23
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### 3 Revision History

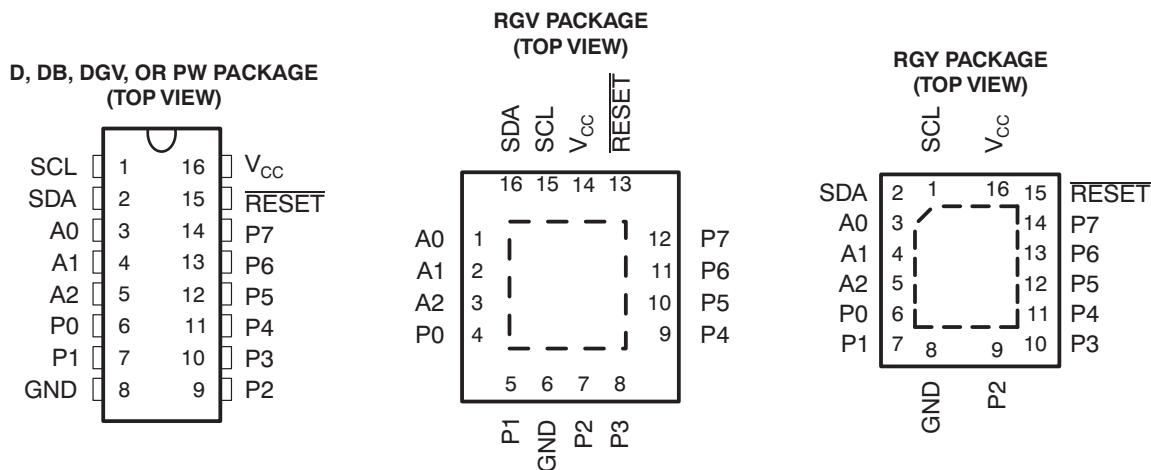
Changes from Revision I (June 2008) to Revision J	Page
• Added $\overline{\text{RESET}}$ Errata section. ....	14
• Added Power-On Reset Errata section. ....	22

## 4 Description (Continued)

The system master can reset the PCA9557 in the event of a timeout or other improper operation by asserting a low in the active-low reset ( $\overline{\text{RESET}}$ ) input. The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine. Asserting  $\overline{\text{RESET}}$  causes the same reset/initialization to occur without depowering the part.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address, allowing up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		DESCRIPTION
	QFN (RGY) SOIC (D), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGV)	
SCL	1	15	Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor.
SDA	2	16	Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor.
A0	3	1	Address input. Connect directly to V <sub>CC</sub> or ground.
A1	4	2	Address input. Connect directly to V <sub>CC</sub> or ground.
A2	5	3	Address input. Connect directly to V <sub>CC</sub> or ground.
P0	6	4	P-port input/output. High impedance open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor.
P1	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P2	9	7	P-port input/output. Push-pull design structure.
P3	10	8	P-port input/output. Push-pull design structure.
P4	11	9	P-port input/output. Push-pull design structure.
P5	12	10	P-port input/output. Push-pull design structure.
P6	13	11	P-port input/output. Push-pull design structure.
P7	14	12	P-port input/output. Push-pull design structure.
$\overline{\text{RESET}}$	15	13	Active-low reset input. Connect to V <sub>CC</sub> through a pullup resistor if no active connection is used.
V <sub>CC</sub>	16	14	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-20	mA
I <sub>I<sub>OK</sub></sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	-20	μA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-50	mA
I <sub>CC</sub>	Continuous current through GND		-250	mA
	Continuous current through V <sub>CC</sub>		160	
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	D package	73	°C/W
		DB package	82	
		DGV package	120	
		PW package	108	
		RGV package	51	
		RGY package	47	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### 6.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	2.3	5.5	V	
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	5.5	V
		A2–A0, P7–P0, $\overline{\text{RESET}}$	2	5.5	
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>	V
		A2–A0, P7–P0, $\overline{\text{RESET}}$	-0.5	0.8	
I <sub>OH</sub>	High-level output current	P7–P1	-10	mA	
I <sub>OL</sub>	Low-level output current	P7–P0	25	mA	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.3 V to 5.5 V	-1.2			V	
V <sub>POR</sub>	Power-on reset voltage	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	V <sub>POR</sub>		1.65	2.1	V	
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = -8 mA	2.3 V		1.8		V	
			3 V		2.6			
			4.5 V		3			
			4.75 V		4.1			
		I <sub>OH</sub> = -10 mA	2.3 V		1.5			
			3 V		2.5			
			4.5 V		3			
			4.75 V		4			
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	2.3 V to 5.5 V		3		mA	
	P port <sup>(3)</sup>	V <sub>OL</sub> = 0.5 V	2.3 V to 5.5 V		8	20		
		V <sub>OL</sub> = 0.55 V			8	20		
		V <sub>OL</sub> = 0.7 V			10	24		
I <sub>OH</sub>	P port, except for P0 <sup>(3)</sup>	V <sub>OH</sub> = 2.3 V	2.3 V to 5.5 V		-4		mA	
	P0 <sup>(3)</sup>	V <sub>OH</sub> = 4.6 V	4.6 V to 5.5 V			1	μA	
		V <sub>OH</sub> = 3.3 V	3.3 V to 5.5 V			1		
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V			±1	μA	
	A2-A0, RESET					±1		
I <sub>IH</sub>	P port	V <sub>I</sub> = V <sub>CC</sub>	2.3 V to 5.5 V			1	μA	
I <sub>IL</sub>	P port	V <sub>I</sub> = GND	2.3 V to 5.5 V			1	μA	
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz	5.5 V		19	25	μA	
			3.6 V		12	22		
			2.7 V		8	20		
		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 100 kHz	5.5 V		1.5	5		
			3.6 V		1	4		
			2.7 V		0.6	3		
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz	5.5 V		0.25	1		
			3.6 V		0.25	0.9		
2.7 V				0.2	0.8			
ΔI <sub>CC</sub>	Additional current in Standby mode	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.3 V to 5.5 V			0.2	mA	
		Every LED I/O at V <sub>I</sub> = 4.3 V, f <sub>SCL</sub> = 0 kHz	5.5 V			0.4		
C <sub>I</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		4	6	pF	
C <sub>IO</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		5.5	8	pF	
	P port				7.5	9.5		

 (1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) The total current sourced by all I/Os must be limited to 85 mA per bit.

(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7-P0) must be limited to a maximum current of 200 mA.

## 6.5 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 13](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
$f_{scl}$	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
$t_{sch}$	I <sup>2</sup> C clock high time	4		0.6		μs
$t_{scl}$	I <sup>2</sup> C clock low time	4.7		1.3		μs
$t_{sp}$	I <sup>2</sup> C spike time		50		50	ns
$t_{sds}$	I <sup>2</sup> C serial data setup time	250		100		ns
$t_{sdh}$	I <sup>2</sup> C serial data hold time	0		0		ns
$t_{icr}$	I <sup>2</sup> C input rise time		1000	$20 + 0.1C_b^{(1)}$	300	ns
$t_{icf}$	I <sup>2</sup> C input fall time		300	$20 + 0.1C_b^{(1)}$	300	ns
$t_{ocf}$	I <sup>2</sup> C output fall time, 10-pF to 400-pF bus		300	$20 + 0.1C_b^{(1)}$	300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between Stop and Start	4.7		1.3		μs
$t_{sts}$	I <sup>2</sup> C Start or repeated Start condition setup time	4.7		0.6		μs
$t_{sth}$	I <sup>2</sup> C Start or repeated Start condition hold time	4		0.6		μs
$t_{sps}$	I <sup>2</sup> C Stop condition setup time	4		0.6		μs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		1		0.9	μs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		0.9	μs
$C_b$	I <sup>2</sup> C bus capacitive load		400		400	pF

(1)  $C_b$  = total capacitance of one bus line in pF

## 6.6 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 15](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
$t_W$	Reset pulse duration <sup>(1)</sup>	16		16		ns
$t_{REC}$	Reset recovery time	0		0		ns
$t_{RESET}$	Time to reset <sup>(2)</sup>	400		400		ns

(1) A pulse duration of 16 ns minimum must be applied to  $\overline{RESET}$  to return the PCA9557 to its default state.

(2) The PCA9557 requires a minimum of 400 ns to be reset.

## 6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 13](#))

PARAMETER	FROM	TO	STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
			MIN	MAX	MIN	MAX	
$t_{pv}$ Output data valid	SCL	P0		250		250	ns
	SCL	P1–P7		200		200	
$t_{ps}$ Input data setup time	P port	SCL	0		0		ns
$t_{ph}$ Input data hold time	P port	SCL	200		200		ns

### 6.8 Typical Characteristics

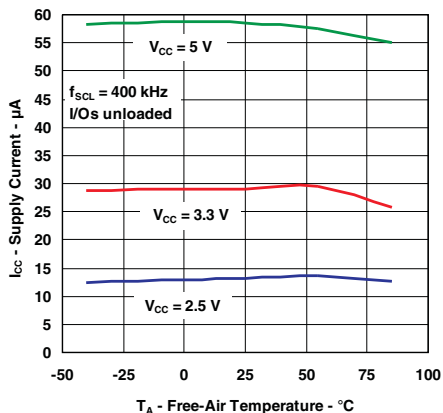


Figure 1. Supply Current vs Temperature

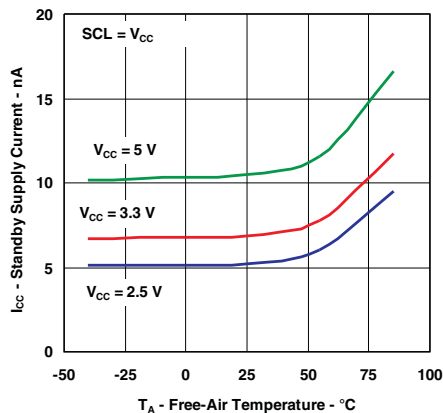


Figure 2. Standby Supply Current vs Temperature

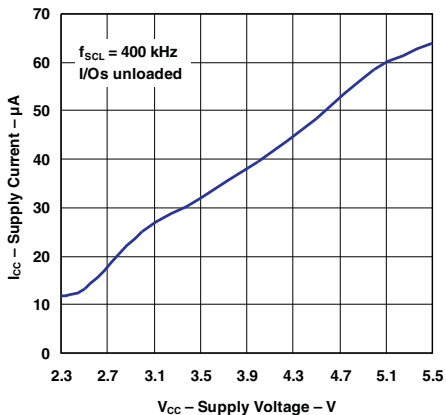


Figure 3. Supply Current vs Supply Voltage

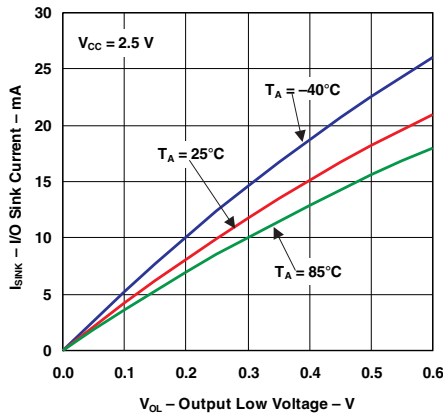


Figure 4. I/O Sink Current vs Output Low Voltage

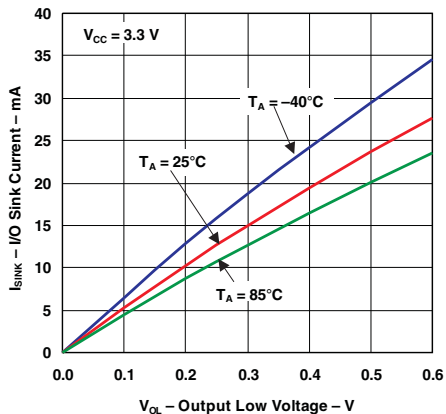


Figure 5. I/O Sink Current vs Output Low Voltage

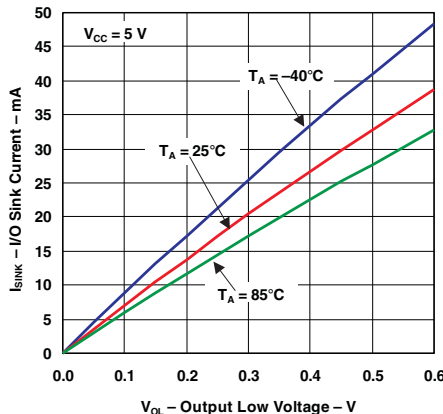


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

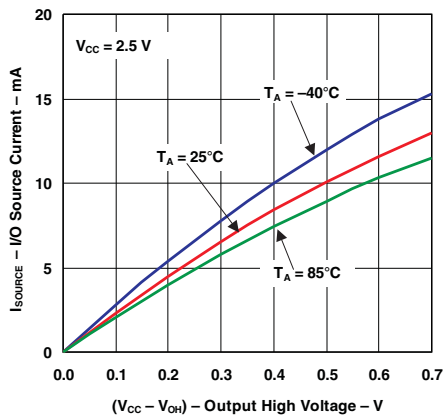


Figure 7. I/O Source Current vs Output High Voltage (P7-P1)

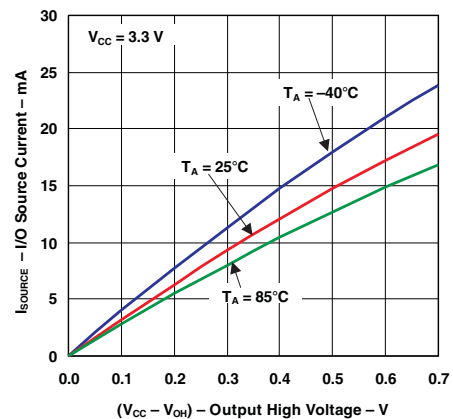


Figure 8. I/O Source Current vs Output High Voltage (P7-P1)

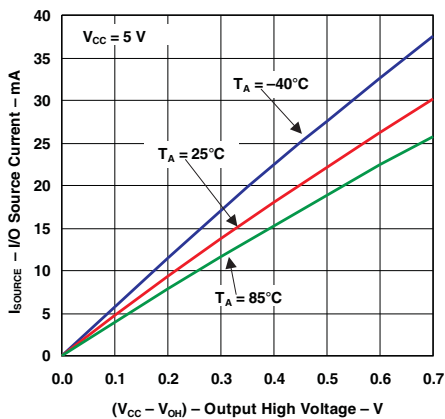


Figure 9. I/O Source Current vs Output High Voltage (P7-P1)

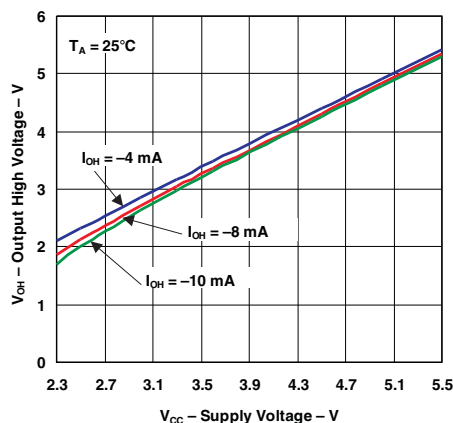


Figure 10. Output High Voltage vs Supply Voltage (P7-P1)

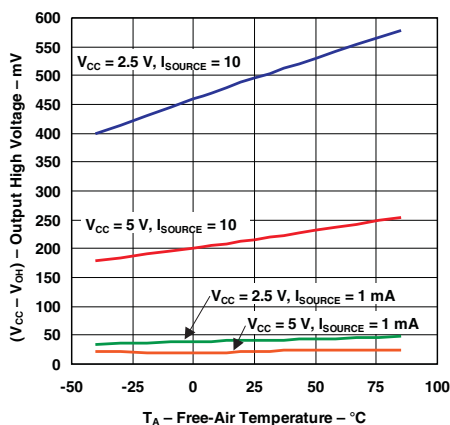


Figure 11. Output High Voltage vs Temperature (P7-P1)

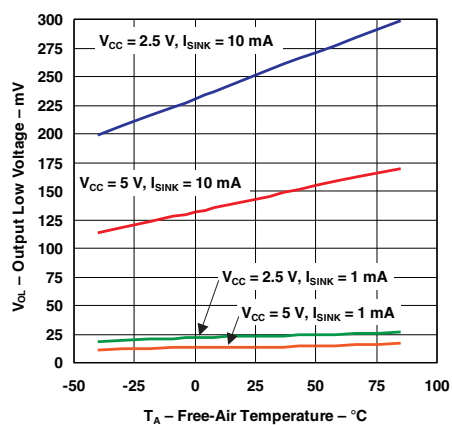
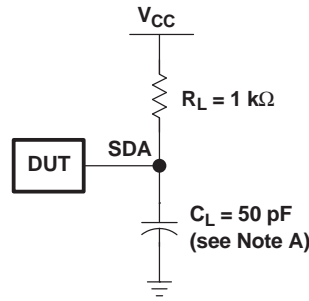


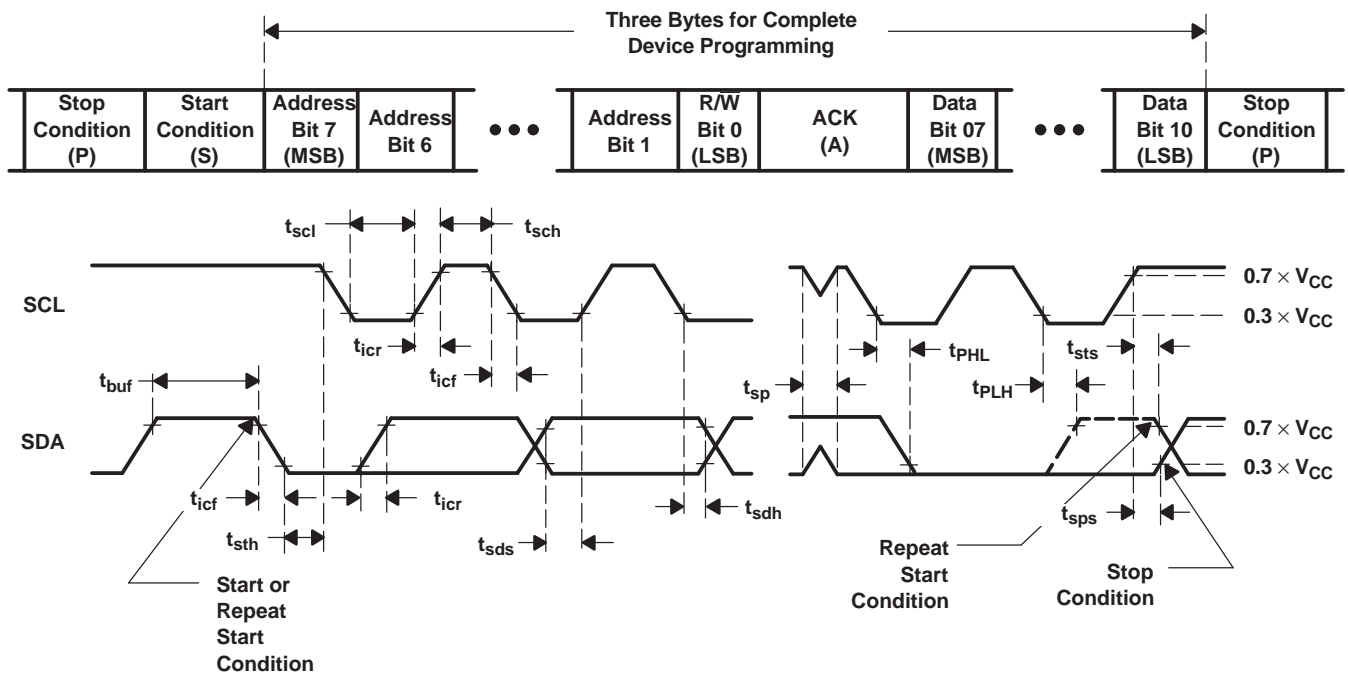
Figure 12. Output Low Voltage vs Temperature



## 7 Parameter Measurement Information



SDA LOAD CONFIGURATION

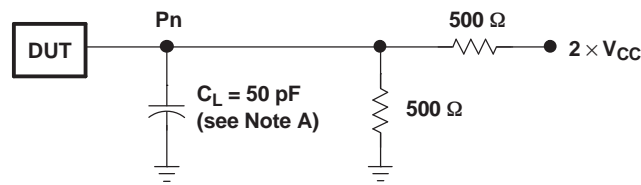
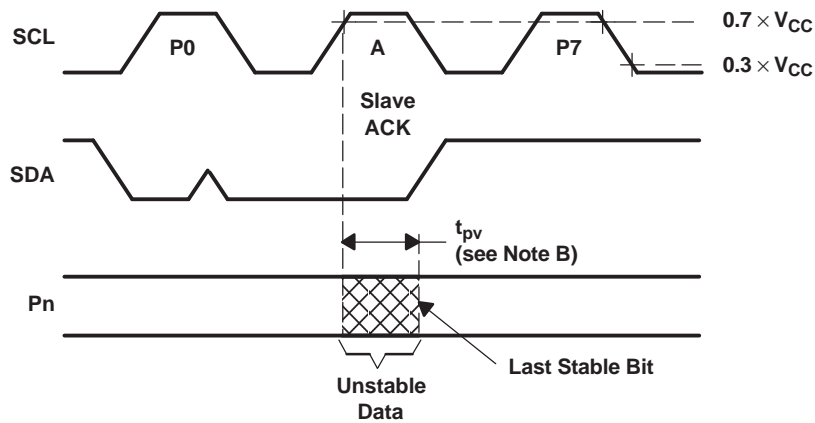
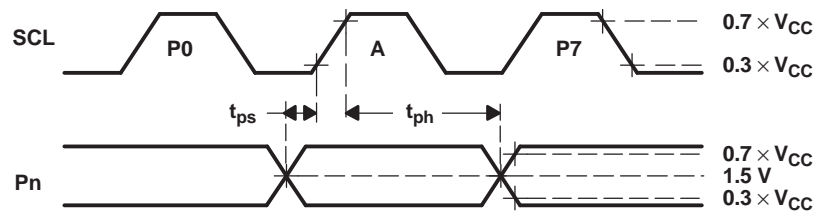


VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

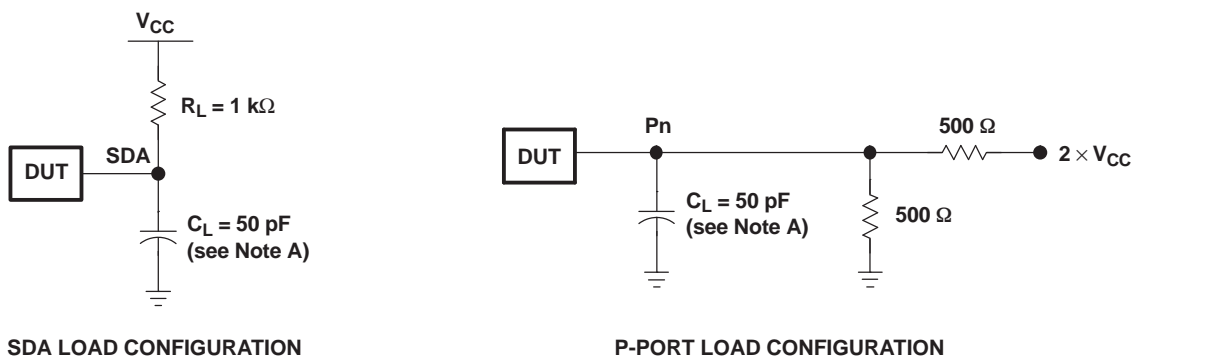
Figure 13. I<sup>2</sup>C Interface Load Circuit And Voltage Waveforms

**Parameter Measurement Information (continued)**

**P-PORT LOAD CONFIGURATION**

**WRITE MODE ( $R/\bar{W} = 0$ )**

**READ MODE ( $R/\bar{W} = 1$ )**

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

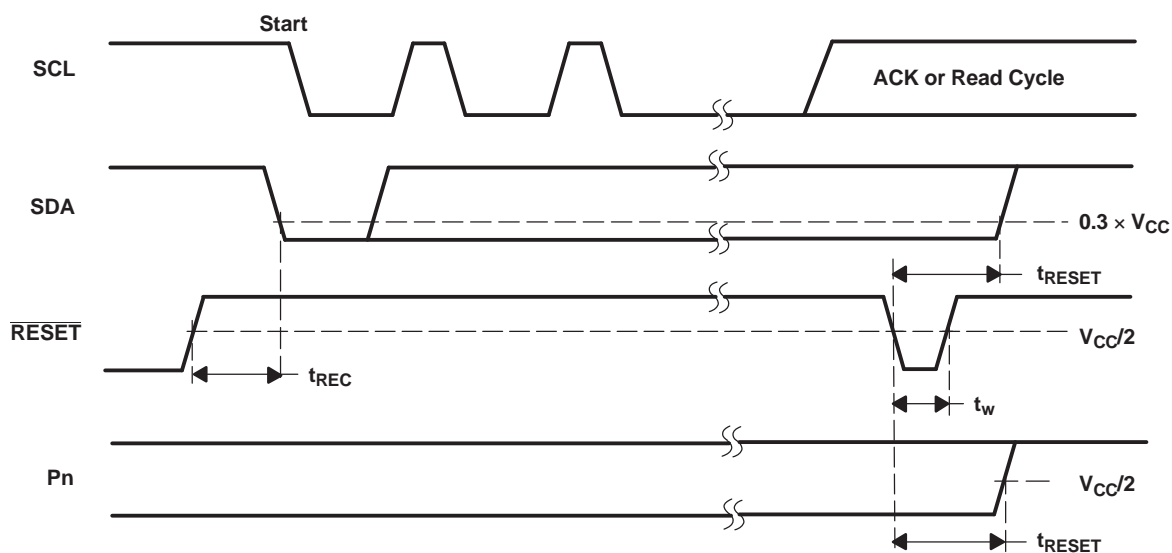
**Figure 14. P-Port Load Circuit And Voltage Waveforms**

Parameter Measurement Information (continued)



SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION

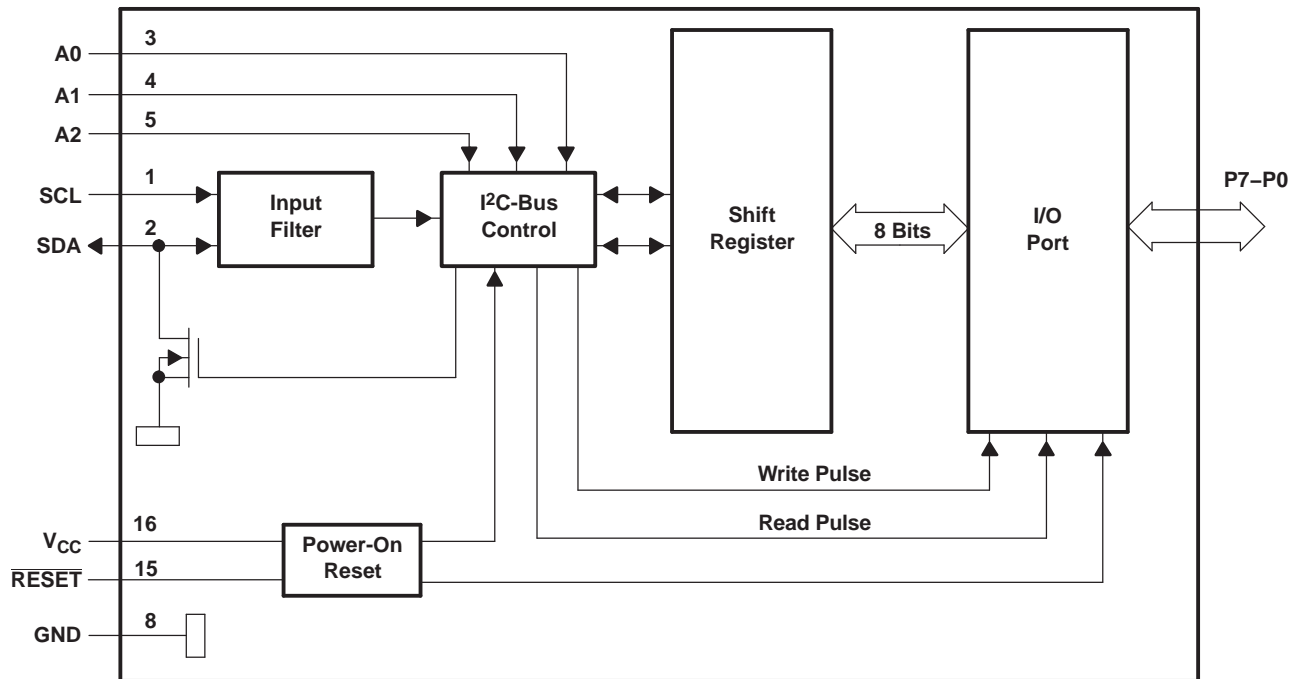


- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- C. I/Os are configured as inputs.
- D. All parameters and waveforms are not applicable to all devices.

Figure 15. Reset Load Circuits And Voltage Waveforms

## 8 Detailed Description

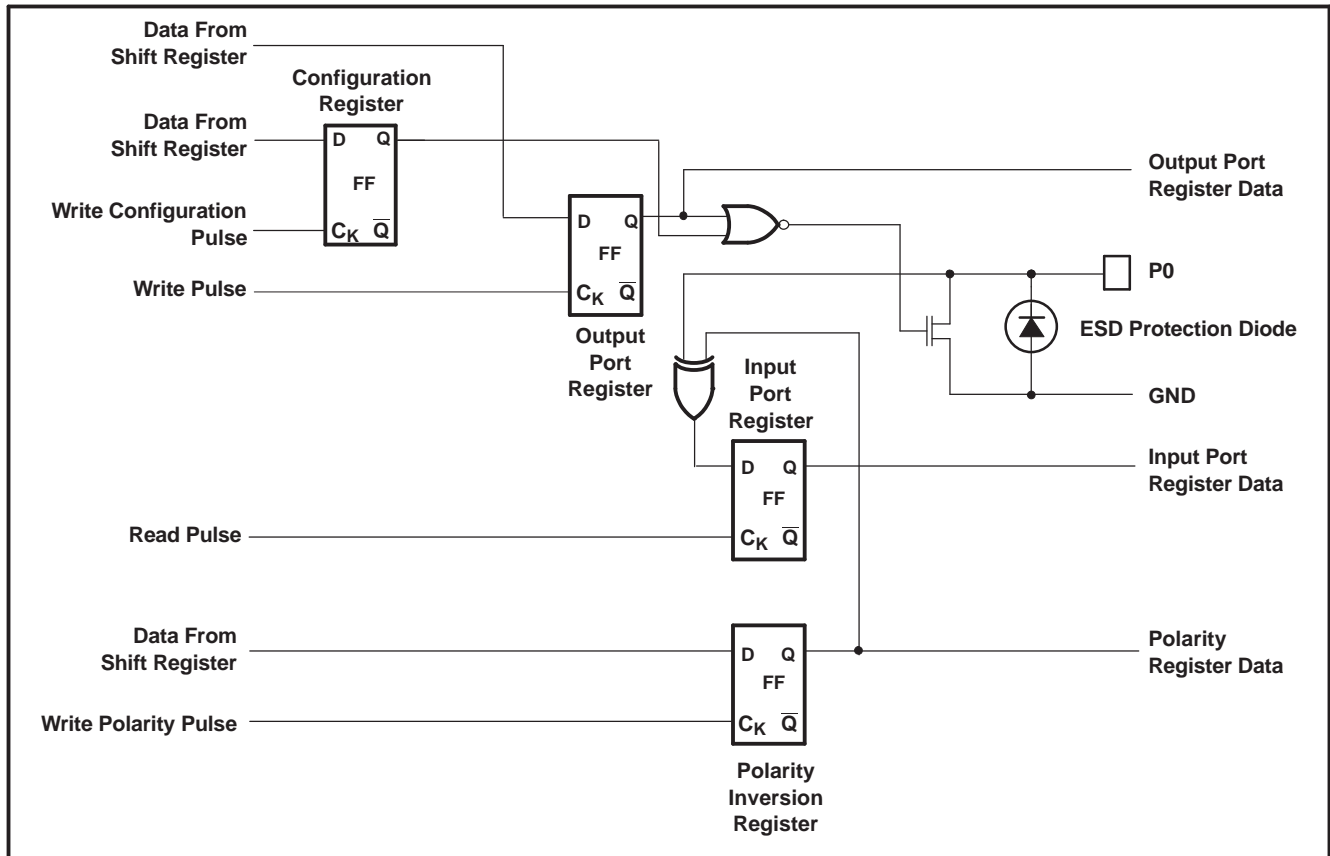
### 8.1 Functional Block Diagram



- A. Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.
- B. All I/Os are set to inputs at reset.

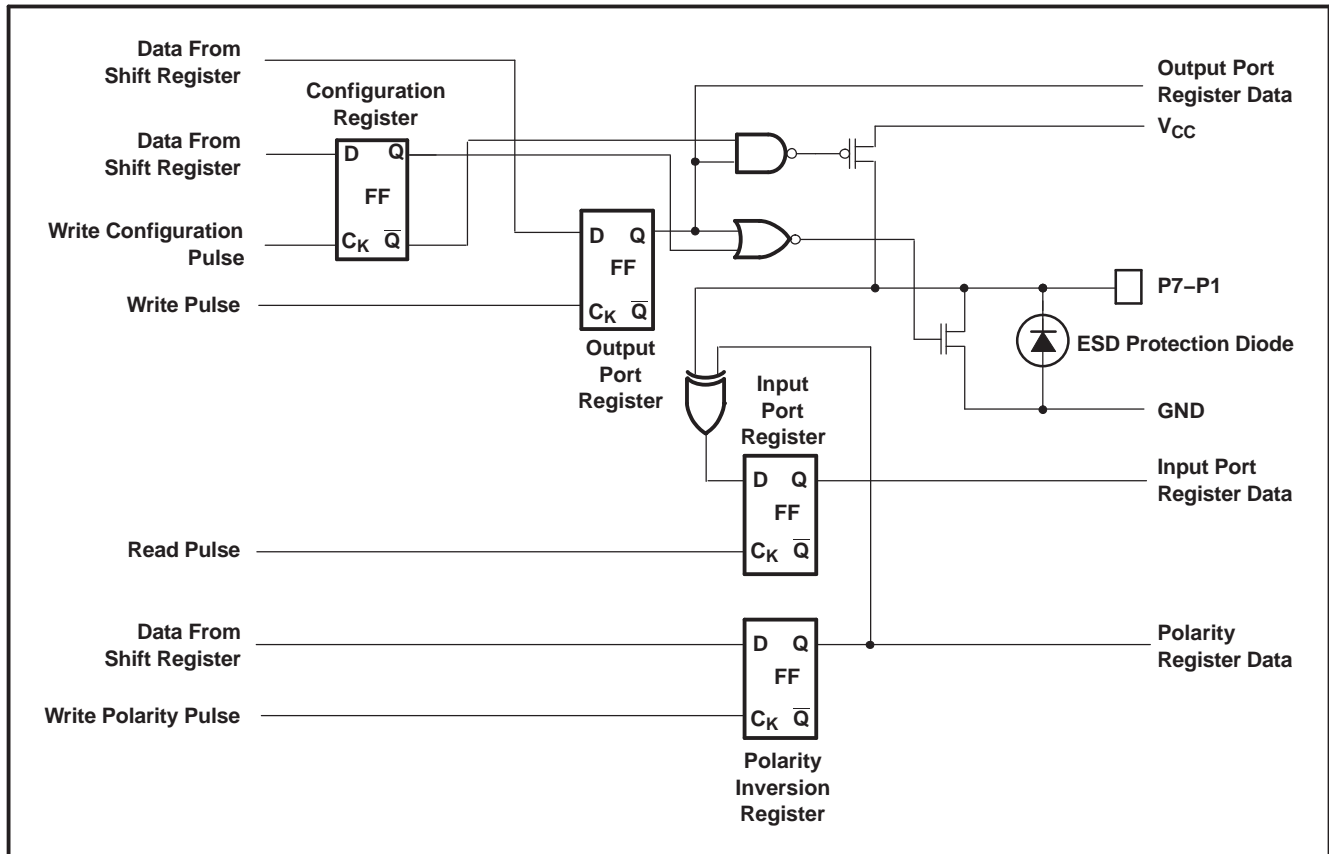
**Figure 16. Logic Diagram (Positive Logic)**

Functional Block Diagram (continued)



A. On power up or reset, all registers return to default values.

Figure 17. Simplified Schematic Diagram Of P0

**Functional Block Diagram (continued)**


A. On power up or reset, all registers return to default values.

**Figure 18. Simplified Schematic Diagram Of P7-P1**

## 8.2 Device Functional Modes

### 8.2.1 $\overline{\text{RESET}}$

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin low for a minimum of  $t_{W}$ . The PCA9557 registers and I<sup>2</sup>C/SMBus state machine are held in their default states until  $\overline{\text{RESET}}$  again is high. This input requires a pullup resistor to V<sub>CC</sub> if no active connection is used.

#### 8.2.1.1 $\overline{\text{RESET}}$ Errata

If  $\overline{\text{RESET}}$  voltage set higher than V<sub>CC</sub>, current will flow from  $\overline{\text{RESET}}$  pin to V<sub>CC</sub> pin.

#### System Impact

V<sub>CC</sub> will be pulled above its regular voltage level.

#### System Workaround

Design such that  $\overline{\text{RESET}}$  voltage is same or lower than V<sub>CC</sub>.

## Device Functional Modes (continued)

### 8.2.2 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the PCA9557 in a reset condition until  $V_{CC}$  has reached  $V_{POR}$ . At that time, the reset condition is released, and the PCA9557 registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{CC}$  must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle. The RESET input can be asserted to reset the system, while keeping the  $V_{CC}$  at its operating level.

Refer to the [Power-On Reset Errata](#) section.

## 8.3 Programming

### 8.3.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 19](#)). After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W).

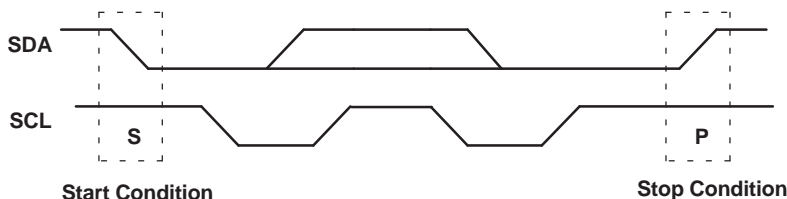
After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (A2–A0) inputs of the slave device must not be changed between the start and the stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see [Figure 20](#)).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 19](#)).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 21](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.



**Figure 19. Definition Of Start And Stop Conditions**

### Programming (continued)

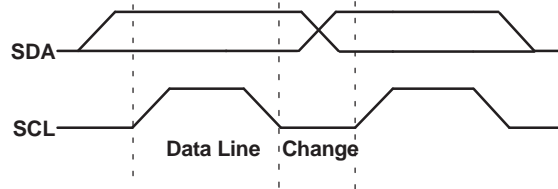


Figure 20. Bit Transfer

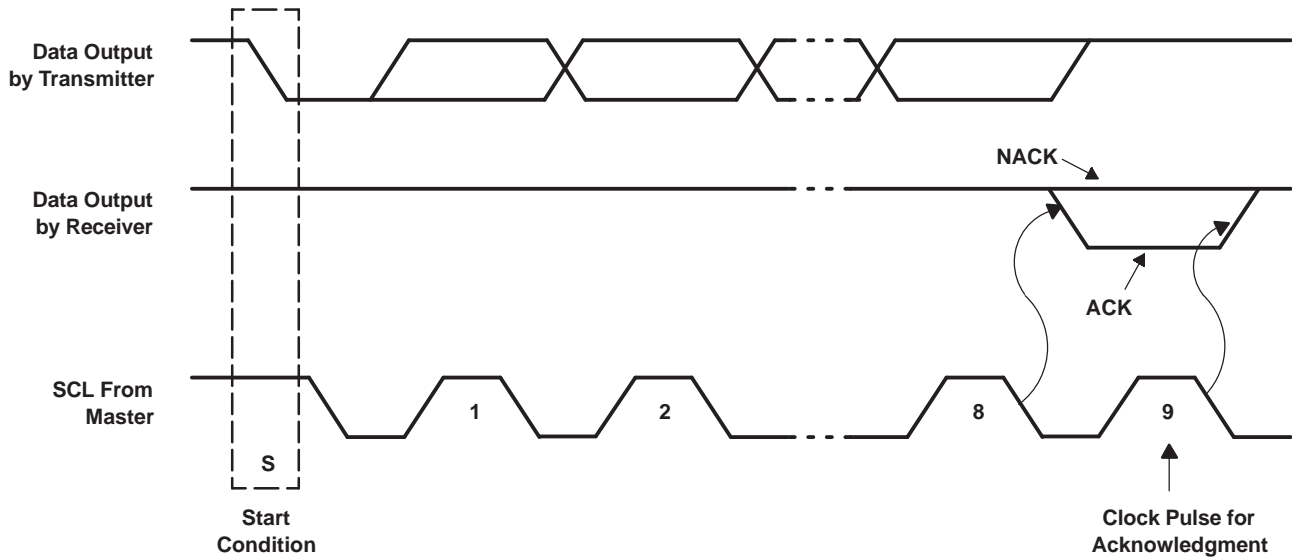


Figure 21. Acknowledgment On The I<sup>2</sup>C Bus

### 8.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	L	H	H	A2	A1	A0	R/W
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

#### 8.3.2.1 Device Address

The address of the PCA9557 is shown in [Figure 22](#).

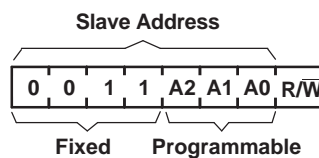


Figure 22. Pca9557 Address



**Table 2. Address Reference**

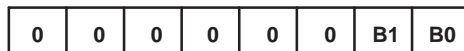
INPUTS			I <sup>2</sup> C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	24 (decimal), 18 (hexadecimal)
L	L	H	25 (decimal), 19 (hexadecimal)
L	H	L	26 (decimal), 1A (hexadecimal)
L	H	H	27 (decimal), 1B (hexadecimal)
H	L	L	28 (decimal), 1C (hexadecimal)
H	L	H	29 (decimal), 1D (hexadecimal)
H	H	L	30 (decimal), 1E (hexadecimal)
H	H	H	31 (decimal), 1F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

### 8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9557. Two bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a new command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.


**Figure 23. Control Register Bits**
**Table 3. Command Byte**

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	0000 0000
1	0	0x02	Polarity Inversion	Read/write byte	1111 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

### 8.3.2.3 Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to signal the I<sup>2</sup>C device that the input port register will be accessed next.

**Table 4. Register 0 (Input Port Register)**

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 5. Register 1 (Output Port Register)**

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	0	0	0	0	0	0	0	0

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

**Table 6. Register 2 (Polarity Inversion Register)**

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	1	1	1	1	0	0	0	0

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7. Register 3 (Configuration Register)**

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

## 8.4 Bus Transactions

Data is exchanged between the master and PCA9557 through write and read commands.

### 8.4.1 Writes

Data is transmitted to the PCA9557 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see Figure 24 and Figure 25).

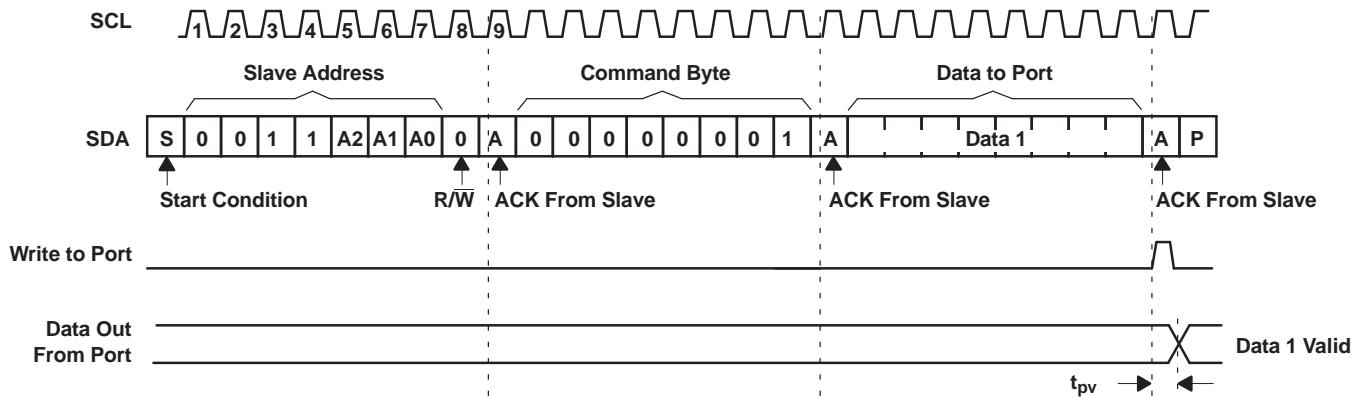


Figure 24. Write To Output Port Register

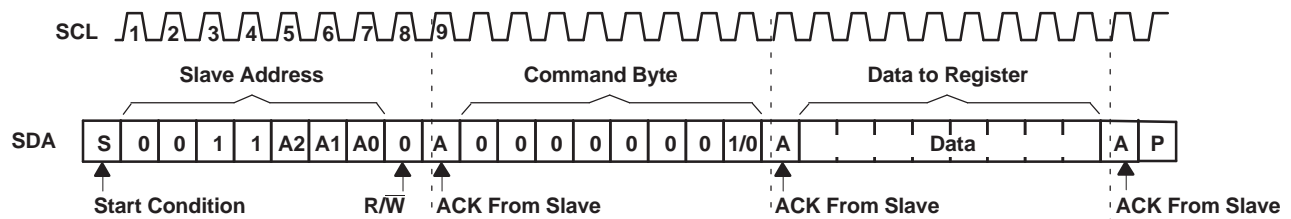
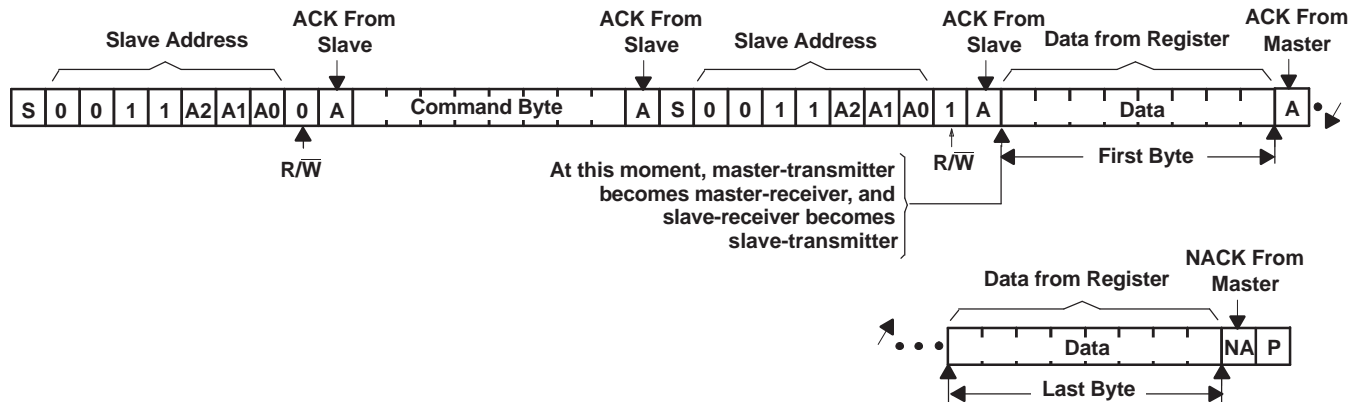


Figure 25. Write To Configuration Or Polarity Inversion Registers

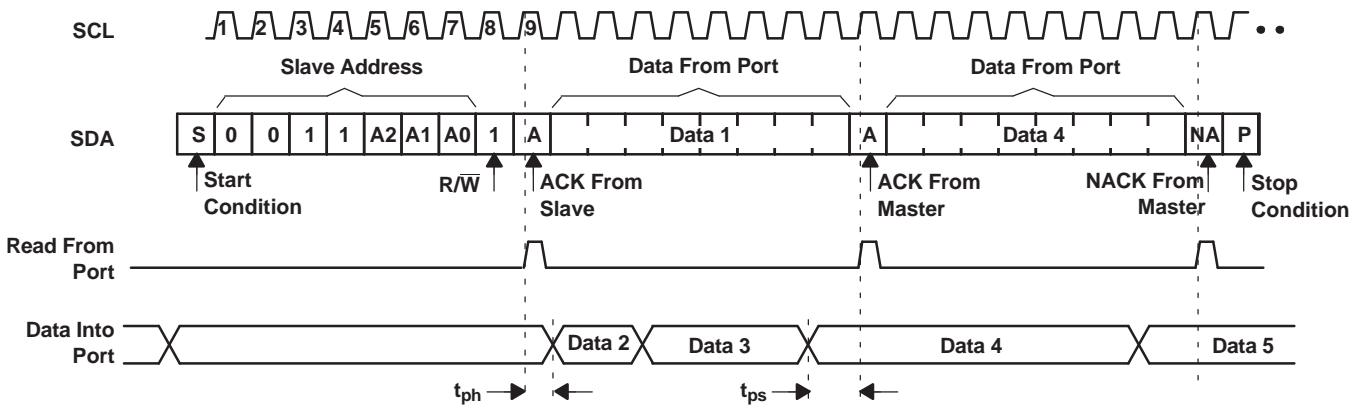
## Bus Transactions (continued)

### 8.4.2 Reads

The bus master first must send the PCA9557 address with the LSB set to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9557 (see Figure 26 and Figure 27). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.



**Figure 26. Read From Register**



- This figure assumes the command byte has been previously programmed with 00h.
- Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.
- This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 26).

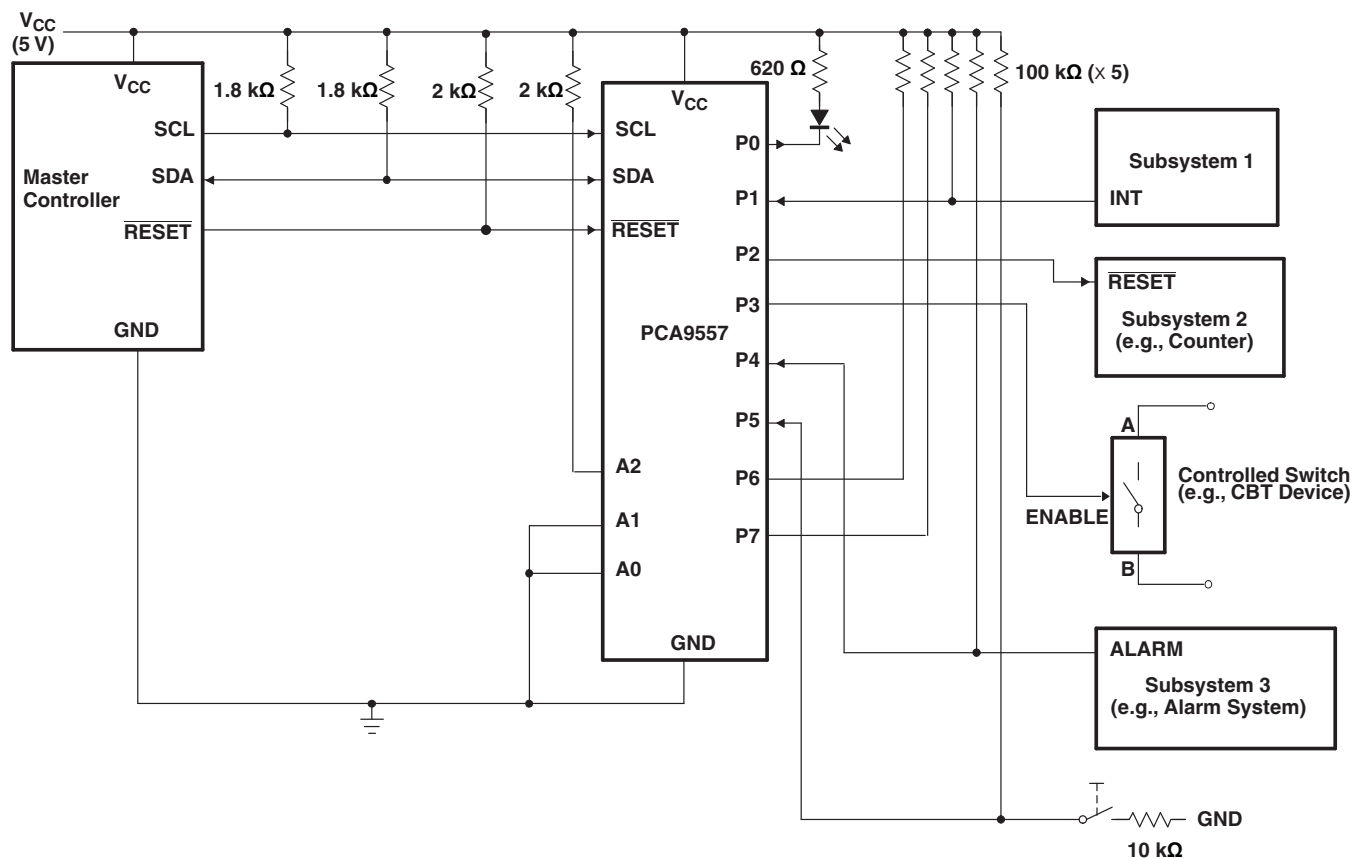
**Figure 27. Read Input Port Register**

## 9 Application And Implementation

### 9.1 Application Information

### 9.2 Typical Application

Figure 28 shows an application in which the PCA9557 can be used.



- A. Device address is configured as 0011100 for this example.
- B. P1, P4, and P5 are configured as inputs.
- C. P0, P2, and P3 are configured as outputs.
- D. P6 and P7 are not used and must be configured as outputs.

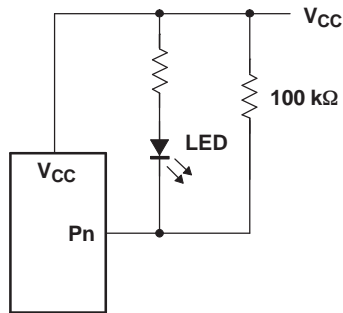
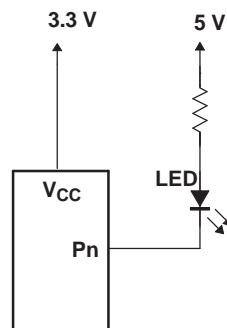
Figure 28. Typical Application

#### 9.2.1 Design Requirements

##### 9.2.1.1 Minimizing $I_{CC}$ When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to  $V_{CC}$  through a resistor as shown in Figure 28. The LED acts as a diode so, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in *Electrical Characteristics* shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{CC}$  when the LED is off.

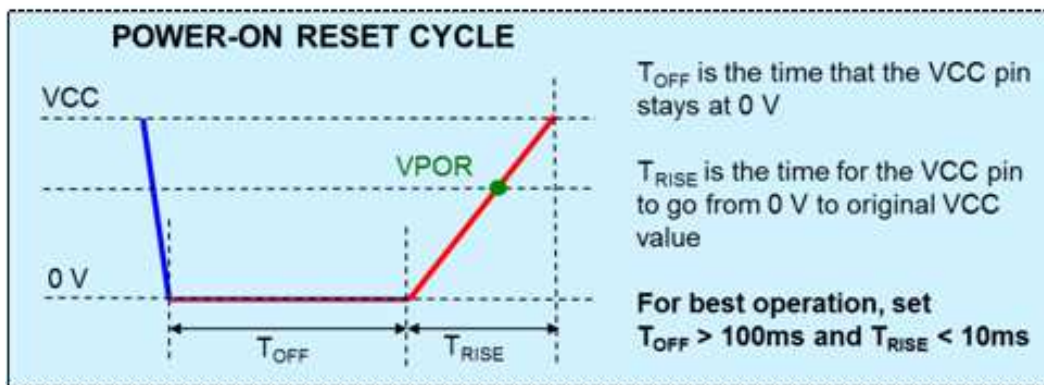
Figure 29 shows a high-value resistor in parallel with the LED. Figure 30 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply-current consumption when the LED is off.

**Typical Application (continued)**

**Figure 29. High-Value Resistor In Parallel With The Led**

**Figure 30. Device Supplied By A Low Voltage**

## 10 Power Supply Recommendations

### 10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



### System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9557D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9557	<a href="#">Samples</a>
PCA9557DB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9557	<a href="#">Samples</a>
PCA9557DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9557	<a href="#">Samples</a>
PCA9557PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557RGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557	<a href="#">Samples</a>
PCA9557RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.



- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9557DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9557DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
PCA9557DT	SOIC	D	16	250	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
PCA9557PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9557PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9557RGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9557RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9557DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
PCA9557DR	SOIC	D	16	2500	367.0	367.0	38.0
PCA9557DT	SOIC	D	16	250	210.0	185.0	35.0
PCA9557PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
PCA9557PWT	TSSOP	PW	16	250	367.0	367.0	35.0
PCA9557RGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
PCA9557RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

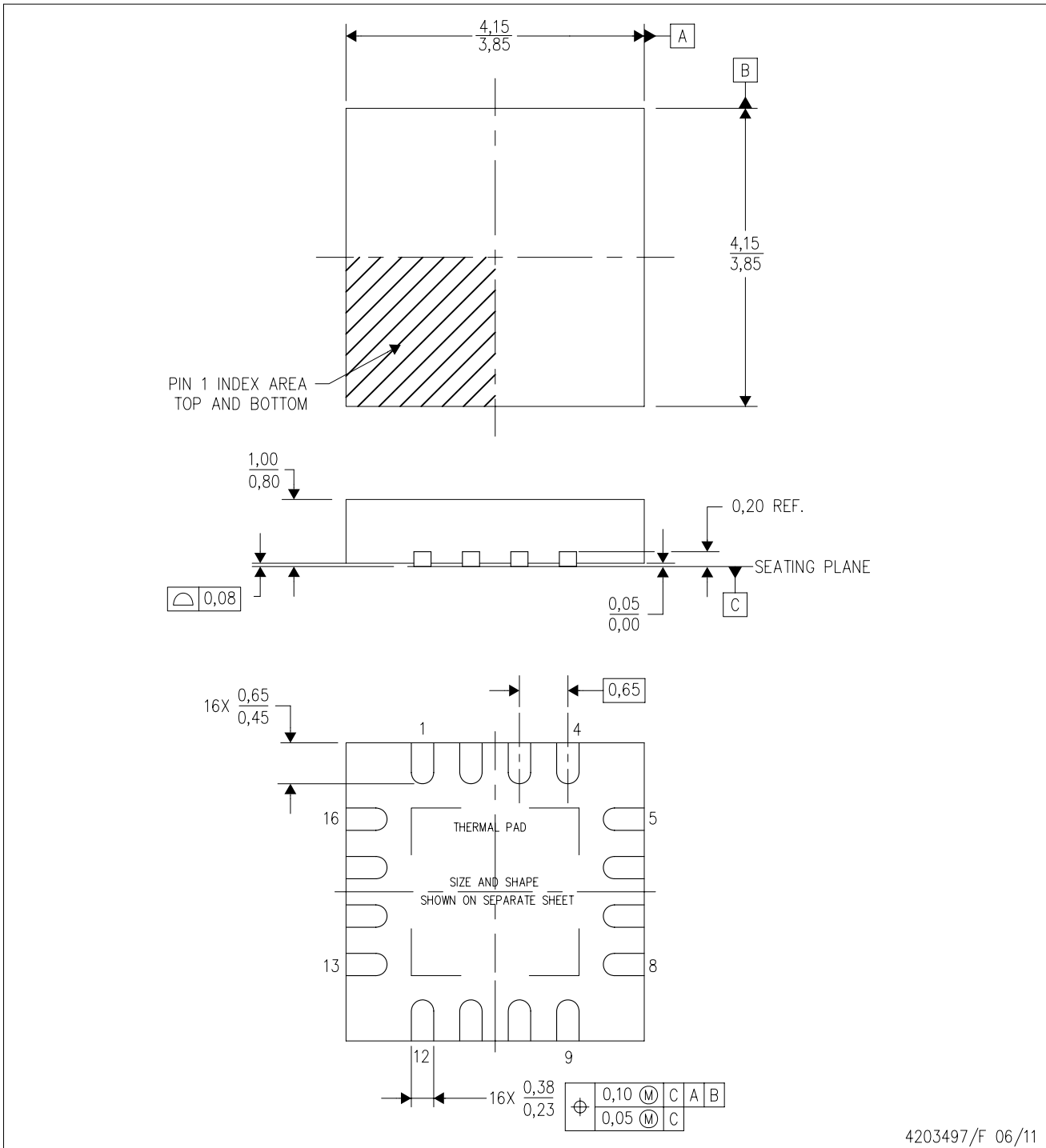


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203497/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RGV (S-PVQFN-N16)

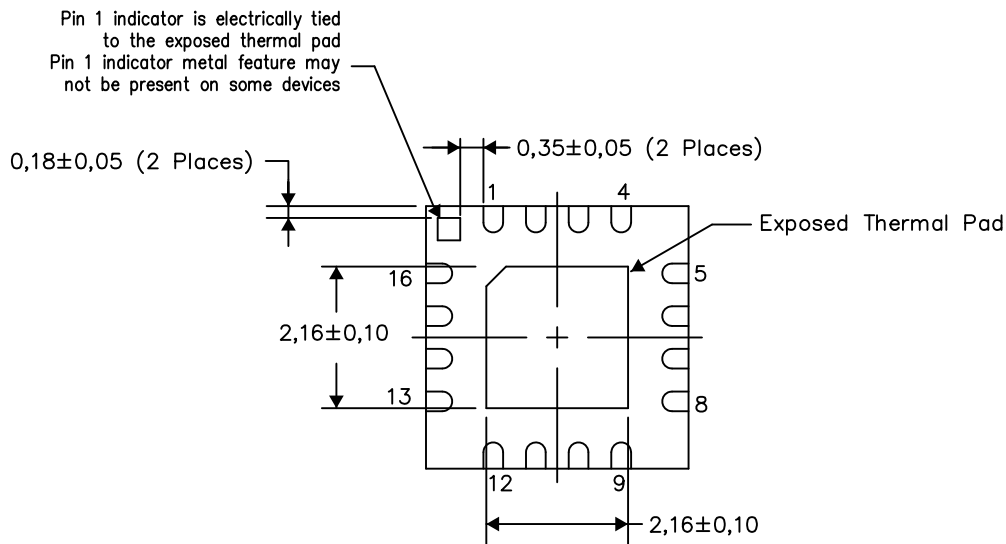
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206351-2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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