ISL98001

Triple Video Digitizer with Digital PLL

FN6148
Rev 5.00
September 21, 2010

The ISL98001 3-Channel, 8-bit Analog Front-End (AFE) contains all the functions necessary to digitize analog YPbPr video signals and RGB graphics signals from DVD players, digital VCRs, video set-top boxes, and personal computers. This product family's conversion rates support HDTV resolutions up to 1080p and PC monitor resolutions up to UXGA and QXGA, while the front end's programmable input bandwidth ensures sharp, clear images at all resolutions.

To maximize performance with the widest variety of video sources, the ISL98001 features a fast-responding digital PLL (DPLL), providing extremely low jitter with PC graphics signals and quick recovery from VCR head switching with video signals. Integrated HSYNC and SOG processing eliminate the need for external slicers, sync separators, Schmitt triggers, and filters.

Glitchless, automatic Macrovision™-compliance is obtained by a digital Macrovision detection function that detects and automatically removes Macrovision from the HSYNC signal.

Ease-of-use is also emphasized with features such as the elimination of PLL charge pump current/VCO range programming and single-bit switching between RGB and YPbPr signals. Automatic Black Level Compensation (ABLC) eliminates part-to-part offset variation, ensuring perfect black level performance in every application.

The ISL98001 is fully backwards compatible (hardware and software) with the X980xx family of AFEs.

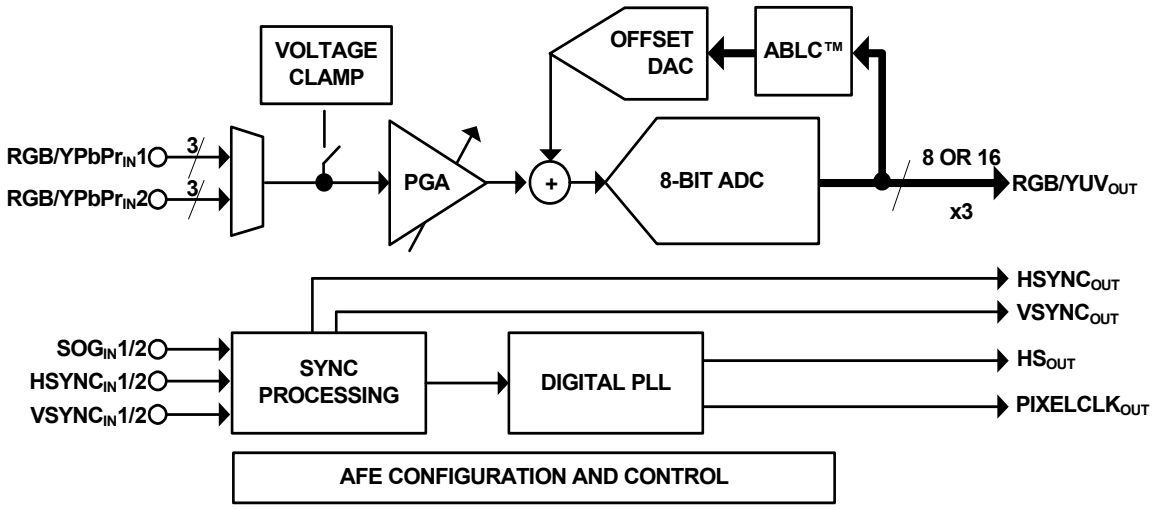
Features

- 140MSPS, 170MSPS, 210MSPS, and 275MSPS maximum conversion rates
- Glitchless Macrovision-compliant sync separator
- Extremely fast recovery from VCR head switching
- Low PLL clock jitter (250ps$_{P-P}$ @ 170MSPS)
- 64 intrapixel sampling positions
- 0.35V$_{P-P}$ to 1.4V$_{P-P}$ video input range
- Programmable bandwidth (100MHz to 780MHz)
- 2-channel input multiplexer
- RGB 4:4:4 and YUV 4:2:2 output formats
- 5 embedded voltage regulators allow operation from single 3.3V supply and enhance performance, isolation
- Completely independent 8-bit gain/10-bit offset control
- Pb-free (RoHS compliant)

Applications

- Digital TVs
- Projectors
- Multifunction monitors
- Digital KVM
- RGB graphics processing

Simplified Block Diagram

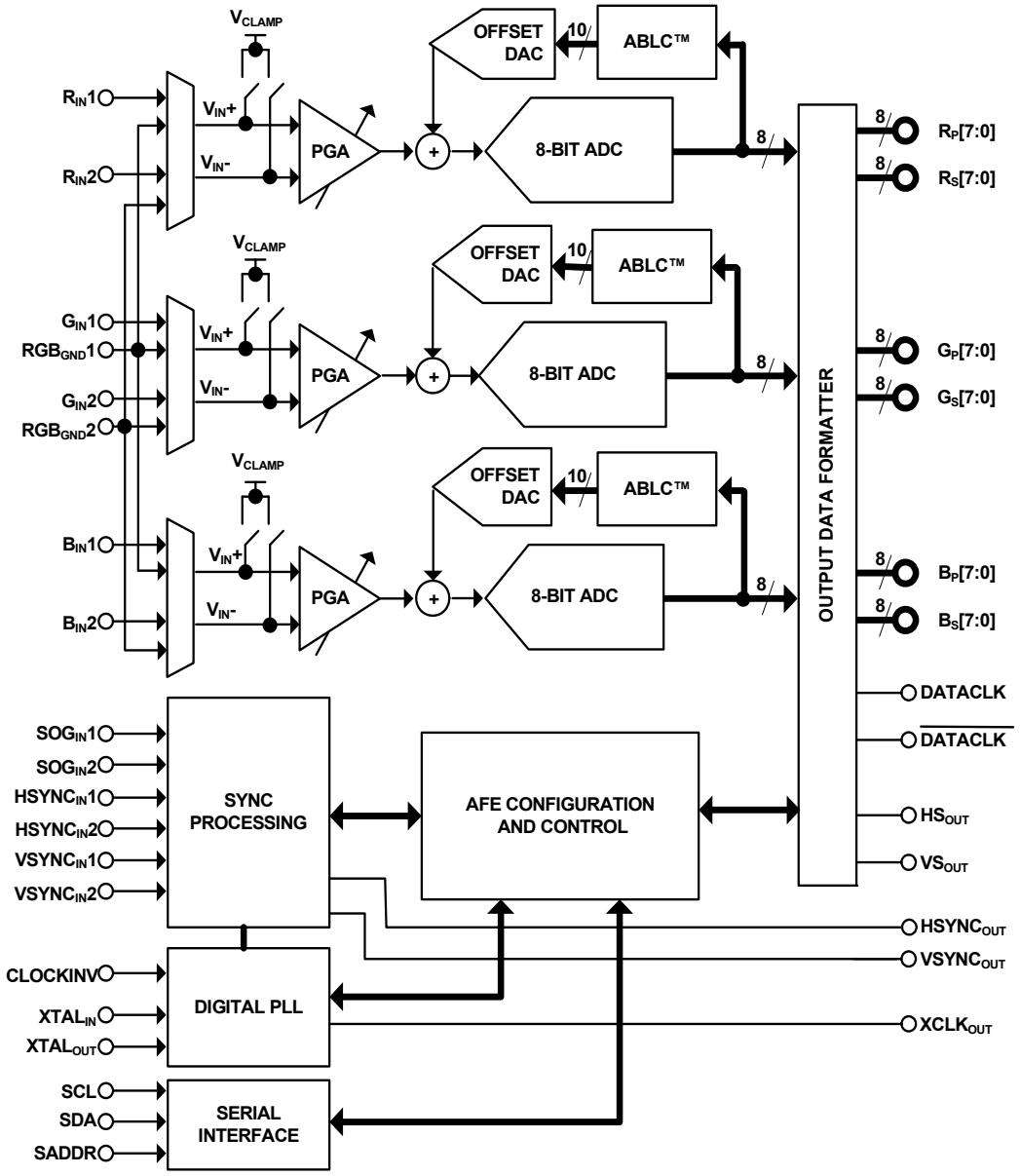


Ordering Information

PART NUMBER (Note)	MAXIMUM PIXEL RATE (MHz)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL98001IQZ-140	140	-40 to +85	128 MQFP	MDP0055
ISL98001CQZ-140	140	0 to +70	128 MQFP	MDP0055
ISL98001CQZ-170	170	0 to +70	128 MQFP	MDP0055
ISL98001CQZ-210	210	0 to +70	128 MQFP	MDP0055
ISL98001CQZ-275	275	0 to +70	128 MQFP	MDP0055

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Absolute Maximum Ratings

Voltage on V_A, V_D, or V_X
(referenced to GND_A = GND_D = GND_X) 4.0V
Voltage on any Analog Input Pin
(referenced to GND_A). . . . . -0.3V to V_A
Voltage on any Digital Input Pin
(referenced to GND_D) . . . . . -0.3V to +6.0V
Current into any Output Pin . . . . . ±20mA
ESD Classification
Human Body Model 2000V
Machine Model 200V

Thermal Information

Thermal Resistance, Typical (Note 1) θ_{JA} (°C/W)
MQFP Package 55
Maximum Biased Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature
Commercial . . . . . 0°C to +70°C
Industrial. . . . . -40°C to +85°C
Supply Voltage. . . . . V_A = V_D = V_X = 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Specifications apply for V_A = V_D = V_X = 3.3V, pixel rate = 140MHz for ISL98001-140, 170MHz for ISL98001-170, 210MHz for ISL98001-210, or 275MHz for ISL98001-275, f_{XTAL} = 25MHz, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	COMMENT	MIN	TYP	MAX	UNIT
FULL CHANNEL CHARACTERISTICS						
	Conversion Rate	Per channel				
	ISL98001-140		10		140	MHz
	ISL98001-170		10		170	MHz
	ISL98001-210		10		210	MHz
	ISL98001-275	To achieve rated 275MHz speeds, see “Initialization” on page 26.	10		275	MHz
	ADC Resolution		8			Bits
	Missing Codes	Guaranteed monotonic			None	
DNL (Full-Channel)	Differential Non-Linearity					
	ISL98001-140			±0.5	+1.0/-0.9	LSB
	ISL98001-170			±0.5	+1.0/-0.9	LSB
	ISL98001-210			±0.6	+1.0/-0.9	LSB
	ISL98001-275			±0.7	+1.2/-0.9	LSB
INL (Full-Channel)	Integral Non-Linearity					
	ISL98001-140			±1.1	±2.75	LSB
	ISL98001-170			±1.1	±3.25	LSB
	ISL98001-210			±1.25	±3.25	LSB
	ISL98001-275			±1.6	±3.75	LSB
	Gain Adjustment Range			±6		dB
	Gain Adjustment Resolution			8		Bits
	Gain Matching Between Channels	Percent of full scale		±1		%
	Full Channel Offset Error, ABLC enabled	ADC LSBs, over time and temperature		±0.125	±0.5	LSB
	Offset Adjustment Range (ABLC enabled or disabled)	ADC LSBs (See “Automatic Black Level Compensation (ABLC™) and Gain Control” on page 19)		±127		LSB

Electrical Specifications Specifications apply for $V_A = V_D = V_X = 3.3V$, pixel rate = 140MHz for ISL98001-140, 170MHz for ISL98001-170, 210MHz for ISL98001-210, or 275MHz for ISL98001-275, f_{XTAL} = 25MHz, T_A = +25°C, unless otherwise noted. **(Continued)**

SYMBOL	PARAMETER	COMMENT	MIN	TYP	MAX	UNIT
ANALOG VIDEO INPUT CHARACTERISTICS ($R_{IN}1$, $G_{IN}1$, $B_{IN}1$, $R_{IN}2$, $G_{IN}2$, $B_{IN}2$)						
	Input Range		0.35	0.7	1.4	V_{P-P}
	Input Bias Current	DC restore clamp off		±0.01	±1	µA
	Input Capacitance			5		pF
	Full Power Bandwidth	Programmable		780		MHz
INPUT CHARACTERISTICS ($SOG_{IN}1$, $SOG_{IN}2$)						
V_{IH}/V_{IL}	Input Threshold Voltage	Programmable - see register listing for details		0 to -0.3		V
	Hysteresis	Centered around threshold		40		mV
	Input Capacitance			5		pF
INPUT CHARACTERISTICS ($HSYNC_{IN}1$, $HSYNC_{IN}2$)						
V_{IH}/V_{IL}	Input Threshold Voltage	Programmable - see register listing for details		0.4 to 3.2		V
	Hysteresis	Centered around threshold voltage		240		mV
R_{IN}	Input Impedance			1.2		kΩ
C_{IN}	Input Capacitance			5		pF
DIGITAL INPUT CHARACTERISTICS (SDA, SADDR, CLOCKINV$_{IN}$, $\overline{\text{RESET}}$)						
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I	Input Leakage Current	$\overline{\text{RESET}}$ has a 70kΩ pullup to V_D		±10		nA
	Input Capacitance			5		pF
SCHMITT DIGITAL INPUT CHARACTERISTICS (SCL, $VSYNC_{IN}1$, $VSYNC_{IN}2$)						
V_T+	Low to High Threshold Voltage		1.45			V
V_T-	High to Low Threshold Voltage				0.95	V
I	Input Leakage Current			±10		nA
	Input Capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS (DATACLK, $\overline{\text{DATACLK}}$)						
V_{OH}	Output HIGH Voltage, I_O = 16mA		2.4			V
V_{OL}	Output LOW Voltage, I_O = -16mA				0.4	V
DIGITAL OUTPUT CHARACTERISTICS (R_P, G_P, B_P, R_S, G_S, B_S, HS_{OUT}, VS_{OUT}, $HSYNC_{OUT}$, $VSYNC_{OUT}$)						
V_{OH}	Output HIGH Voltage, I_O = 8mA		2.4			V
V_{OL}	Output LOW Voltage, I_O = -8mA				0.4	V
R_{TRI}	Pulldown to GND_D when Three-state	R_P, G_P, B_P, R_S, G_S, B_S only		56		kΩ
DIGITAL OUTPUT CHARACTERISTICS (SDA, $XCLK_{OUT}$)						
V_{OH}	Output HIGH Voltage, I_O = 4mA	$XCLK_{OUT}$ only; SDA is open-drain	2.4			V
V_{OL}	Output LOW Voltage, I_O = -4mA				0.4	V
POWER SUPPLY REQUIREMENTS						
V_A	Analog Supply Voltage		3	3.3	3.6	V
V_D	Digital Supply Voltage		3	3.3	3.6	V
V_X	Crystal Oscillator Supply Voltage		3	3.3	3.6	V
I_A	Analog Supply Current				200	mA

Electrical Specifications Specifications apply for $V_A = V_D = V_X = 3.3V$, pixel rate = 140MHz for ISL98001-140, 170MHz for ISL98001-170, 210MHz for ISL98001-210, or 275MHz for ISL98001-275, f_{XTAL} = 25MHz, T_A = +25°C, unless otherwise noted. **(Continued)**

SYMBOL	PARAMETER	COMMENT	MIN	TYP	MAX	UNIT
I_D	Digital Supply Current	With grayscale ramp input			200	mA
I_X	Crystal Oscillator Supply Current			1.4	2	mA
P_D	Total Power Dissipation					
	ISL98001-140	With grayscale ramp input		0.95	1.10	W
	ISL98001-170	With grayscale ramp input		1.05	1.15	W
	ISL98001-210	With grayscale ramp input		1.10	1.20	W
	ISL98001-275	With grayscale ramp input		1.20	1.30	W
	Standby Mode	ADCs, PLL powered down		50	80	mW
AC TIMING CHARACTERISTICS						
	PLL Jitter			250	450	ps p-p
	Sampling Phase Steps	5.6° per step	64			
	Sampling Phase Tempco			±1		ps/°C
	Sampling Phase Differential Nonlinearity	Degrees out of 360°		±3		°
	HSYNC Frequency Range		10		150	kHz
f_{XTAL}	Crystal Frequency Range		23	25	27	MHz
f_{XTALIN}	Frequency Range with External 3.3V Clock Signal Driving $XTAL_{IN}$		23	25	33.5	MHz
t_{SETUP}	DATA Valid Before Rising Edge of DATACLK	15pF DATACLK load, 15pF DATA load (Note 2)	1.3			ns
t_{HOLD}	DATA Valid After Rising Edge of DATACLK	15pF DATACLK load, 15pF DATA load (Note 2)	2.0			ns
AC TIMING CHARACTERISTICS (2-WIRE INTERFACE)						
f_{SCL}	SCL Clock Frequency		0		400	kHz
	Maximum Width of a Glitch on SCL that Will be Suppressed	2 XTAL periods min	80			ns
t_{AA}	SCL LOW to SDA Data Out Valid	5 XTAL periods plus SDA's RC time constant			Refer to comment	µs
t_{BUF}	Time the Bus Must be Free Before a New Transmission Can Start		1.3			µs
t_{LOW}	Clock LOW Time		1.3			µs
t_{HIGH}	Clock HIGH Time		0.6			µs
$t_{SU:STA}$	Start Condition Setup Time		0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		0.6			µs
$t_{SU:DAT}$	Data In Setup Time		100			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
$t_{SU:STO}$	Stop Condition Setup Time		0.6			µs
t_{DH}	Data Output Hold Time	4 XTAL periods min	160			ns

NOTE:

2. Setup and hold times are specified for a 170MHz DATACLK rate.

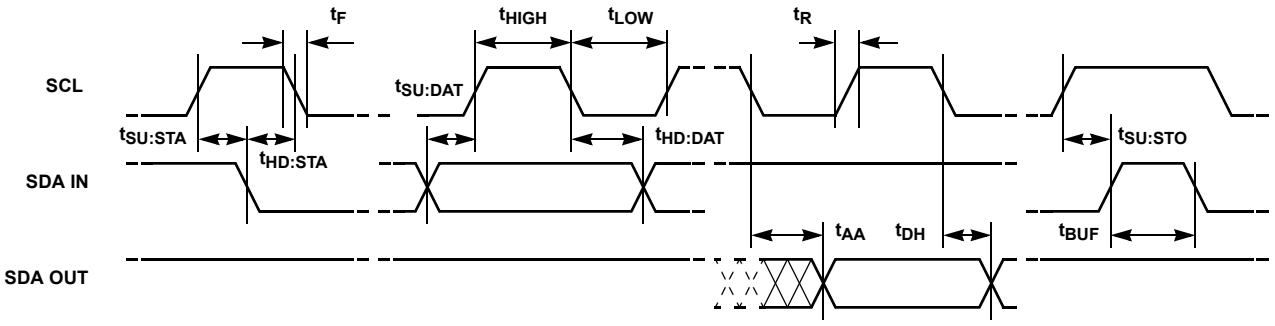


FIGURE 1. 2-WIRE INTERFACE TIMING

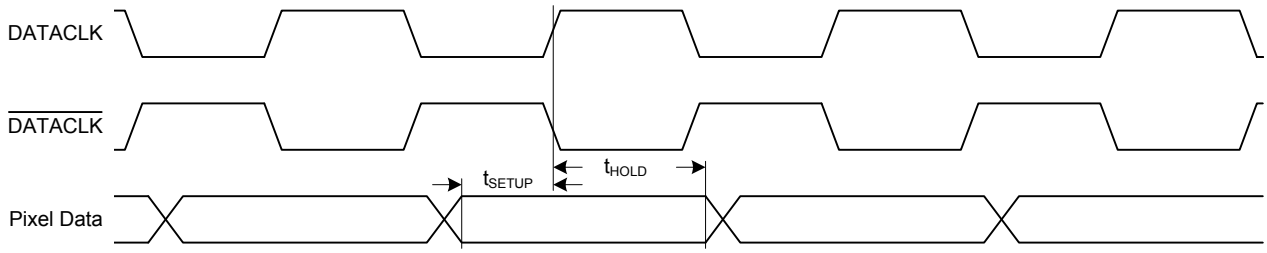


FIGURE 2. DATA OUTPUT SETUP AND HOLD TIMING

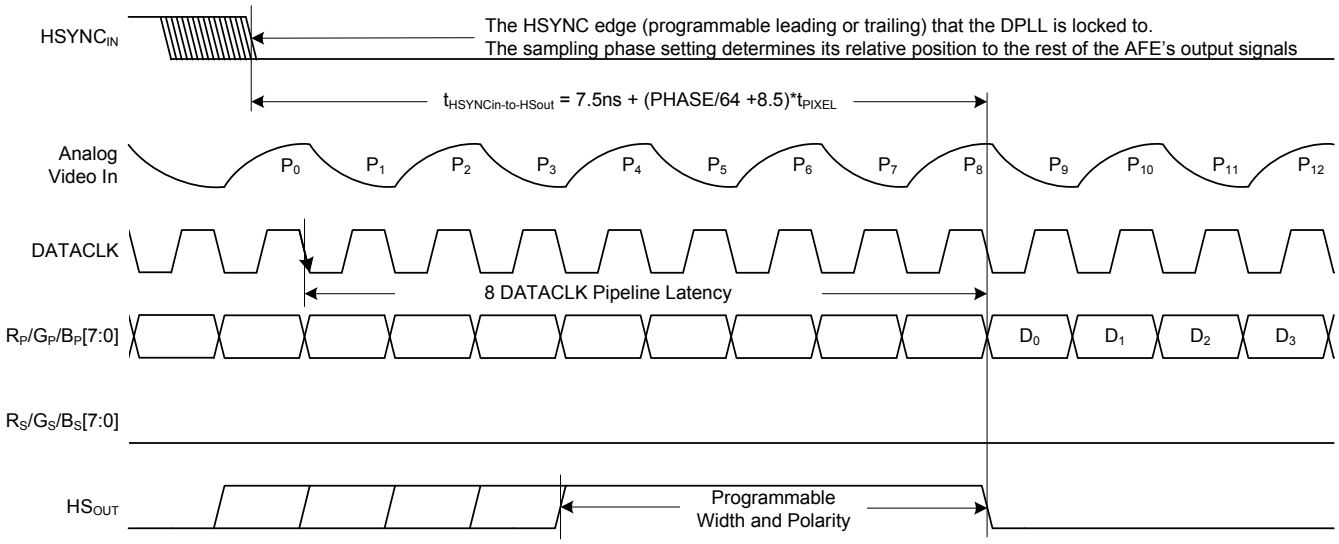


FIGURE 3. 24-BIT OUTPUT MODE

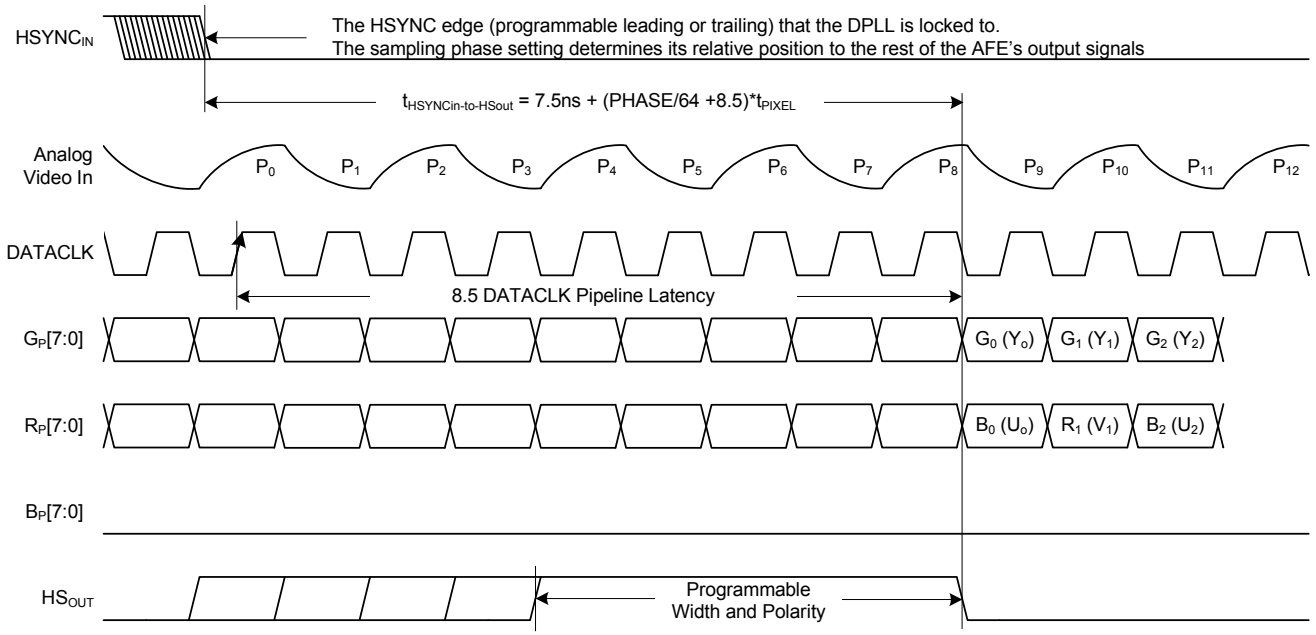


FIGURE 4. 24-BIT 4:2:2 OUTPUT MODE (FOR YUV SIGNALS)

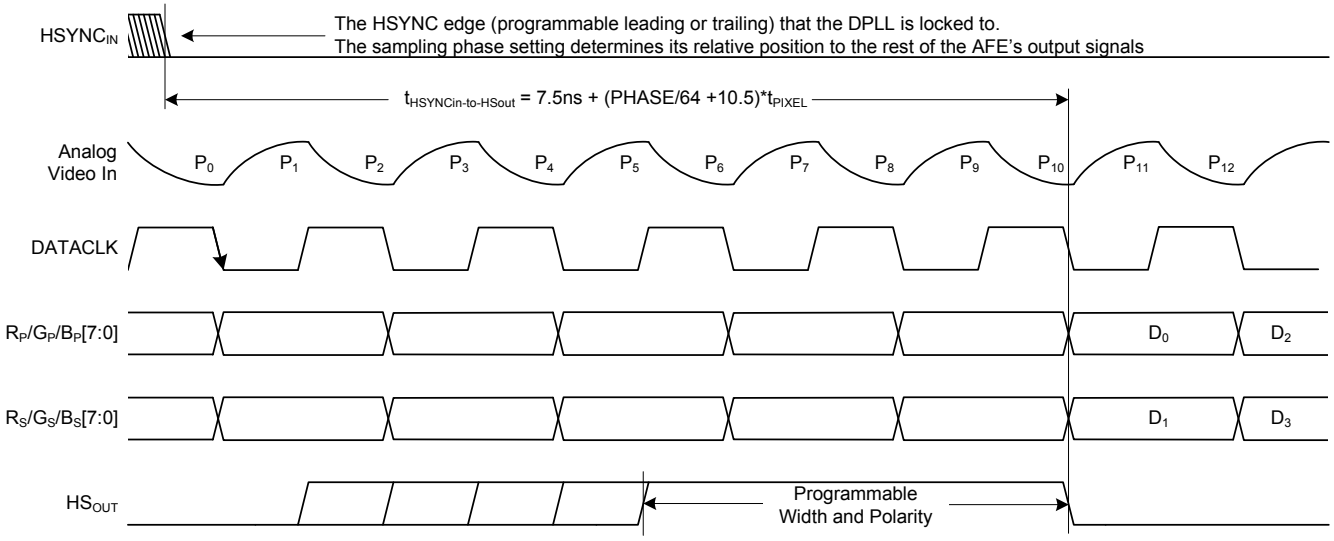


FIGURE 5. 48-BIT OUTPUT MODE

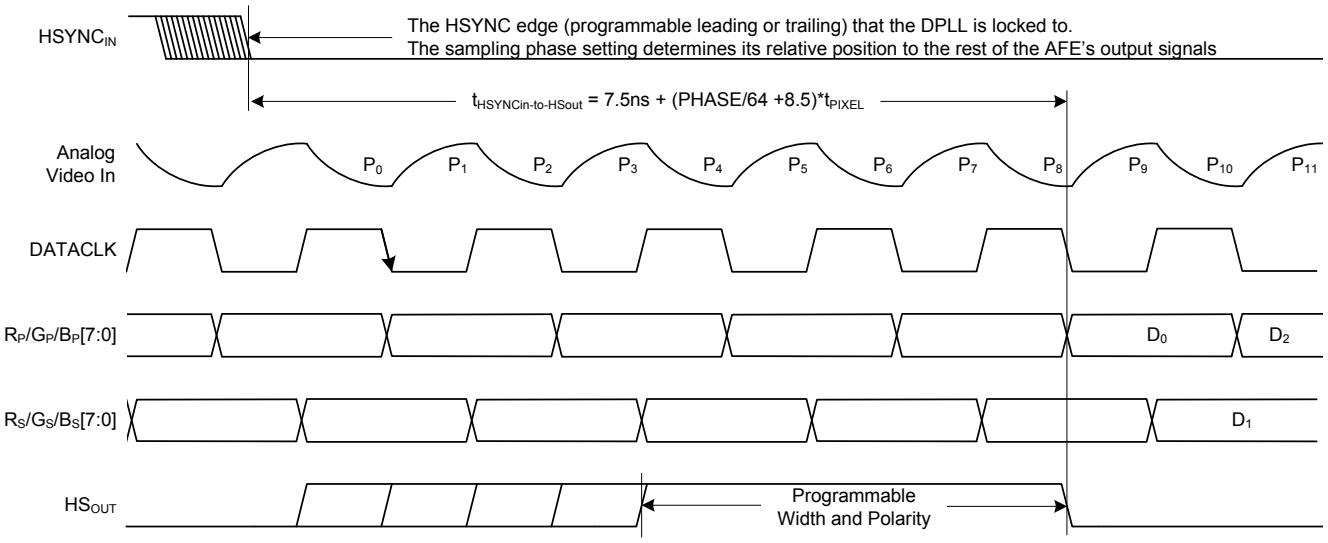
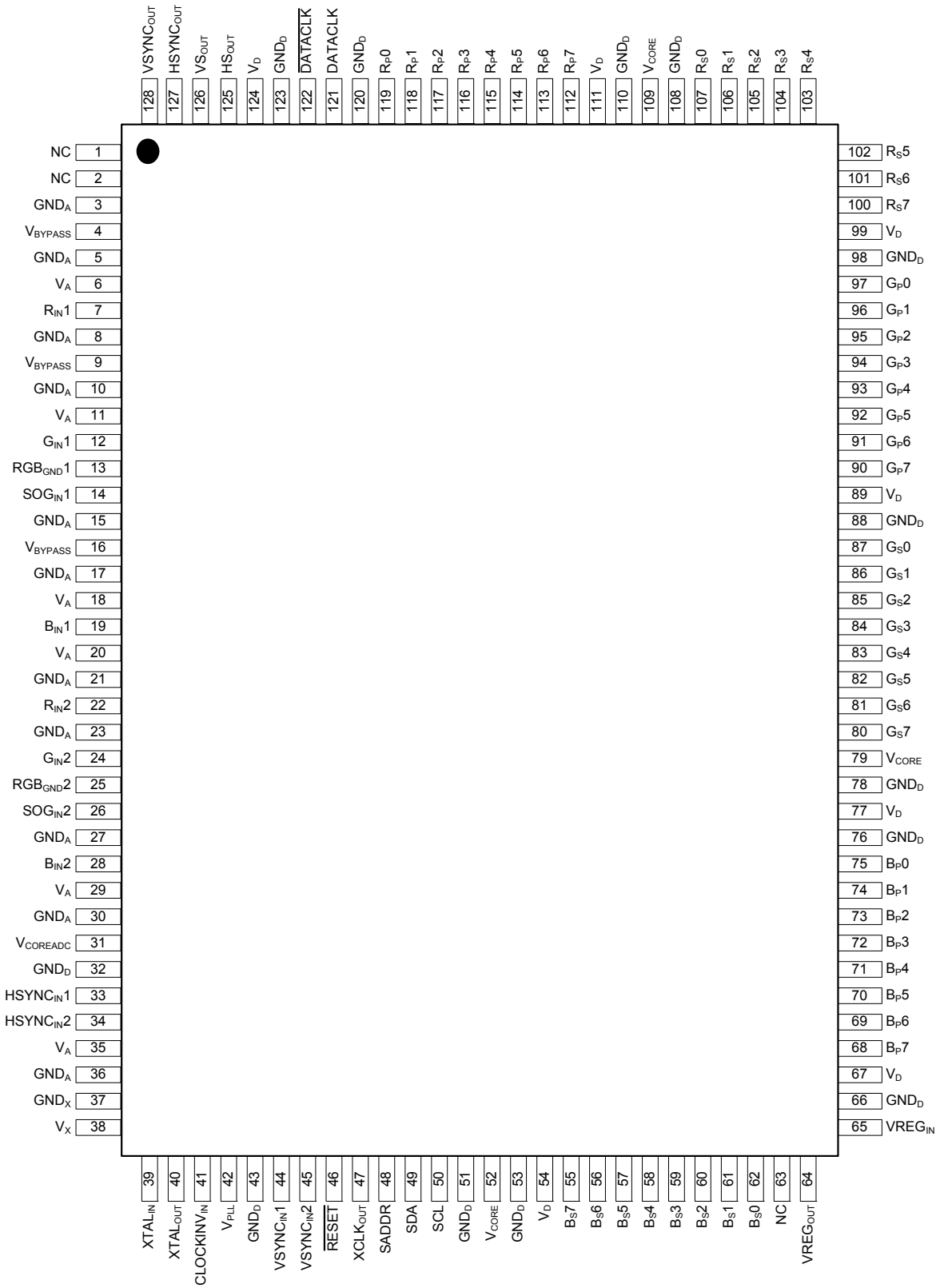


FIGURE 6. 48-BIT OUTPUT MODE, INTERLEAVED TIMING

Pin Configuration (MQFP, ISL98001)



Pin Descriptions

SYMBOL	MQFP PIN #(s)	DESCRIPTION
$R_{IN}1$	7	Analog input. Red Channel 1. DC couple or AC couple through 0.1µF.
$G_{IN}1$	12	Analog input. Green Channel 1. DC couple or AC couple through 0.1µF.
$B_{IN}1$	19	Analog input. Blue Channel 1. DC couple or AC couple through 0.1µF.
$RGB_{GND}1$	13	Analog input. Ground reference for the R, G, and B inputs of channel 1 in the DC coupled configuration. Connect to the same ground as Channel 1's R, G, and B termination resistors. This signal is not used in the AC-coupled configuration, but the pin should still be tied to GND_A.
$SOG_{IN}1$	14	Analog input. Sync on Green. Connect to $G_{IN}1$ through a 0.01µF capacitor in series with a 500Ω resistor.
$HSYNC_{IN}1$	33	Digital input, 5V tolerant, 240mV hysteresis, 1.2kΩ impedance to GND_A. Connect to Channel 1's HSYNC signal through a 680Ω series resistor.
$VSYNC_{IN}1$	44	Digital input, 5V tolerant, 500mV hysteresis. Connect to Channel 1's VSYNC signal.
$R_{IN}2$	22	Analog input. Red Channel 2. DC couple or AC couple through 0.1µF.
$G_{IN}2$	24	Analog input. Green Channel 2. DC couple or AC couple through 0.1µF.
$B_{IN}2$	28	Analog input. Blue Channel 2. DC couple or AC couple through 0.1µF.
$RGB_{GND}2$	25	Analog input. Ground reference for the R, G, and B inputs of Channel 2 in the DC coupled configuration. Connect to the same ground as Channel 1's R, G, and B termination resistors. This signal is not used in the AC-coupled configuration, but the pin should still be tied to GND_A.
$SOG_{IN}2$	26	Analog input. Sync on Green. Connect to $G_{IN}1$ through a 0.01µF capacitor in series with a 500Ω resistor.
$HSYNC_{IN}2$	34	Digital input, 5V tolerant, 240mV hysteresis, 1.2kΩ impedance to GND_A. Connect to Channel 2's HSYNC signal through a 680Ω series resistor.
$VSYNC_{IN}2$	45	Digital input, 5V tolerant, 500mV hysteresis. Connect to Channel 2's VSYNC signal.
$CLOCKINV_{IN}$	41	Digital input, 5V tolerant. When high, changes the pixel sampling phase by 180°. Toggle at frame rate during VSYNC to allow 2x undersampling to sample odd and even pixels on sequential frames. Tie to D_{GND} if unused.
$\overline{RESET}$	46	Digital input, 5V tolerant, active low, 70kΩ pullup to V_D. Take low for at least 1µs and then high again to reset the ISL98001. This pin is not necessary for normal use and may be tied directly to the V_D supply.
$XTAL_{IN}$	39	Analog input. Connect to external 24.5MHz to 27MHz crystal and load capacitor (See crystal spec for recommended loading). Typical oscillation amplitude is $1.0V_{P-P}$ centered around 0.5V.
$XTAL_{OUT}$	40	Analog output. Connect to external 24.5MHz to 27MHz crystal and load capacitor (See crystal spec for recommended loading). Typical oscillation amplitude is $1.0V_{P-P}$ centered around 0.5V.
$XCLK_{OUT}$	47	3.3V digital output. Buffered crystal clock output at f_{XTAL} or $f_{XTAL}/2$. May be used as system clock for other system components.
SADDR	48	Digital input, 5V tolerant. Address = 0x4C when tied low. Address = 0x4D when tied high.
SCL	50	Digital input, 5V tolerant, 500mV hysteresis. Serial data clock for 2-wire interface.
SDA	49	Bidirectional Digital I/O, open drain, 5V tolerant. Serial data I/O for 2-wire interface.
R_P[7:0]	112-119	3.3V digital output. Red channel, primary pixel data. 56k pulldown when three-stated.
R_S[7:0]	100-107	3.3V digital output. Red channel, secondary pixel data. 56k pulldown when three-stated.
G_P[7:0]	90-97	3.3V digital output. Green channel, primary pixel data. 56k pulldown when three-stated.
G_S[7:0]	80-87	3.3V digital output. Green channel, secondary pixel data. 56k pulldown when three-stated.
B_P[7:0]	68-75	3.3V digital output. Blue channel, primary pixel data. 56k pulldown when three-stated.
B_S[7:0]	55-62	3.3V digital output. Blue channel, secondary pixel data. 56k pulldown when three-stated.
DATACLK	121	3.3V digital output. Data clock output. Equal to pixel clock rate in 24-bit mode, one half of pixel clock rate in 48-bit mode.
DATACLK	122	3.3V digital output. Inverse of DATACLK.
HS_{OUT}	125	3.3V digital output. HSYNC output aligned with pixel data. Use this output to frame the digital output data. This output is always purely horizontal sync (without any composite sync signals).

Pin Descriptions (Continued)

SYMBOL	MQFP PIN #(s)	DESCRIPTION
VS_{OUT}	126	3.3V digital output. Artificial VSYNC output aligned with pixel data. VS_{OUT} is generated 8 pixel clocks after the trailing edge of HS_{OUT}. *This signal is usually not needed.*
$HSYNC_{OUT}$	127	3.3V digital output. Buffered HSYNC (or SOG or CSYNC) output. This is typically used for measuring HSYNC period. This output will pass composite sync signals and Macrovision signals if present on $HSYNC_{IN}$ or SOG_{IN}.
$VSYNC_{OUT}$	128	3.3V digital output. Buffered VSYNC output. For composite sync signals, this output will be asserted for the duration of the disruption of the normal HSYNC pattern. This is typically used for measuring VSYNC period.
V_A	6, 11, 18, 20, 29, 35	Power supply for the analog section. Connect to a 3.3V supply and bypass each pin to GND_A with 0.1µF.
GND_A	3, 5, 8, 10, 15, 17, 21, 23, 27, 30, 36	Ground return for V_A and V_{BYPASS}.
V_D	54, 67, 77, 89, 99, 111, 124	Power supply for all digital I/Os. Connect to a 3.3V supply and bypass each pin to GND_D with 0.1µF.
GND_D	32, 43, 51, 53, 66, 76, 78, 88, 98, 108, 110, 120, 123	Ground return for V_D, V_{CORE}, $V_{COREADC}$, and V_{PLL}.
V_X	38	Power supply for crystal oscillator. Connect to a 3.3V supply and bypass to GND_X with 0.1µF.
GND_X	37	Ground return for V_X.
V_{BYPASS}	4, 9, 16	Bypass these pins to GND_A with 0.1µF. Do not connect these pins to each other or anything else.
$VREG_{IN}$	65	3.3V input voltage for V_{CORE} voltage regulator. Connect to a 3.3V source and bypass to GND_D with 0.1µF.
$VREG_{OUT}$	64	Regulated output voltage for V_{PLL}, $V_{COREADC}$ and V_{CORE}; typically 1.9V. Connect only to V_{PLL}, $V_{COREADC}$ and V_{CORE} and bypass at input pins as instructed in the following. Do not connect to anything else - this output can only supply power to V_{PLL}, $V_{COREADC}$ and V_{CORE}.
$V_{COREADC}$	31	Internal power for the ADC's digital logic. Connect to $VREG_{OUT}$ through a 10Ω resistor and bypass to GND_D with 0.1µF.
V_{PLL}	42	Internal power for the PLL's digital logic. Connect to $VREG_{OUT}$ through a 10Ω resistor and bypass to GND_D with 0.1µF.
V_{CORE}	52, 79, 109	Internal power for core logic. Connect to $VREG_{OUT}$ and bypass each pin to GND_D with 0.1µF.
NC	1, 2, 63	Reserved. Do not connect anything to these pins.

Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Device ID (read only)	3:0	Device Revision	1 = initial silicon, 2 = second revision, etc.
		7:4	Device ID	1 = ISL98001
0x01	SYNC Status (read only)	0	HSYNC1 Active	0: HSYNC1 is Inactive 1: HSYNC1 is Active
		1	HSYNC2 Active	0: HSYNC2 is Inactive 1: HSYNC2 is Active
		2	VSYNC1 Active	0: VSYNC1 is Inactive 1: VSYNC1 is Active
		3	VSYNC2 Active	0: VSYNC2 is Inactive 1: VSYNC2 is Active
		4	SOG1 Active	0: SOG1 is Inactive 1: SOG1 is Active
		5	SOG2 Active	0: SOG2 is Inactive 1: SOG2 is Active
		6	PLL Locked	0: PLL is unlocked 1: PLL is locked to incoming HSYNC
		7	CSYNC Detect at Sync Splitter	0: Composite Sync signal not detected 1: Composite Sync signal is detected
0x02	SYNC Polarity (read only)	0	HSYNC1 Polarity	0: HSYNC1 is Active High 1: HSYNC1 is Active Low
		1	HSYNC2 Polarity	0: HSYNC2 is Active High 1: HSYNC2 is Active Low
		2	VSYNC1 Polarity	0: VSYNC1 is Active High 1: VSYNC1 is Active Low
		3	VSYNC2 Polarity	0: VSYNC2 is Active High 1: VSYNC2 is Active Low
		4	HSYNC1 Trilevel	0: HSYNC1 is Standard Sync 1: HSYNC1 is Trilevel Sync
		5	HSYNC2 Trilevel	0: HSYNC2 is Standard Sync 1: HSYNC2 is Trilevel Sync
		7:6	N/A	Returns 0
0x03	HSYNC Slicer (0x33)	2:0	HSYNC1 Threshold	000 = lowest (0.4V) **All values referred to** 011 = default (1.6V) **voltage at HSYNC input** 111 = highest (3.2V) **pin, 240mV hysteresis**
		3	Reserved	Set to 00
		6:4	HSYNC2 Threshold	See HSYNC1
		7	Disable Glitch Filter	0: HSYNC/VSYNC Glitch Filter Enabled (default) 1: HSYNC/VSYNC Glitch Filter Disabled
0x04	SOG Slicer (0x16) Note: Due to normal device-to-device variation in slicer levels, SOG Slicer settings of 0 (0mV), 1 (20mV), and 2 (40mV) may not be functional. The minimum recommended SOG Slicer setting is 3 (60mV).	3:0	SOG1 and SOG2 Threshold	0x0 = lowest (0mV) 0x6 = default (120mV) **20mV step size** 0xF = highest (300mV)
		4	SOG Filter Enable	0: SOG low pass filter disabled 1: SOG low pass filter enabled, 14MHz corner (default)
		5	SOG Hysteresis Disable	0: 40mV SOG hysteresis enabled 1: 40mV SOG hysteresis disabled (default)
		7:6	Reserved	Set to 00.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x05	Input configuration (0x00)	0	Channel Select	0: VGA1 1: VGA2
		1	Input Coupling	0: AC coupled (positive input connected to clamp DAC during clamp time, negative input disconnected from outside pad and always internally tied to appropriate clamp DAC). 1: DC coupled (+ and - inputs are brought to pads and never connected to clamp DACs). Analog clamp signal is turned off in this mode.
		2	RGB/YPbPr	0: RGB inputs Base ABLC target code = 0x00 for R, G, and B) 1: YPbPr inputs Base ABLC target code = 0x00 for G (Y) Base ABLC target code = 0x80 for R (Pr) and B (Pb)
		3	Sync Type	0: Separate HSYNC/VSYNC 1: Composite (from SOG or CSYNC on HSYNC)
		4	Composite Sync Source	0: SOG_{IN} 1: $HSYNC_{IN}$ Note: If Sync Type = 0, the multiplexer will pass $HSYNC_{IN}$ regardless of the state of this bit.
		5	COAST CLAMP enable	0: DC restore clamping and ABLC suspended during COAST. 1: DC restore clamping and ABLC continue during COAST.
		6	Sync Mask Disable	0: Interval between HSYNC pulses masked (preventing PLL from seeing Macrovision and any spurious glitches). 1: Interval between HSYNC pulses not masked (Macrovision will cause PLL to lose lock).
		7	$HSYNC_{OUT}$ Mask Disable	0: $HSYNC_{OUT}$ signal is masked (any Macrovision, sync glitches on incoming SYNC are stripped from $HSYNC_{OUT}$). 1: $HSYNC_{OUT}$ signal is not masked (any Macrovision, sync glitches on incoming SYNC appear on $HSYNC_{OUT}$). If Sync Mask Disable = 1, $HSYNC_{OUT}$ is not masked.
0x06	Red Gain (0x55)	7:0	Red Gain	Channel gain, where: gain (V/V) = 0.5 + [7:0]/170 0x00: gain = 0.5V/V ($1.4V_{P-P}$ input = full range of ADC) 0x55: gain = 1.0V/V ($0.7V_{P-P}$ input = full range of ADC) 0xFF: gain = 2.0V/V ($0.35V_{P-P}$ input = full range of ADC)
0x07	Green Gain (0x55)	7:0	Green Gain	
0x08	Blue Gain (0x55)	7:0	Blue Gain	

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x09	Red Offset (0x80)	7:0	Red Offset	ABLC enabled: digital offset control. A 1LSB change in this register will shift the ADC output by 1 LSB. ABLC disabled: analog offset control. These bits go to the upper 8-bits of the 10-bit offset DAC. A 1LSB change in this register will shift the ADC output approximately 1 LSB (Offset DAC range = 0) or 0.5LSBs (Offset DAC range = 1). 0x00 = min DAC value or -0x80 digital offset, 0x80 = mid DAC value or 0x00 digital offset, 0xFF = max DAC value or +0x7F digital offset
0x0A	Green Offset (0x80)	7:0	Green Offset	
0x0B	Blue Offset (0x80)	7:0	Blue Offset	
0x0C	Offset DAC Configuration (0x00)	0	Offset DAC Range	0: ±½ ADC fullscale (1 DAC LSB ~ 1 ADC LSB) 1: ±¼ ADC fullscale (1 DAC LSB ~ ½ ADC LSB)
		1	Reserved	Set to 0.
		3:2	Red Offset DAC LSBs	These bits are the LSBs necessary for 10-bit manual offset DAC control. Combine with their respective MSBs in registers 0x09, 0x0A, and 0x0B to achieve 10-bit offset DAC control.
		5:4	Green Offset DAC LSBs	
		7:6	Blue Offset DAC LSBs	
0x0D	AFE Bandwidth (0x2E)	0	Unused	Value doesn't matter
		3:1	AFE BW	3dB point for AFE lowpass filter 000b: 100MHz 111b: 780MHz (default)
		7:4	Peaking	0x0: Peaking off 0x1: Moderate peaking 0x2: Maximum recommended peaking (default) Values above 2 are not recommended.
0x0E	PLL Htotal MSB (0x03)	5:0	PLL Htotal MSB	14-bit HTOTAL (number of active pixels) value The minimum HTOTAL value supported is 0x200. HTOTAL to PLL is updated on LSB write only.
0x0F	PLL Htotal LSB (0x20)	7:0	PLL Htotal LSB	
0x10	PLL Sampling Phase (0x00)	5:0	PLL Sampling Phase	Used to control the phase of the ADC's sample point relative to the period of a pixel. Adjust to obtain optimum image quality. One step = 5.625° (1.56% of pixel period).
0x11	PLL Pre-coast (0x04)	7:0	Pre-coast	Number of lines the PLL will coast prior to the start of VSYNC.
0x12	PLL Post-coast (0x04)	7:0	Post-coast	Number of lines the PLL will coast after the end of VSYNC.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x13	PLL Misc (0x04)	0	PLL Lock Edge HSYNC1	0: Lock on trailing edge of HSYNC1 (default) 1: Lock on leading edge of HSYNC1
		1	PLL Lock Edge HSYNC2	0: Lock on trailing edge of HSYNC2 (default) 1: Lock on leading edge of HSYNC2
		2	Reserved	Set to 0
		3	$CLKINV_{IN}$ Pin Disable	0: $CLKINV_{IN}$ pin enabled (default) 1: $CLKINV_{IN}$ pin disabled (internally forced low)
		5:4	$CLKINV_{IN}$ Pin Function	00: CLKINV (default) 01: External CLAMP (See Note) 10: External COAST 11: External PIXCLK Note: the CLAMP pulse is used to - perform a DC restore (if enabled) - start the ABLC function (if enabled), and - update the data to the Offset DACs (always). In the default internal CLAMP mode, the ISL98001 automatically generates the CLAMP pulse. If External CLAMP is selected, the Offset DAC values only change on the leading edge of CLAMP. If there is no internal clamp signal, there will be up to a 100ms delay between when the PGA gain or offset DAC register is written to, and when the PGA or offset DAC is actually updated.
		6	$XCLK_{OUT}$ Frequency	0: $XCLK_{OUT} = f_{CRYSTAL}$ (default) 1: $XCLK_{OUT} = f_{CRYSTAL}/2$
		7	Disable $XCLK_{OUT}$	0 = $XCLK_{OUT}$ enabled 1 = $XCLK_{OUT}$ is logic low
0x14	DC Restore and ABLC starting pixel MSB (0x00)	4:0	DC Restore and ABLC starting pixel (MSB)	Pixel after $HSYNC_{IN}$ trailing edge to begin DC restore and ABLC functions. 13-bits. Set this register to the first stable black pixel following the trailing edge of $HSYNC_{IN}$.
0x15	DC Restore and ABLC starting pixel LSB (0x03)	7:0	DC Restore and ABLC starting pixel (LSB)	
0x16	DC Restore Clamp Width (0x10)	7:0	DC Restore clamp width (pixels)	Width of DC restore clamp used in AC-coupled configurations. Has no effect on ABLC. Minimum value is 0x02 (a setting of 0x01 or 0x00 will not generate a clamp pulse).
0x17	ABLC Configuration (0x40)	0	ABLC disable	0: ABLC enabled (default) 1: ABLC disabled
		1	Reserved	Set to 0.
		3:2	ABLC pixel width	Number of black pixels averaged every line for ABLC function 00: 16 pixels [default] 01: 32 pixels 10: 64 pixels 11: 128 pixels
		6:4	ABLC bandwidth	ABLC Time constant (lines) = $2^{(5+[6:4])}$ 000 = 32 lines 100 = 512 lines (default) 111 = 4096 lines
		7	Reserved	Set to 0.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x18	Output Format (0x00)	0	Bus Width	0: 24-bits: Data output on R_P, G_P, B_P only; R_S, G_S, B_S are all driven low (default). 1: 48-bits: Data output on R_P, R_P, G_P, G_S, B_S, B_S.
		1	Interleaving (48-bit mode only)	0: No interleaving: data changes on same edge of DATACLK (default). 1: Interleaved: Secondary databus data changes on opposite edge of DATACLK from primary databus.
		2	Bus Swap (48-bit mode only)	0: First data byte after trailing edge of HSOUT appears on R_P, G_P, B_P (default). 1: First data byte after trailing edge of HSOUT appears on R_S, G_S, B_S (primary and secondary busses are reversed).
		3	UV order (422 mode only)	0: U0 V0 U2 V2 U4 V4 U6 V6… (default) 1: U0 V1 U2 V3 U4 V5 U6 V7… (X980xx)
		4	422 mode	0: Data is formatted as 4:4:4 (RGB, default). 1: Data is decimated to 4:2:2 (YUV), blue channel is driven low.
		5	DATACLK Polarity	0: HS_{OUT}, VS_{OUT}, and Pixel Data changes on falling edge of DATACLK (default). 1: HS_{OUT}, VS_{OUT}, and Pixel Data changes on rising edge of DATACLK.
		6	VS_{OUT} Polarity	0: Active High (default) 1: Active Low
		7	HS_{OUT} Polarity	0: Active High (default) 1: Active Low
0x19	HS_{OUT} Width (0x10)	7:0	HS_{OUT} Width	HS_{OUT} width, in pixels. Minimum value is 0x01 for 24-bit modes, 0x02 for 48-bit modes.
0x1A	Output Signal Disable (0x00)	0	Three-state R_P[7:0]	0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56kΩ pulldown resistors to GND_D.
		1	Three-state R_S7:0]	
		2	Three-state G_P[7:0]	
		3	Three-state G_S7:0]	
		4	Three-state B_P[7:0]	
		5	Three-state B_S[7:0]	
		6	Three-state $\overline{\text{DATACLK}}$	0 = $\overline{\text{DATACLK}}$ enabled 1 = $\overline{\text{DATACLK}}$ three-stated
		7	Three-state DATACLK	0 = DATACLK enabled 1 = DATACLK three-stated
0x1B	Power Control (0x00)	0	Red Power-down	0 = Red ADC operational (default) 1 = Red ADC powered down
		1	Green Power-down	0 = Green ADC operational (default) 1 = Green ADC powered down
		2	Blue Power-down	0 = Blue ADC operational (default) 1 = Blue ADC powered down
		3	PLL Power-down	0 = PLL operational (default) 1 = PLL powered down
		7:4	Reserved	Set to 0.
0x1C	PLL Tuning (0x49)	7:0	Reserved	Use default setting of 0x49 for all PC and video modes except signals coming from an analog VCR. Set to 0x4C for analog videotape compatibility.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x1D	Red ABLC Target (0x00)	7:0	Red ABLC Target	This is a 2's complement number controlling the target code of the Red ADC output when ABLC is enabled. In RGB mode, the Red ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). In YPbPr mode, the Red ADC output will be servoed to 0x80 + the number in this register (-0x80 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.
0x1E	Green ABLC Target (0x00)	7:0	Green ABLC Target	This is a 2's complement number controlling the target code of the Green ADC output when ABLC is enabled. In RGB and YPbPr modes, the Green ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.
0x1F	Blue ABLC Target (0x00)	7:0	Blue ABLC Target	This is a 2's complement number controlling the target code of the Blue ADC output when ABLC is enabled. In RGB mode, the Blue ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). In YPbPr mode, the Blue ADC output will be servoed to 0x80 + the number in this register (-0x80 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.
0x23	DC Restore Clamp (0x18)	3:0	Reserved	Set to 1000
		6:4	DC Restore Clamp Impedance	DC Restore clamp's ON resistance. Shared for all three channels 0: Infinite (clamp disconnected) (default) 1: 1600Ω 2: 800Ω 3: 533Ω 4: 400Ω 5: 320Ω 6: 267Ω 7: 228Ω
		7	Reserved	Set to 0.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x25	Sync Separator Control (0x00)	0	Three-state Sync Outputs	0: $VSYNC_{OUT}$, $HSYNC_{OUT}$, VS_{OUT}, HS_{OUT} are active (default). 1: $VSYNC_{OUT}$, $HSYNC_{OUT}$, VS_{OUT}, HS_{OUT} are in three-state.
		1	COAST Polarity	0: Coast active high (default) 1: Coast active low Set to 0 for internal VSYNC extracted from CSYNC. Set to 0 or 1 as appropriate to match external VSYNC or external COAST.
		2	HS_{OUT} Lock Edge	0: HS_{OUT}'s *trailing* edge is locked to selected $HSYNC_{IN}$'s lock edge. Leading edge moves backward in time as HS_{OUT} width is increased (X980xx default). 1: HS_{OUT}'s *leading* edge is locked to selected $HSYNC_{IN}$'s lock edge. Trailing edge moves forward in time as HS_{OUT} width is increased.
		3	Reserved	Set to 0
		4	$VSYNC_{OUT}$ Mode	0: $VSYNC_{OUT}$ is aligned to $HSYNC_{OUT}$ edge, providing “perfect” VSYNC signal (default). 1: $VSYNC_{OUT}$ is “raw” integrator output.
		5	Reserved	Set to 0
		6	Reserved	Set to 0
		7	VS_{OUT} Mode	0: VS_{OUT} is output on VS_{OUT} pin (default). 1: COAST (including pre- and post-coast COAST) is output on VS_{OUT} pin.
0x2B	Crystal Multiplier (0x14)	7:0	Crystal Multiplier	When using the ISL98001-275, the value in this register must need to be changed to achieve the maximum conversion rate (see “Initialization” on page 26. This register may also be adjusted to lower power consumption at slower pixel rates (see the “Reducing Power Dissipation” on page 26 for more information).

Technical Highlights

The ISL98001 provides all the features of traditional triple channel video AFEs, but adds several next-generation enhancements, bringing performance and ease of use to new levels.

DPLL

All video AFEs must phase lock to an HSYNC signal, supplied either directly or embedded in the video stream (Sync On Green). Historically this has been implemented as a traditional analog PLL. At SXGA and lower resolutions, an analog PLL solution has proven adequate, if somewhat troublesome (due to the need to adjust charge pump currents, VCO ranges and other parameters to find the optimum trade-off for a wide range of pixel rates).

As display resolutions and refresh rates have increased, however, the pixel period has shrunk. An XGA pixel at a 60Hz refresh rate has 15.4ns to change and settle to its new value. But at UXGA 75Hz, the pixel period is 4.9ns. Most consumer graphics cards (even the ones with “350MHz” DACs) spend most of that time slewing to the new pixel value. The pixel may settle to its final value with 1ns or less before it begins slewing to the next pixel. In many cases it rings and never settles at all. So precision, low-jitter sampling is a fundamental requirement at these speeds, and a difficult one for an analog PLL to meet.

The ISL98001's DPLL has less than 250ps of jitter, peak to peak, and independent of the pixel rate. The DPLL generates 64-phase steps per pixel (vs the industry standard 32), for fine, accurate positioning of the sampling point. The crystal-locked NCO inside the DPLL completely eliminates drift due to charge pump leakage, so there is inherently no frequency or phase change across a line. An intelligent all-digital loop filter/controller eliminates the need for the user to have to program or change anything (except for the number of pixels) to lock over a range from interlaced video (10MHz or higher) to UXGA 60Hz (170MHz, with the ISL98001-170).

The DPLL eliminates much of the performance limitations and complexity associated with noise-free digitization of high speed signals.

Automatic Black Level Compensation (ABLC™) and Gain Control

Traditional video AFEs have an offset DAC prior to the ADC, to both correct for offsets on the incoming video signals and add/subtract an offset for user “brightness control” without sacrificing the 8-bit dynamic range of the ADC. This solution is adequate, but it places significant requirements on the system's firmware, which must execute a loop that detects the black portion of the signal and then servos the offset DACs until that offset is nulled (or produces the desired ADC output code). Once this has been accomplished, the offset (both the offset in the AFE and the offset of the video card generating the signal) is subject to drift - the temperature inside a monitor or projector can easily change +50°C between power-on/offset calibration on a cold morning and the temperature reached once the monitor and the monitor's environment have reached steady state. Offset can drift significantly over +50°C, reducing image quality and requiring that the user do a manual calibration once the monitor has warmed up.

In addition to drift, many AFEs exhibit interaction between the offset and gain controls. When the gain is changed, the magnitude of the offset is changed as well. This again increases the complexity of the firmware as it tries to optimize gain and offset settings for a given video input signal. Instead of adjusting just the offset, then the gain, both have to be adjusted interactively until the desired ADC output is reached.

The ISL98001 simplifies offset and gain adjustment and completely eliminates offset drift using its Automatic Black Level Compensation (ABLC™) function. ABLC monitors the black level and continuously adjusts the ISL98001's 10-bit offset DACs to null out the offset. Any offset, whether due to the video source or the ISL98001's analog amplifiers, is eliminated with 10-bit (1/4 of an ADC LSB) accuracy. Any drift is compensated for well before it can have a visible effect. Manual offset adjustment control is still available - an 8-bit register allows the firmware to adjust the offset ±64 codes in exactly 1 ADC LSB increments. And gain is now completely independent of offset - adjusting the gain no longer affects the offset, so there is no longer a need to program the firmware to cope with interactive offset and gain controls.

Finally, there should be no concerns over ABLC itself introducing visible artifacts; it doesn't. ABLC functions at a very low frequency, changing the offset in 1/4 LSB increments, so it can't cause visible brightness fluctuations. And once ABLC is locked, if the offset doesn't drift, the DACs won't change. If desired, ABLC can be disabled, allowing the firmware to work in the traditional way, with 10-bit offset DACs under the firmware's control.

Gain and Offset Control

To simplify image optimization algorithms, the ISL98001 features fully-independent gain and offset adjustment. Changing the gain does not affect the DC offset, and the weight of an Offset DAC LSB does not vary depending on the gain setting.

The full-scale gain is set in the three 8-bit registers (0x06-0x08). The ISL98001 can accept input signals with amplitudes ranging from $0.35V_{P-P}$ to $1.4V_{P-P}$.

The offset controls shift the entire RGB input range, changing the input image brightness. Three separate registers provide independent control of the R, G, and B channels. Their nominal setting is 0x80, which forces the ADC to output code 0x00 (or 0x80 for the R (Pr) and B (Pb) channels in YPbPr mode) during the back porch period when ABLC is enabled.

Functional Description

Inputs

The ISL98001 digitizes analog video inputs in both RGB and Component (YPbPr) formats, with or without embedded sync (SOG).

RGB Inputs

For RGB inputs, the black/blank levels are identical and equal to 0V. The range for each color is typically 0V to 0.7V from black to white. HSYNC and VSYNC are separate signals.

Component YPbPr Inputs

In addition to RGB and RGB with SOG, the ISL98001 has an option that is compatible with the component YPbPr video inputs typically generated by DVD players. While the ISL98001 digitizes signals in these color spaces, it does not perform color space conversion; if it digitizes an RGB signal, it outputs digital RGB, while if it digitizes a YPbPr signal, it outputs digital YCbCr, also called YUV.

The Luminance (Y) signal is applied to the Green channel and is processed in a manner identical to the Green input with SOG described previously. The color difference signals Pb and Pr are bipolar and swing both above and below the black level. When the YPbPr mode is enabled, the black level output for the color difference channels shifts to a mid scale value of 0x80. Setting configuration register 0x05[2] = 1 enables the YPbPr signal processing mode of operation.

TABLE 1. YUV MAPPING (4:4:4)

INPUT SIGNAL	ISL98001 INPUT CHANNEL	ISL98001 OUTPUT ASSIGNMENT	OUTPUT SIGNAL
Y	Green	Green	$Y_0Y_1Y_2Y_3$
Pb	Blue	Blue	$U_0U_1U_2U_3$
Pr	Red	Red	$V_0V_1V_2V_3$

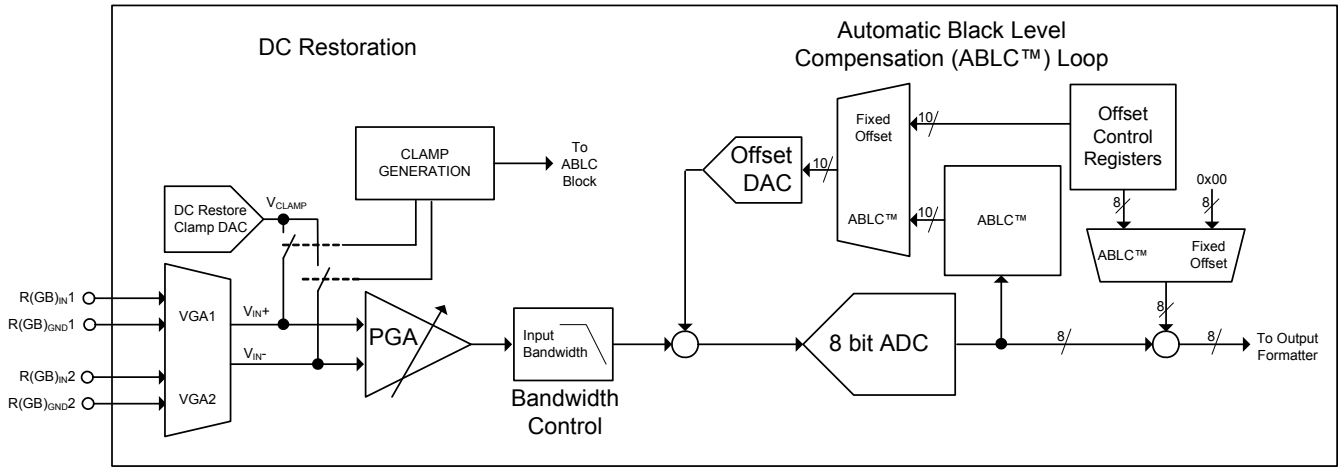


FIGURE 7. VIDEO FLOW (INCLUDING ABLC)

The ISL98001 can optionally decimate the incoming data to provide a 4:2:2 output stream (configuration register 0x18[4] = 1) as shown in Table 2.

TABLE 2. YUV MAPPING (4:2:2)

INPUT SIGNAL	ISL98001 INPUT CHANNEL	ISL98001 OUTPUT ASSIGNMENT	OUTPUT SIGNAL
Y	Green	Green	$Y_0Y_1Y_2Y_3$
Pb	Blue	Blue	driven low
Pr	Red	Red	$U_0V_0U_2V_2$

There is also a “compatibility mode”, enabled by setting bit 3 of register 0x18 to a 1, that outputs the U and V data with the format used by the previous generation (“X980xx”) series of AFEs, shown in Table 3.

TABLE 3. YUV MAPPING (4:2:2)

INPUT SIGNAL	ISL98001 INPUT CHANNEL	ISL98001 OUTPUT ASSIGNMENT	OUTPUT SIGNAL
Y	Green	Green	$Y_0Y_1Y_2Y_3$
Pb	Blue	Blue	driven low
Pr	Red	Red	$U_0V_1U_2V_3$

Input Coupling

Inputs can be either AC-coupled (default) or DC-coupled (See register 0x05[1]). AC coupling is usually preferred since it allows video signals with substantial DC offsets to be accurately digitized. The ISL98001 provides a complete internal DC-restore function, including the DC restore clamp (See Figure 7) and programmable clamp timing (registers 0x14, 0x15, 0x16, and 0x23).

When AC-coupled, the DC restore clamp is applied every line, a programmable number of pixels after the trailing edge of HSYNC. If register 0x05[5] = 0 (the default), the clamp will not be applied while the DPLL is coasting, preventing any clamp voltage errors from composite sync edges, equalization pulses, or Macrovision signals.

After the trailing edge of HSYNC, the DC restore clamp is turned on after the number of pixels specified in the DC Restore and ABLC Starting Pixel registers (0x14 and 0x15) has been reached. The clamp is applied for the number of pixels specified by the DC Restore Clamp Width Register (0x16). The clamp can be applied to the back porch of the video, or to the front porch (by increasing the DC Restore and ABLC Starting Pixel registers so all the active video pixels are skipped).

If DC-coupled operation is desired, the input to the ADC will be the difference between the input signal ($R_{IN}1$, for example) and that channel’s ground reference ($RGB_{GND}1$ in that example).

SOG

For component YPbPr signals, the sync signal is embedded on the Y channel’s video, which is connected to the green input, hence the name SOG (Sync on Green). The horizontal sync information is encoded onto the video input by adding the sync tip during the blanking interval. The sync tip level is typically 0.3V below the video black level.

To minimize the loading on the Green channel, the SOG input for each of the green channels should be AC-coupled to the ISL98001 through a series combination of a 10nF capacitor and a 500Ω resistor. Inside the ISL98001, a window comparator compares the SOG signal with an internal 4-bit programmable threshold level reference ranging from 0mV to 300mV below the minimum sync level. The SOG threshold level, hysteresis, and low-pass filter is programmed via register 0x04. If the Sync-On-Green function is not needed, the SOG_{IN} pin(s) may be left unconnected.

SYNC Processing

The ISL98001 can process sync signals from 3 different sources: discrete HSYNC and VSYNC, composite sync on

the HSYNC input, or composite sync from a Sync-On-Green (SOG) signal embedded on the Green video input. The ISL98001 has SYNC activity detect functions to help the firmware determine which sync source is available.

Macrovision

The ISL98001 automatically detects the presence of Macrovision-encoded video. When Macrovision is detected, it generates a mask signal that is ANDed with the incoming SOG CSYNC signal to remove the Macrovision before the HSYNC goes to the PLL. No additional programming is required to support Macrovision.

If desired (it is never necessary in normal operation), this function can be disabled by setting the Sync Mask Disable (register 0x05 bit 6) to a 1.

The mask signal is also applied to the $HSYNC_{OUT}$ signal. When Sync Mask Disable = 0, any Macrovision present on the incoming sync will not be visible on $HSYNC_{OUT}$. If the application requires the Macrovision pulses to be visible on $HSYNC_{OUT}$, set the $HSYNC_{OUT}$ Mask Disable bit (register 0x05 bit 7).

Headswitching from Analog Videotape Signals

Occasionally this AFE may be used to digitize signals coming from analog videotape sources. The most common example of this is a Digital VCR (which for best signal quality would be connected to this AFE with a component YPbPr connection). If the digital VCR is playing an older analog VHS tape, the sync signals from the VCR may contain the worst of the traditional analog tape artifacts: headswitching. Headswitching is traditionally the enemy of PLLs with large capture ranges, because a headswitch can cause the HSYNC period to change by as much as ±90%. To the PLL, this can look like a frequency change of -50% to greater than +900%, causing errors in the output frequency (and obviously the phase) to change. Subsequent HSYNCs have the correct, original period, but most analog PLLs will take dozens of lines to settle back to the correct frequency and phase after a headswitch disturbance. This causes the top of the image to “tear” during normal playback. In “trick modes” (fast forward and rewind), the HSYNC signal has multiple headswitch-like discontinuities, and many PLLs never settle to the correct value before the next headswitch, rendering the image completely unintelligible.

Intersil’s DPLL has the capability to correct large phase changes almost instantly by maximizing the phase error gain while keeping the frequency gain relatively low. This is done by changing the contents of register 0x1C to 0x4C. This increases the phase error gain to 100%. Because a phase setting this high will slightly increase jitter, the default setting (0x49) for register 0x1C is recommended for all other sync sources.

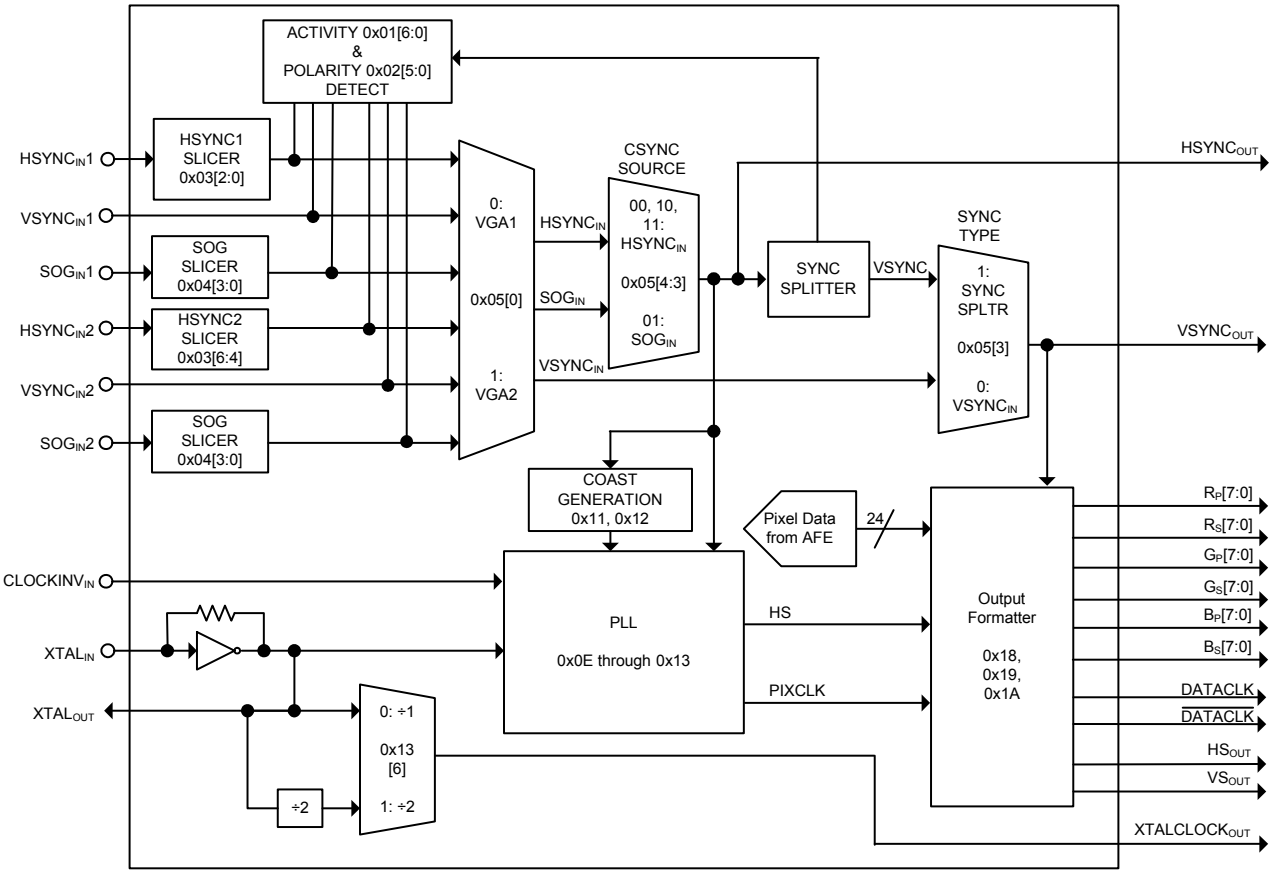


FIGURE 8. SYNC FLOW

PGA

The ISL98001's Programmable Gain Amplifier (PGA) has a nominal gain range from 0.5V/V (-6dB) to 2.0V/V (+6dB). The transfer function is in Equation 1:

$$\text{Gain}\left(\frac{V}{V}\right) = 0.5 + \frac{\text{GainCode}}{170} \quad \text{(EQ. 1)}$$

where GainCode is the value in the Gain register for that particular color. Note that for a gain of 1V/V, the GainCode should be 85 (0x55). This is a different center value than the 128 (0x80) value used by some other AFEs, so the firmware should take this into account when adjusting gains.

The PGAs are updated by the internal clamp signal once per line. In normal operation this means that there is a maximum delay of one HSYNC period between a write to a Gain register for a particular color and the corresponding change in that channel's actual PGA gain. If there is no regular HSYNC/SOG source, or if the external clamp option is enabled (register 0x13[5:4]) but there is no external clamp signal being generated, it may take up to 100ms for a write to the Gain register to update the PGA. This is not an issue in normal operation with RGB and YPbPr signals.

Bandwidth and Peaking Control

Register 0x0D[3:1] controls a low pass filter allowing the input bandwidth to be adjusted with three bit resolution between its default value (0x0E = 780MHz) and its minimum bandwidth (0x00, for 100MHz). Typically the higher the resolution, the higher the desired input bandwidth. To minimize noise, video signals should be digitized with the minimum bandwidth setting that passes sharp edges.

TABLE 4. BANDWIDTH CONTROL

0x0D[3:0] VALUE (LSB = "x" = "don't care")	AFE BANDWIDTH
000x	100MHz
001x	130MHz
010x	150MHz
011x	180MHz
100x	230MHz
101x	320MHz
110x	480MHz
111x	780MHz

Table 4 shows the corner frequencies for different register settings.

Register 0x0D[7:4] controls a programmable zero, allowing high frequencies to be boosted, restoring some of the harmonics lost due to excessive EMI filtering, cable losses, etc. This control has a very large range, and can introduce high frequency noise into the image, so it should be used judiciously, or as an advanced user adjustment.

TABLE 5. PEAKING CORNER FREQUENCIES

0X0D[7:4] VALUE	ZERO CORNER FREQUENCY
0x0	Peaking disabled
0x1	800MHz
0x2	400MHz
0x3	265MHz
0x4	200MHz
0x5	160MHz
0x6	135MHz
0x7	115MHz
0x8	100MHz
0x9	90MHz
0xA	80MHz
0xB	70MHz
0xC	65MHz
0xD	60MHz
0xE	55MHz
0xF	50MHz

Table 5 shows the corner frequency of the zero for different peaking register settings. Values above 0x2 may cause excessive noise, depending on the quality of the input signal and the PCB environment.

Offset DAC

The ISL98001 features a 10-bit Digital-to-Analog Converter (DAC) to provide extremely fine control over the full channel offset. The DAC is placed after the PGA to eliminate interaction between the PGA (controlling "contrast") and the Offset DAC (controlling "brightness").

In normal operation, the Offset DAC is controlled by the ABLC circuit, ensuring that the offset is always reduced to sub-LSB levels (See"Automatic Black Level Compensation (ABLC™)" on page 23). When ABLC is enabled, the Offset registers (0x09, 0x0A, 0x0B) control a digital offset added to or subtracted from the output of the ADC. This mode provides the best image quality and eliminates the need for any offset calibration.

If desired, ABLC can be disabled (0x17[0] = 1) and the Offset DAC programmed manually, with the 8 most

TABLE 6. OFFSET DAC RANGE AND OFFSET DAC ADJUSTMENT

OFFSET DAC RANGE 0X0C[0]	10-BIT OFFSET DAC RESOLUTION	ABLC 0x17[0]	USER OFFSET CONTROL RESOLUTION USING REGISTERS 0x09 - 0X0B ONLY (8-BIT OFFSET CONTROL)	USER OFFSET CONTROL RESOLUTION USING REGISTERS 0X09 - 0x0B AND 0X0C[7:2](10-BIT OFFSET CONTROL)
0	0.25 ADC LSBs (0.68mV)	0 (ABLC on)	1 ADC LSB (digital offset control)	N/A
1	0.125 ADC LSBs (0.34mV)	0 (ABLC on)	1 ADC LSB (digital offset control)	N/A
0	0.25 ADC LSBs (0.68mV)	1 (ABLC off)	1.0 ADC LSB (analog offset control)	0.25 ADC LSB (analog offset control)
1	0.125 ADC LSBs (0.34mV)	1 (ABLC off)	0.5 ADC LSB (analog offset control)	0.125 ADC LSB (analog offset control)

significant bits in registers 0x09, 0x0A, 0x0B, and the 2 least significant bits in register 0x0C[7:2].

The default Offset DAC range is ±127 ADC LSBs. Setting 0x0C[0] = 1 reduces the swing of the Offset DAC by 50%, making 1 Offset DAC LSB the weight of 1/8th of an ADC LSB. This provides the finest offset control and applies to both ABLC and manual modes.

Automatic Black Level Compensation (ABLC™)

ABLC is a function that continuously removes all offset errors from the incoming video signal by monitoring the offset at the output of the ADC and servoing the 10-bit analog DAC to force those errors to zero. When ABLC is enabled, the user offset control is a digital adder, with 8-bit resolution (refer to Table 6).

When the ABLC function is enabled (0x17[0] = 0), the ABLC function is executed every line after the trailing edge of HSYNC. If register 0x05[5] = 0 (the default), the ABLC function will be not be triggered while the DPLL is coasting, preventing any composite sync edges, equalization pulses, or Macrovision signals from corrupting the black data and potentially adding a small error in the ABLC accumulator.

After the trailing edge of HSYNC, the start of ABLC is delayed by the number of pixels specified in registers 0x14 and 0x15. After that delay, the number of pixels specified by register 0x17[3:2] are averaged together and added to the ABLC's accumulator. The accumulator stores the average black levels for the number of lines specified by register 0x17[6:4], which is then used to generate a 10-bit DAC value.

The default values provide excellent results with offset stability and absolute accuracy better than 1 ADC LSB for most input signals.

ADC

The ISL98001 features 3 fully differential, high-speed 8-bit ADCs.

Clock Generation

A Digital Phase Lock Loop (DPLL) is employed to generate the pixel clock frequency. The HSYNC input and the external XTAL provide a reference frequency to the PLL. The PLL then generates the pixel clock frequency that equal to the incoming HSYNC frequency times the HTOTAL value programmed into registers 0x0E and 0x0F.

The stability of the clock is very important and correlates directly with the quality of the image. During each pixel time transition, there is a small window where the signal is slewing from the old pixel amplitude and settling to the new pixel value. At higher frequencies, the pixel time transitions at a faster rate, which makes the stable pixel time even smaller. Any jitter in the pixel clock reduces the effective stable pixel time and thus the sample window in which pixel sampling can be made accurately.

Sampling Phase

The ISL98001 provides 64 low-jitter phase choices per pixel period, allowing the firmware to precisely select the optimum sampling point. The sampling phase register is 0x10.

External Pixel Clock

The ISL98001 can bypass the PLL and use an external clock signal to drive the ADCs but when this is done the programmable sample phase is not available. When bits [5:4] of register 0x13 are set to 11 a clock signal on the $CLOCKINV_{IN}$ pin is used.

HSYNC Slicer

To further minimize jitter, the HSYNC inputs are treated as analog signals, and brought into a precision slicer block with thresholds programmable in 400mV steps with 240mV of hysteresis, and a subsequent digital glitch filter that ignores any HSYNC transitions within 100ns of the initial transition. This processing greatly increases the AFE's rejection of ringing and reflections on the HSYNC line and allows the AFE to perform well even with pathological HSYNC signals.

Voltages given above and in the HSYNC Slicer register description are with respect to a 3.3V sync signal at the $HSYNC_{IN}$ input pin. To achieve 5V compatibility, a 680Ω series resistor should be placed between the HSYNC source and the $HSYNC_{IN}$ input pin. Relative to a 5V input, the hysteresis will be 240mV*5V/3.3V = 360mV, and the slicer step size will be 400mV*5V/3.3V = 600mV per step.

TABLE 7. SYNC SOURCE DETECTION TABLE

HSYNC DETECT	VSYNC DETECT	SOG DETECT	TRILEVEL DETECT	RESULT
1	1	X	X	Sync is on HSYNC and VSYNC
1	0	X	X	Sync is composite sync on HSYNC. Set Input configuration register to CSYNC on HSYNC and confirm that CSYNC detect bit is set.
0	0	1	0	Sync is composite sync on SOG. It is possible that trilevel sync is present but amplitude is too low to set trilevel detect bit. Use video mode table to determine if this video mode is likely to have trilevel sync, and set clamp start, width values appropriately if it is.
0	0	1	1	Sync is composite sync on SOG. Sync is likely to be trilevel.
0	0	0	X	No valid sync sources on any input.

SOG Slicer

The SOG input has programmable threshold, 40mV of hysteresis, and an optional low pass filter that can be used to remove high frequency video spikes (generated by overzealous video peaking in a DVD player, for example) that can cause false SOG triggers. The SOG threshold sets the comparator threshold relative to the sync tip (the bottom of the SOG pulse).

SYNC Status and Polarity Detection

The SYNC Status register (0x01) and the SYNC Polarity register (0x02) continuously monitor all 6 sync inputs ($VSYNC_{IN}$, $HSYNC_{IN}$, and SOG_{IN} for each of 2 channels) and report their status. However, accurate sync activity detection is always a challenge. Noise and repetitive video patterns on the Green channel may look like SOG activity when there actually is no SOG signal, while non-standard SOG signals and trilevel sync signals may have amplitudes below the default SOG slicer levels and not be easily detected. As a consequence, not all of the activity detect bits in the ISL98001 are correct under all conditions.

Table 7 shows how to use the SYNC Status register (0x01) to identify the presence of and type of a sync source. The firmware should go through the table in the order shown, stopping at the first entry that matches the activity indicators in the SYNC Status register.

Final validation of composite sync sources (SOG or Composite sync on HSYNC) should be done by setting the Input Configuration register (0x05) to the composite sync source determined by this table, and confirming that the CSYNC detect bit is set.

The accuracy of the Trilevel Sync detect bit can be increased by multiple reads of the Trilevel Sync detect bit. See the **Trilevel Sync Detect** section for more details.

For best SOG operation, the SOG low pass filter (register 0x04[4] should always be enabled to reject the high frequency peaking often seen on video signals.

HSYNC and VSYNC Activity Detect

Activity on these bits always indicates valid sync pulses, so they should have the highest priority and be used even if the SOG activity bit is also set.

SOG Activity Detect

The SOG activity detect bit monitors the output of the SOG slicer, looking for 64 consecutive pulses with the same period and duty cycle. If there is no signal on the Green (or Y) channel, the SOG slicer will clamp the video to a DC level and will reject any sporadic noise. There should be no false positive SOG detects if there is no video on Green (or Y).

If there is video on Green (or Y) with no valid SOG signal, the SOG activity detect bit may sometimes report false positives (it will detect SOG when no SOG is actually present). This is due to the presence of video with a repetitive pattern that creates a waveform similar to SOG. For example, the desktop of a PC operating system is black during the front porch, horizontal sync, and back porch, then increases to a larger value for the video portion of the screen. This creates a repetitive video waveform very similar to SOG that may falsely trigger the SOG Activity detect bit. However, in these cases where there is active video without SOG, the SYNC information will be provided either as separate H and V sync on $HSYNC_{IN}$ and $VSYNC_{IN}$, or composite sync on $HSYNC_{IN}$. $HSYNC_{IN}$ and $VSYNC_{IN}$ should therefore be used to qualify SOG. The SOG Active bit should only be considered valid if HSYNC Activity Detect = 0. Note: Some pattern generators can output HSYNC and SOG simultaneously, in which case both the HSYNC and the SOG activity bits will be set, and valid. Even in this case, however, the monitor should still choose HSYNC over SOG.

TriLevel Sync Detect

Unlike SOG detect, the TriLevel Sync detect function does not check for 64 consecutive trilevel pulses in a row, and is therefore less robust than the SOG detect function. It will report false positives for SOG-less video for the same reasons the SOG activity detect does, and should therefore be qualified with both HSYNC and SOG. TriLevel Sync Detect should only be considered valid if HSYNC Activity Detect = 0 and SOG Activity Detect = 1.

If there is a SOG signal, the TriLevel Detect bit will operate correctly for standard trilevel sync levels ($600mV_{P-P}$). In some real-world situations, the peak-to-peak sync amplitude

may be significantly smaller, sometimes 300mV$_{P-P}$ or less. In these cases the sync slicer will continue to operate correctly, but the TriLevel Detect bit may not be set. Trilevel detection accuracy can be enhanced by polling the trilevel bit multiple times. If HSYNC is inactive, SOG is present, and the TriLevel Sync Detect bit is read as a 1, there is a high likelihood there is trilevel sync.

CSYNC Present

If a composite sync source (either CSYNC on HSYNC or SOG) is selected through bits 3 and 4 of register 0x05, the CSYNC Present bit in register 0x01 should be set. CSYNC Present detects the presence of a low frequency, repetitive signal inside HSYNC, which indicates a VSYNC signal. The CSYNC Present bit should be used to confirm that the signal being received is a reliable composite sync source.

SYNC Output Signals

The ISL98001 has 2 pairs of HSYNC and VSYNC output signals, HSYNC$_{OUT}$ and VSYNC$_{OUT}$, and HS$_{OUT}$ and VS$_{OUT}$.

HSYNC$_{OUT}$ and VSYNC$_{OUT}$ are buffered versions of the incoming sync signals; no synchronization is done. These signals are used for mode detection

HS$_{OUT}$ and VS$_{OUT}$ are generated by the ISL98001's logic and are synchronized to the output DATACLK and the digital pixel data on the output databus. HS$_{OUT}$ is used to signal the start of a new line of digital data. VS$_{OUT}$ is not needed in most applications.

Both HSYNC$_{OUT}$ and VSYNC$_{OUT}$ (including the sync separator function) remain active in power-down mode. This allows them to be used in conjunction with the Sync Status registers to detect valid video without powering up the ISL98001.

HSYNC$_{OUT}$

HSYNC$_{OUT}$ is an unmodified, buffered version of the incoming HSYNC$_{IN}$ or SOG$_{IN}$ signal of the selected channel, with the incoming signal's period, polarity, and width to aid in mode detection. HSYNC$_{OUT}$ will be the same format as the incoming sync signal: either horizontal or composite sync. If a SOG input is selected, HSYNC$_{OUT}$ will output the entire SOG signal, including the VSYNC portion, pre-/post-equalization pulses if present, and Macrovision pulses if present. HSYNC$_{OUT}$ remains active when the ISL98001 is in power-down mode. HSYNC$_{OUT}$ is generally used for mode detection.

VSYNC$_{OUT}$

VSYNC$_{OUT}$ is an unmodified, buffered version of the incoming VSYNC$_{IN}$ signal of the selected channel, with the original VSYNC period, polarity, and width to aid in mode detection. If a SOG input is selected, this signal will output the VSYNC signal extracted by the ISL98001's sync slicer. Extracted VSYNC will be the width of the embedded VSYNC pulse plus pre- and post-equalization pulses (if present). Macrovision pulses from an NTSC DVD source will lengthen the width of the VSYNC pulse. Macrovision pulses from other sources (PAL DVD or videotape) may appear as a second VSYNC pulse encompassing the width of the Macrovision. See the Macrovision section for more information. VSYNC$_{OUT}$ (including the sync separator function) remains active in power-down mode. VSYNC$_{OUT}$ is generally used for mode detection, start of field detection, and even/odd field detection.

HS$_{OUT}$

HS$_{OUT}$ is generated by the ISL98001's control logic and is synchronized to the output DATACLK and the digital pixel data on the output databus. Its trailing edge is aligned with pixel 0. Its width, in units of pixels, is determined by register 0x19, and its polarity is determined by register 0x18[7]. As the width is increased, the trailing edge stays aligned with pixel 0, while the leading edge is moved backwards in time relative to pixel 0. HS$_{OUT}$ is used by the scaler to signal the start of a new line of pixels.

The HS$_{OUT}$ Width register (0x19) controls the width of the HS$_{OUT}$ pulse. The pulse width is nominally 1 pixel clock period times the value in this register. In the 48 bit output mode (register 0x18[0] = 1), or the YPbPr input mode (register 0x05[2] = 1), the HS$_{OUT}$ width is incremented in 2 pixel clock (1 DATACLK) increments (see Table 8).

TABLE 8. HS$_{OUT}$ WIDTH

	HS$_{OUT}$ WIDTH (PIXEL CLOCKS)		
REGISTER 0x19 VALUE	**24-BIT MODE, RGB**	**24-BIT MODE, YPbPr**	**ALL 48-BIT MODES**
0	0	1	0
1	1	1	0
2	2	3	2
3	3	3	2
4	4	5	4
5	5	5	4
6	6	7	6
7	7	7	6

VS$_{OUT}$

VS$_{OUT}$ is generated by the ISL98001's control logic and is synchronized to the output DATACLK and the digital pixel data on the output databus. Its leading and trailing edges are aligned with pixel 7 (8 pixels after HSYNC trailing edge). Its width, in units of lines, is equal to the width of the incoming VSYNC (See the VSYNC$_{OUT}$ description). Its polarity is determined by register 0x18[6]. Note: *This output is not needed in most applications. Intersil strongly discourages using this signal - use VSYNC$_{OUT}$ instead.*

Crystal Oscillator

An external 22MHz to 27MHz crystal supplies the low-jitter reference clock to the DPLL. The absolute frequency of this crystal within this range is unimportant, as is the crystal's temperature coefficient, allowing use of less expensive, lower-grade crystals.

As an alternative to a crystal, the $XTAL_{IN}$ pin can be driven with a 3.3V CMOS-level external clock source at any frequency between 22MHz and 33.5MHz. The ISL98001's jitter specification assumes a low-jitter crystal source. If the external clock source has increased jitter, the sample clock generated by the DPLL may exhibit increased jitter as well.

Reset

The ISL98001 has a Power On Reset (POR) function that resets the chip to its default state when power is initially applied, including resetting all the registers to their default settings as described in the Register Listing. The external $\overline{RESET}$ pin duplicates the reset function of the POR without having to cycle the power supplies. The $\overline{RESET}$ pin does not need to be used in normal operation and can be tied high.

Initialization

The ISL98001 initializes with default register settings for an AC-coupled, 640x480 RGB input on the VGA1 channel, with a 24-bit output. An input signal meeting these conditions will be output on the databus without writing to any of the configuration registers. The configuration registers will need to be changed as required to support other resolutions, different input channels, different sync sources, phase optimization etc.

The ISL98001-275 requires one additional register write to operate at their maximum speed. The ISL98001 generates an internal reference clock equal to the crystal frequency times the value in register 0x2B (nominally 0x14 or 20 decimal). The typical value of this clock is therefore 500MHz (25MHz*20). The minimum value of this clock is 360MHz.

This internal clock needs to be greater than 2 times the PLL pixel rate. The nominal value of 500MHz therefore supports pixel rates up to 250MHz. To achieve pixel rates of 275MHz, or to work with lower frequency crystals, the multiplier in register 0x2B must be programmed using Equation 2:

$$0x2B\ value = INT\left(2\frac{f_{MAX\_PIXELCLK}}{f_{CRYSTAL}}\right) + 1 \qquad \text{(EQ. 2)}$$

For example, if the maximum pixel clock is 263MHz (QXGA), and the crystal frequency is 24MHz, then register 0x2B should be set to 1 + INT(2*263/24) = 1 + INT(21.917) = 1 + 21 = 22 = 0x16. Table 9 illustrates the compensation values required to operate the ISL98001-275 at its maximum speed of 275MHz. If lower maximum Pixel Clock frequencies are needed, using the formula above to reduce the value of register 0x2B will reduce power consumption.

TABLE 9. CRYSTAL MULTIPLIER FOR 275MHz PIXEL RATE

CRYSTAL FREQUENCY RANGE (MHz)	REGISTER 0x2B VALUE	
	DECIMAL	HEX
23 to 23.9	24	0x18
23.9 to 25	23	0x17
25.0 to 26.2	22	0x16
26.2 to 27	21	0x15

Reducing Power Dissipation

It is possible to reduce the total power consumption of the ISL98001 in applications where power is a concern. There are several techniques that can be used to reduce power consumption:

- **Internal Digital Voltage Regulator.** The ISL98001 features a 3.3V to 1.9V voltage regulator (pins $VREG_{IN}$ and $VREG_{OUT}$) for the low voltage digital supply. This regulator typically sources 100mA at 1.9V, dissipating up to 140mW in heat. Providing an external, clean 1.8V supply to the V_{CORE}, V_{PLL}, and $V_{COREADC}$ will substantially reduce power dissipation. The external 1.8V supply should ramp up after (or at the same time as) the digital 3.3V (V_D) supply.
- **Internal Analog Voltage Regulator.** The ISL98001 also features a 3.3V to 1.9V voltage regulator for the low voltage analog supply. This voltage appears on the V_{BYPASS} pins. Unlike the digital low voltage supply, there are no "in" and "out" connections for this regulator. However, this internal regulator can only source voltage, and can be effectively bypassed by driving the V_{BYPASS} pins with an external, clean 2.0V supply. The external 2.0V supply should ramp up after (or at the same time as) the analog 3.3V (V_A) supply.
- **Buffering Digital Outputs.** Switching 24 or 48 data output pins into a capacitive bus can consume significant current. The higher the capacitance on the external databus, the higher the switching current. To minimize current consumption inside the ISL98001, minimize bus capacitance and/or insert data buffers such as the SN64AVC16827 between the ISL98001's data outputs and the external databus.
- **Internal Reference Frequency.** The crystal frequency is multiplied by the value in register 0x2B to generate an internal high frequency reference clock. For pixel rates up to 160MHz, this internal frequency should be set to 400MHz ±10% for minimum power consumption. For example, for a 33MHz frequency at $XTAL_{IN}$, register 0x2B should be set to a value of 0x0C to minimize power. For pixel rates greater than 160MHz, the register 0x2B value should be set using Equation 2 in the "Initialization" section on page 26.

Standby Mode

The ISL98001 can be placed into a low power standby mode by writing a 0x0F to register 0x1B, powering down the triple ADCs, the DPLL, and most of the internal clocks.

To allow input monitoring and mode detection during power-down, the following blocks remain active:

- Serial interface (including the crystal oscillator) to enable register read/write activity
- Activity and polarity detect functions (registers 0x01 and 0x02)
- The $HSYNC_{OUT}$ and $VSYNC_{OUT}$ pins (for mode detection)

EMI Considerations

There are two possible sources of EMI on the ISL98001:

Crystal oscillator. The EMI from the crystal oscillator is negligible. This is due to an amplitude-regulated, low voltage sine wave oscillator circuit, instead of the typical high-gain square wave inverter-type oscillator, so there are no harmonics. Note: The crystal oscillator is not a significant source of EMI.

Digital output switching. This is the largest potential source of EMI. However, the EMI is determined by the PCB layout and the loading on the databus. The way to control this is to put series resistors on the output of all the digital pins (as our demo board and reference circuits show). These resistors should be as large as possible, while still meeting the setup and hold timing requirements of the scaler. We recommend starting with 22Ω. If the databus is heavily loaded (long traces, many other part on the same bus), this value may need to be reduced. If the databus is lightly loaded, it may be increased.

Intersil's recommendations to minimize EMI are:

- Minimize the databus trace length
- Minimize the databus capacitive loading.

If EMI is a problem in the final design, increase the value of the digital output series resistors to reduce slew rates on the bus. This can only be done as long as the scaler's setup and hold timing requirements continue to be met.

ISL98001 Serial Communication

Overview

The ISL98001 uses a 2-wire serial bus for communication with its host. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

1) The Host selects the ISL98001 it wishes to communicate with.
2) The Host writes the initial ISL98001 Configuration Register address it wishes to write to or read from.
3) The Host writes to or reads from the ISL98001's Configuration Register. The ISL98001's internal address pointer auto increments, so to read registers 0x00 through 0x1B, for example, one would write 0x00 in step 2, then repeat step three 28 times, with each read returning the next register value.

The ISL98001 has a 7-bit address on the serial bus. The upper 6-bits are permanently set to 100110, with the lower bit determined by the state of pin 48 (SADDR). This allows two ISL98001s to be independently controlled while sharing the same bus.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 9). The ISL98001 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a R/$\overline{W}$ bit, indicating if the next transaction will be a Read (R/$\overline{W}$ = 1) or a Write (R/$\overline{W}$ = 0). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 10).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 9), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Data on the serial bus must be valid for the entire time SCL is high (Figure 11). To achieve this, data being written to the ISL98001 is latched on a delayed version of the rising edge of SCL. SCL is delayed and deglitched inside the ISL98001 for three crystal clock periods (120ns for a 25MHz crystal) to eliminate spurious clock pulses that could disrupt serial communication.

When the contents of the ISL98001 are being read, the SDA line is updated after the falling edge of SCL, delayed and deglitched in the same manner.

Configuration Register Write

Figure 12 shows two views of the steps necessary to write one or more words to the Configuration Register.

Configuration Register Read

Figure 13 shows two views of the steps necessary to read one or more words from the Configuration Register.

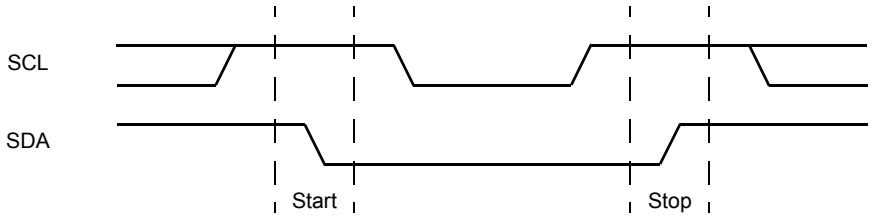


FIGURE 9. VALID START AND STOP CONDITIONS

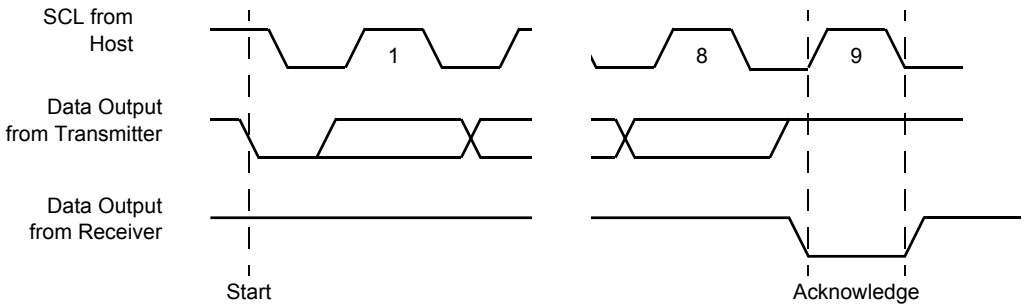


FIGURE 10. ACKNOWLEDGE RESPONSE FROM RECEIVER

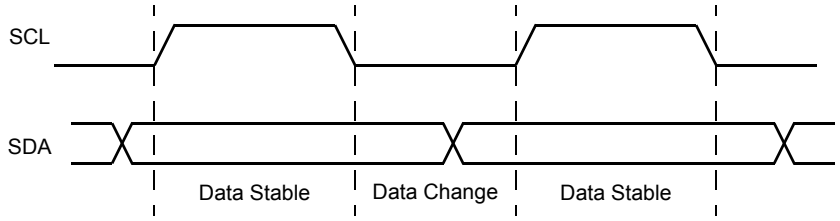
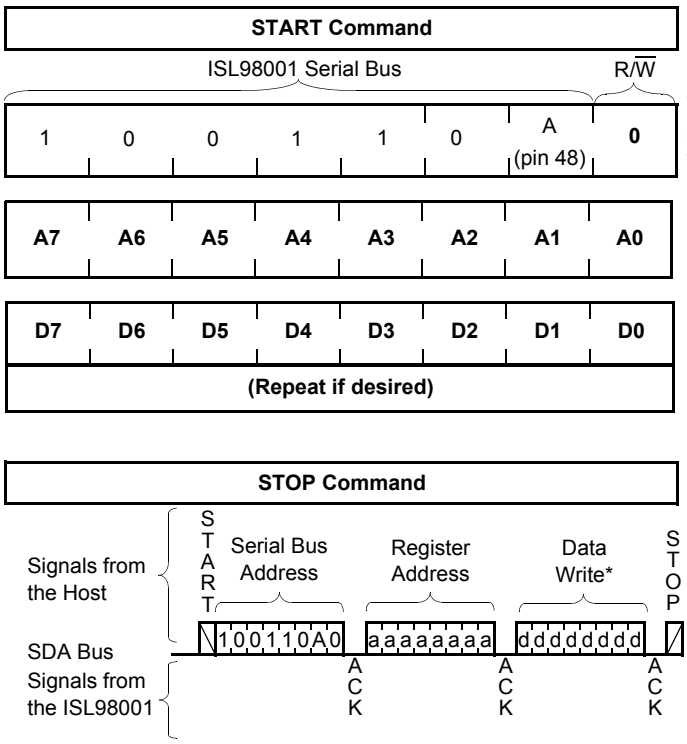


FIGURE 11. VALID DATA CHANGES ON THE SDA BUS



Signals the beginning of serial I/O

ISL98001 Serial Bus Address Write

This is the 7-bit address of the ISL98001 on the 2-wire bus. The address is 0x4C if pin 48 is low, 0x4D if pin 48 is high. Shift this value left to when adding the R/W bit.

ISL98001 Register Address Write

This is the address of the ISL98001's configuration register that the following byte will be written to.

ISL98001 Register Data Write(s)

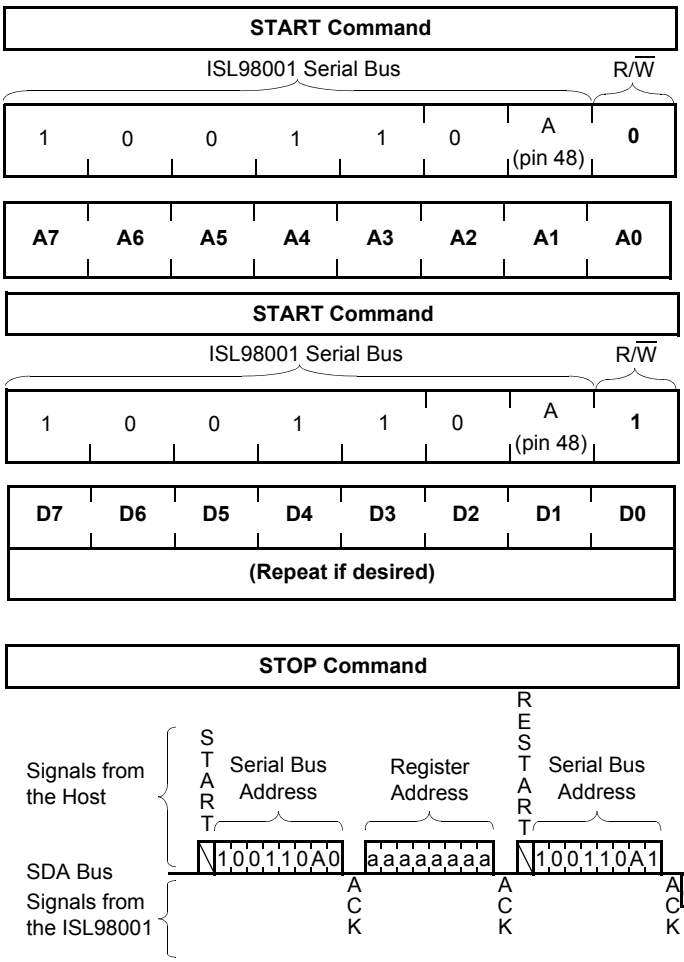
This is the data to be written to the ISL98001's configuration register.

Note: The ISL98001's Configuration Register's address pointer auto increments after each data write: repeat this step to write multiple sequential bytes of data to the Configuration Register.

Signals the ending of serial I/O

* The data write step may be repeated to write to the ISL98001's Configuration Register sequentially, beginning at the Register Address written in the previous step.

FIGURE 12. CONFIGURATION REGISTER WRITE



Signals the beginning of serial I/O

ISL98001 Serial Bus Address Write

This is the 7-bit address of the ISL98001 on the 2-wire bus. The address is 0x4C if pin 48 is low, 0x4D if pin 48 is high. R/$\overline{W}$ = 0, indicating next transaction will be a write.

ISL98001 Register Address Write

This sets the initial address of the ISL98001's configuration register for subsequent reading.

Ends the previous transaction and starts a new one

ISL98001 Serial Bus Address Write

This is the 7-bit address of the ISL98001 on the 2-wire bus. The address is 0x4C if pin 48 is low, 0x4D if pin 48 is high. R/$\overline{W}$ = 1, indicating next transaction(s) will be a read.

ISL98001 Register Data Read(s)

This is the data read from the ISL98001's configuration register.

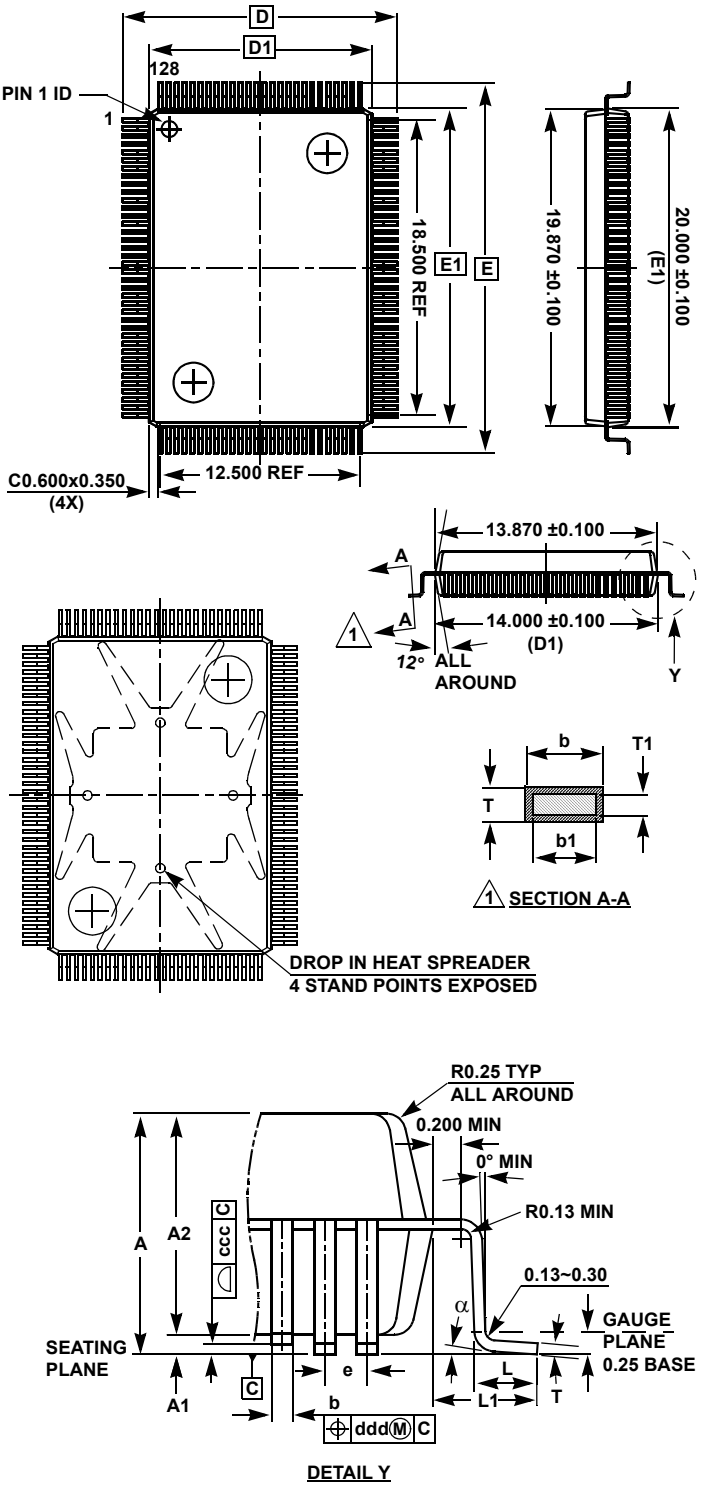
Note: The ISL98001's Configuration Register's address pointer auto increments after each data read: repeat this step to read multiple sequential bytes of data from the Configuration Register.

Signals the ending of serial I/O

* The data read step may be repeated to read from the ISL98001's Configuration Register sequentially, beginning at the Register Address written in the two steps previous.

FIGURE 13. CONFIGURATION REGISTER READ

Metric Plastic Quad Flatpack Packages (MQFP)



MDP0055

14x20mm 128 LEAD MQFP (WITH AND WITHOUT HEAT SPREADER) 3.2mm FOOTPRINT

SYMBOL	DIMENSIONS (MILLIMETERS)	REMARKS
A	Max 3.40	Overall height
A1	0.250~0.500	Standoff
A2	2.750 ±0.250	Package thickness
α	0°~7°	Foot angle
b	0.220 ±0.050	Lead width (1)
b1	0.200 ±0.030	Lead base metal width (1)
D	17.200 ±0.250	Lead tip to tip
D1	14.000 ±0.100	Package length
E	23.200 ±0.250	Lead tip to tip
E1	20.000 ±0.100	Package width
e	0.500 Base	Lead pitch
L	0.880 ±0.150	Foot length
L1	1.600 Ref.	Lead length
T	0.170 ±0.060	Frame thickness (1)
T1	0.152 ±0.040	Frame base metal thickness (1)
ccc	0.100	Foot coplanarity
ddd	0.100	Foot position

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NOTES:

1. General tolerance: Distance ±0.100, Angle +2.5°.
2. (1) Matte finish on package body surface except ejection and pin 1 marking (Ra 0.8~2.0um).
3. All molded body sharp corner RADII unless otherwise specified (Max RO.200).
4. Package/Leadframe misalignment (X, Y): Max. 0.127
5. Top/Bottom misalignment (X, Y): Max. 0.127
6. Drawing does not include plastic or metal protrusion or cutting burr.
7. (2) Compliant to JEDEC MS-022.