Ultralow Noise BiFET Op Amp

AD743

FEATURES

Ultralow Noise Performance
- 2.9 nV/√Hz at 10 kHz
- 0.38 μV p-p, 0.1 Hz to 10 Hz
- 6.9 fA/√Hz Current Noise at 1 kHz

Excellent DC Performance
- 0.5 mV Max Offset Voltage
- 250 pA Max Input Bias Current
- 1000 V/mV Min Open-Loop Gain

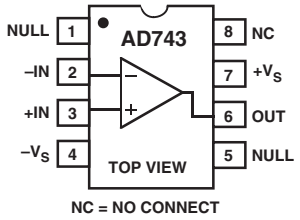
AC Performance
- 2.8 V/μs Slew Rate
- 4.5 MHz Unity-Gain Bandwidth
- THD = 0.0003% @ 1 kHz
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

- Sonar Preamplifiers
- High Dynamic Range Filters (>140 dB)
- Photodiode and IR Detector Amplifiers
- Accelerometers

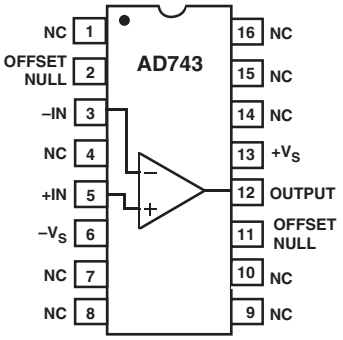
CONNECTION DIAGRAMS

8-Lead PDIP (N)



NC = NO CONNECT

16-Lead SOIC (R)



NC = NO CONNECT

GENERAL DESCRIPTION

The AD743 is an ultralow noise, precision, FET input, monolithic operational amplifier. It offers a combination of the ultralow voltage noise generally associated with bipolar input op amps and the very low input current of a FET input device. Furthermore, the AD743 does not exhibit an output phase reversal when the negative common-mode voltage limit is exceeded.

The AD743's guaranteed, maximum input voltage noise of 4.0 nV/√Hz at 10 kHz is unsurpassed for a FET input monolithic op amp, as is the maximum 1.0 μV p-p, 0.1 Hz to 10 Hz noise. The AD743 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The AD743 is specifically designed for use as a preamp in capacitive sensors, such as ceramic hydrophones. The AD743J is rated over the commercial temperature range of 0°C to 70°C.

The AD743 is available in a 16-lead SOIC and 8-lead PDIP.

PRODUCT HIGHLIGHTS

1. The low offset voltage and low input offset voltage drift of the AD743 coupled with its ultralow noise performance mean that the AD743 can be used for upgrading many applications now using bipolar amplifiers.
2. The combination of low voltage and low current noise make the AD743 ideal for charge sensitive applications such as accelerometers and hydrophones.
3. The low input offset voltage and low noise level of the AD743 provide >140 dB dynamic range.
4. The typical 10 kHz noise level of 2.9 nV/√Hz permits a three op amp instrumentation amplifier, using three AD743s, to be built which exhibits less than 4.2 nV/√Hz noise at 10 kHz and which has low input bias currents.

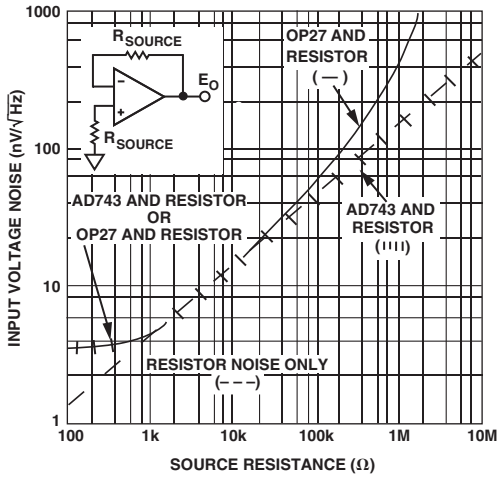


Figure 1. Input Voltage Noise vs. Source Resistance

REV. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD743–SPECIFICATIONS (@ 25°C and ±15 V dc, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT OFFSET VOLTAGE[1]					
Initial Offset			0.25	1.0	mV
Initial Offset	T_{MIN} to T_{MAX}			1.5	mV
vs. Temperature	T_{MIN} to T_{MAX}		2		µV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		dB
vs. Supply (PSRR)	T_{MIN} to T_{MAX}	88			dB
INPUT BIAS CURRENT[3]					
Either Input	V_{CM} = 0 V		150	400	pA
Either Input @ T_{MAX}	V_{CM} = 0 V			8.8	nA
Either Input	V_{CM} = 10 V		250	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V			2.2	nA
FREQUENCY RESPONSE					
Gain BW, Small Signal	G = –1		4.5		MHz
Full Power Response	V_O = 20 V p-p		25		kHz
Slew Rate, Unity Gain	G = –1		2.8		V/µs
Settling Time to 0.01%			6		µs
Total Harmonic Distortion[4]	f = 1 kHz				
(TPC 16)	G = –1		0.0003		%
INPUT IMPEDANCE					
Differential			$1 \times 10^{10} \| 20$		Ω‖pF
Common Mode			$3 \times 10^{11} \| 18$		Ω‖pF
INPUT VOLTAGE RANGE					
Differential[5]			±20		V
Common-Mode Voltage			+13.3, –10.7		V
Over Maximum Operating Range[6]		–10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		dB
	T_{MIN} to T_{MAX}	78			dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.38		µV p-p
	f = 10 Hz		5.5		nV/√Hz
	f = 100 Hz		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9		fA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V,				
	R_{LOAD} ≥ 2 kΩ	1000	4000		V/mV
	T_{MIN} to T_{MAX}	800			V/mV
	R_{LOAD} = 600 Ω	1200			V/mV
OUTPUT CHARACTERISTICS					
Voltage	R_{LOAD} ≥ 600 Ω	+13, –12			V
	R_{LOAD} ≥ 600 Ω		+13.6, –12.6		V
	T_{MIN} to T_{MAX}	+12, –10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, –13.1		V
Current	Short Circuit	20	40		mA
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±4.8		±18	V
Quiescent Current			8.1	10.0	mA
TRANSISTOR COUNT	No. of Transistors		50		

NOTES

[1]Input offset voltage specifications are guaranteed after five minutes of operation at T_A = 25°C.

[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V; and $+V_S$ = 12 V to 18 V, $-V_S$ = 15 V.

[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = 25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –1, R_L = 2 kΩ, C_L = 10 pF.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.

[6]The AD743 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range
AD743J . . . . . 0°C to 70°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] 8-lead PDIP: θ_{JA} = 100°C/W, θ_{JC} = 30°C/W.
16-lead SOIC: θ_{JA} = 100°C/W, θ_{JC} = 30°C/W.

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL-STD-883C has been performed on the AD743. The AD743 is a Class 1 device, passing at 1000 V and failing at 1500 V on null Pins 1 and 5, when tested, using an IMCS 5000 automated ESD tester. Pins other than null pins fail at greater than 2500 V.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD743JN	0°C to 70°C	N-8
AD743JR-16	0°C to 70°C	R-16
AD743JR-16-REEL	0°C to 70°C	Tape and Reel
AD743JR-16-REEL7	0°C to 70°C	Tape and Reel

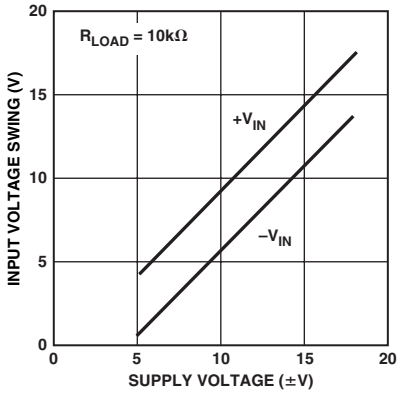
*N = PDIP; R = SOIC.

CAUTION

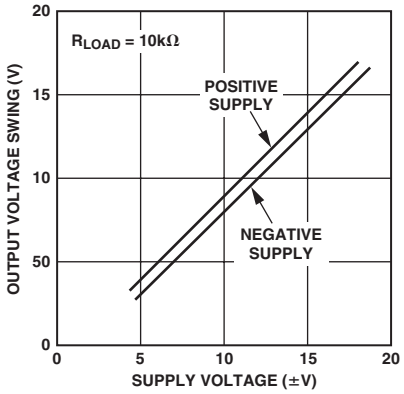
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD743 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD743–Typical Performance Characteristics

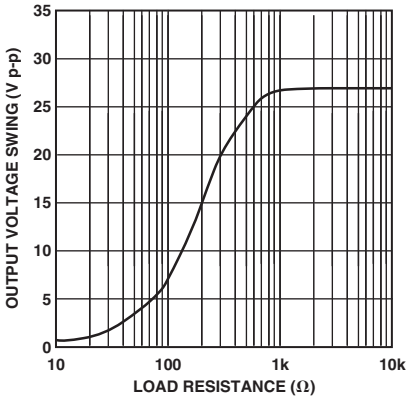
(@ 25°C, V_S = 15 V)



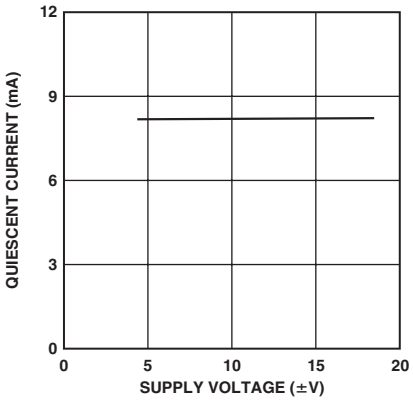
TPC 1. Input Voltage Swing vs. Supply Voltage



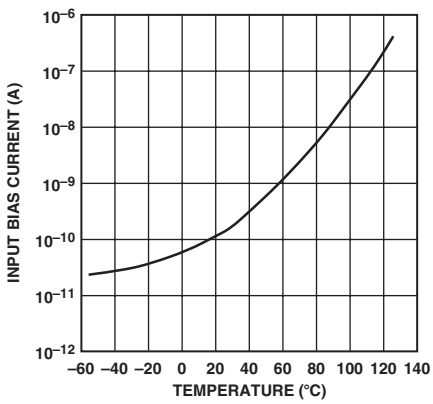
TPC 2. Output Voltage Swing vs. Supply Voltage



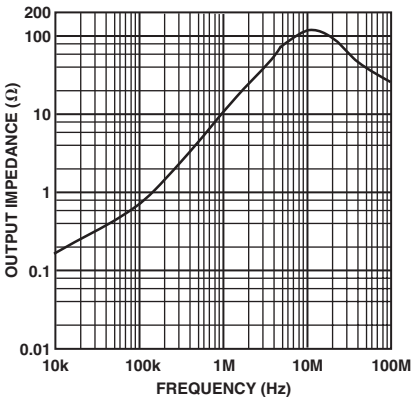
TPC 3. Output Voltage Swing vs. Load Resistance



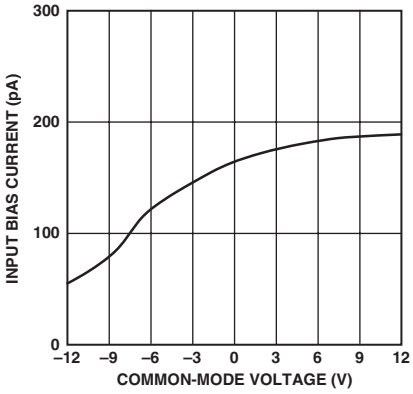
TPC 4. Quiescent Current vs. Supply Voltage



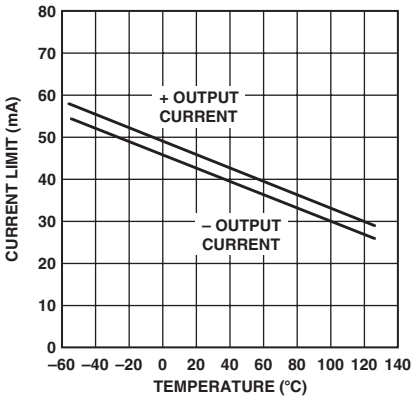
TPC 5. Input Bias Current vs. Temperature



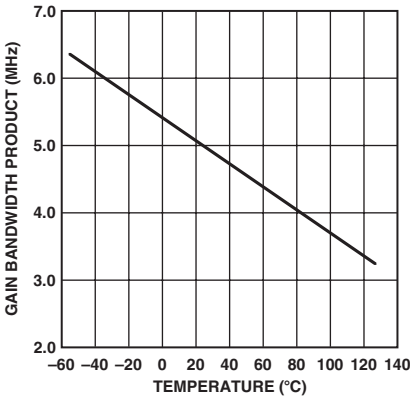
TPC 6. Output Impedance vs. Frequency (Closed-Loop Gain = –1)



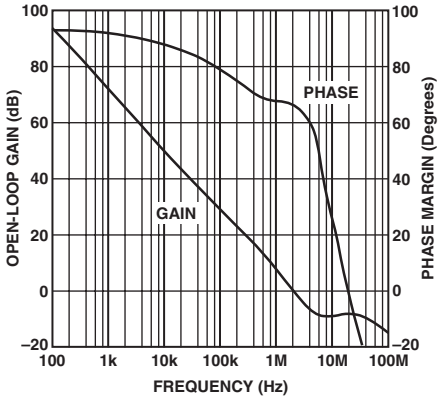
TPC 7. Input Bias Current vs. Common-Mode Voltage



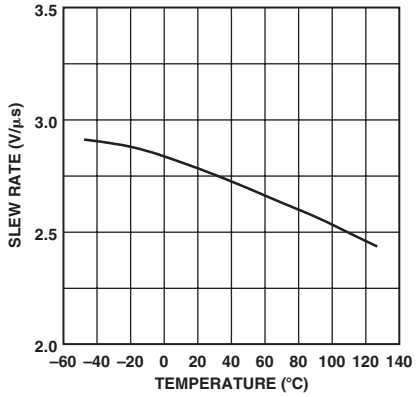
TPC 8. Short Circuit Current Limit vs. Temperature



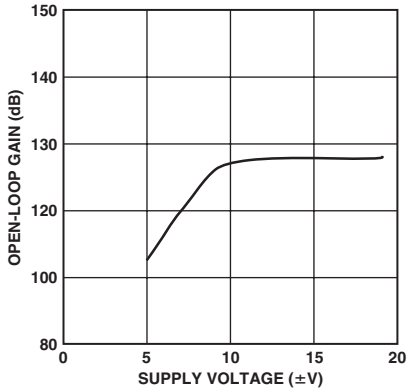
TPC 9. Gain Bandwidth Product vs. Temperature



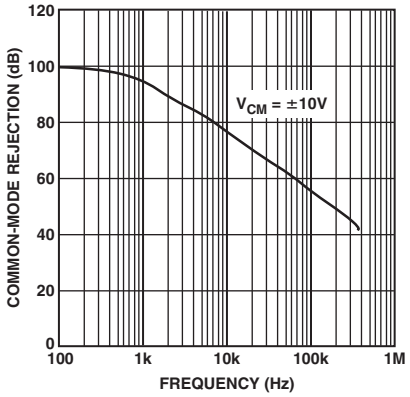
TPC 10. Open-Loop Gain and Phase vs. Frequency



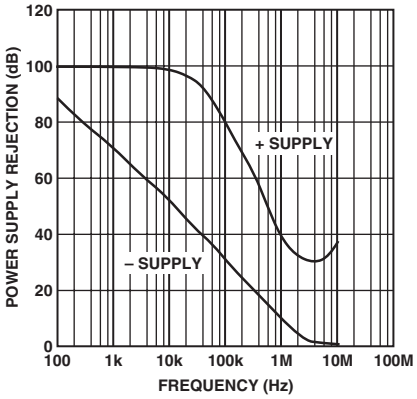
TPC 11. Slew Rate vs. Temperature (Gain = –1)



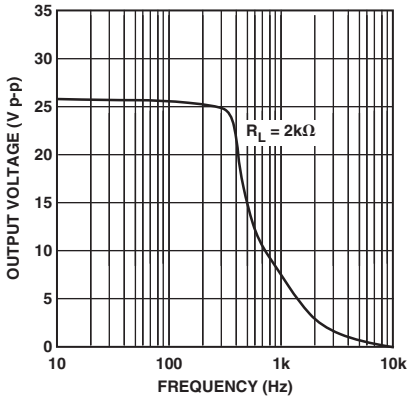
TPC 12. Open-Loop Gain vs. Supply Voltage, R_{LOAD} = 2 kΩ



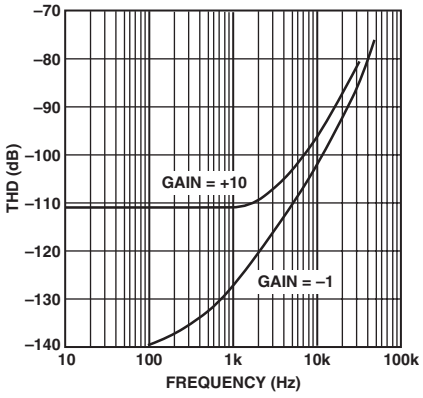
TPC 13. Common-Mode Rejection vs. Frequency



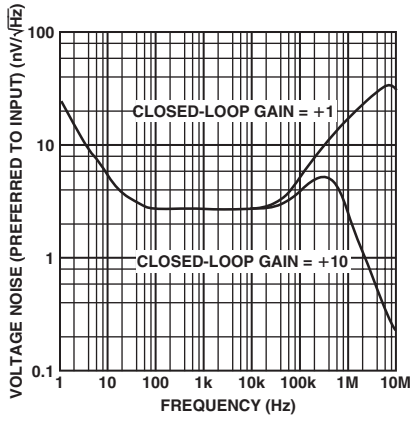
TPC 14. Power Supply Rejection vs. Frequency



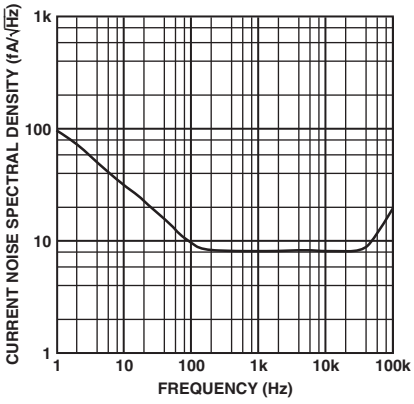
TPC 15. Large Signal Frequency Response



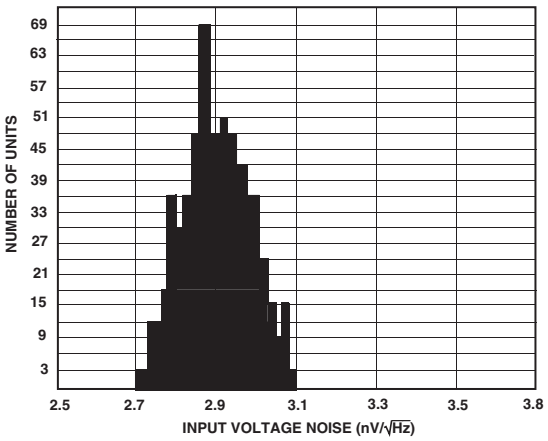
TPC 16. Total Harmonic Distortion vs. Frequency



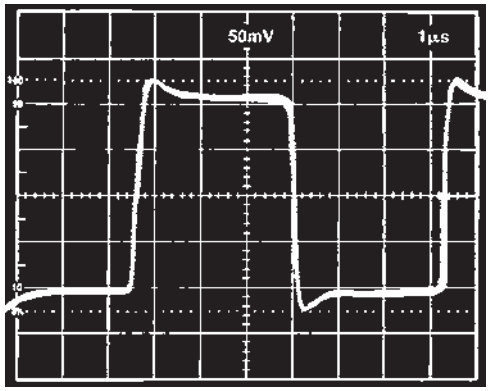
TPC 17. Input Voltage Noise Spectral Density



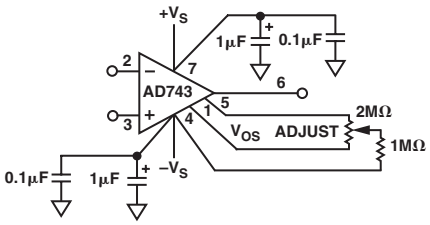
TPC 18. Input Current Noise Spectral Density



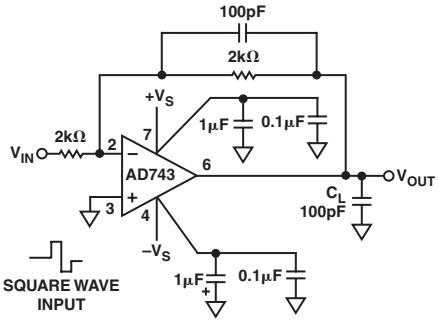
TPC 19. Typical Noise Distribution @ 10 kHz (602 Units)



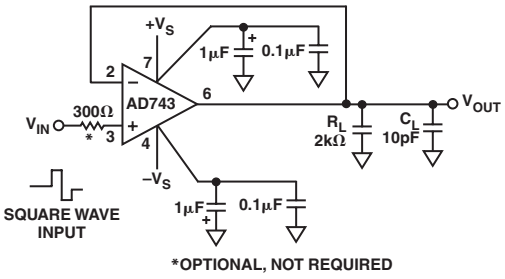
TPC 23. Unity-Gain Follower Small Signal Pulse Response



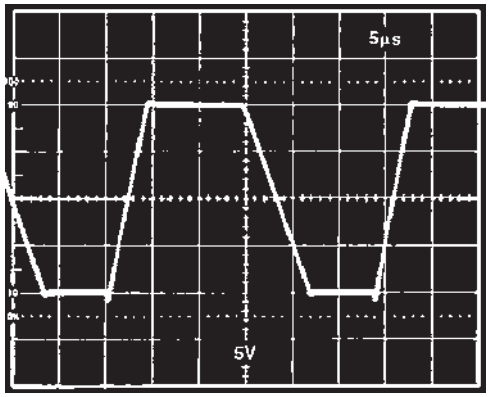
TPC 20. Offset Null Configuration



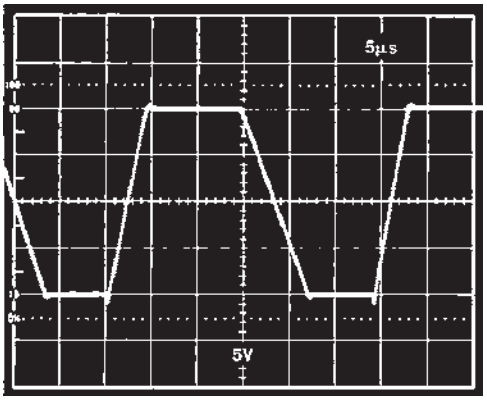
TPC 24. Unity-Gain Inverter



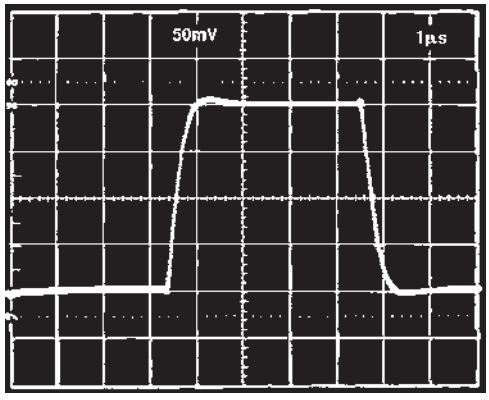
TPC 21. Unity-Gain Follower



TPC 25. Unity-Gain Inverter Large Signal Pulse Response



TPC 22. Unity-Gain Follower Large Signal Pulse Response



TPC 26. Unity-Gain Inverter Small Signal Pulse Response

OP AMP PERFORMANCE: JFET VS. BIPOLAR

The AD743 is the first monolithic JFET op amp to offer the low input voltage noise of an industry-standard bipolar op amp without its inherent input current errors. This is demonstrated in Figure 2, which compares input voltage noise versus input source resistance of the OP27 and AD743 op amps. From this figure, it is clear that at high source impedance the low current noise of the AD743 also provides lower total noise. It is also important to note that with the AD743 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD743 also reduce errors due to offset and drift at high source impedances (Figure 3).

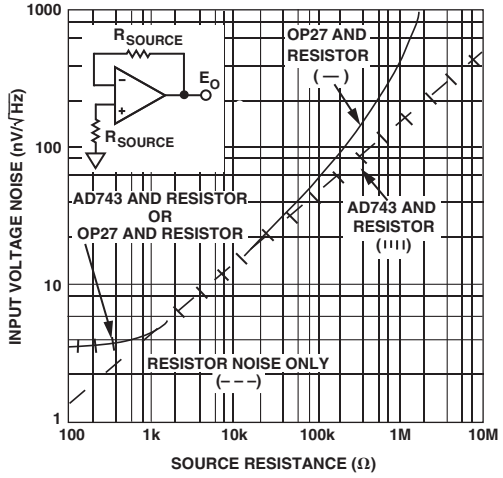


Figure 2. Total Input Noise Spectral Density @ 1 kHz vs. Source Resistance

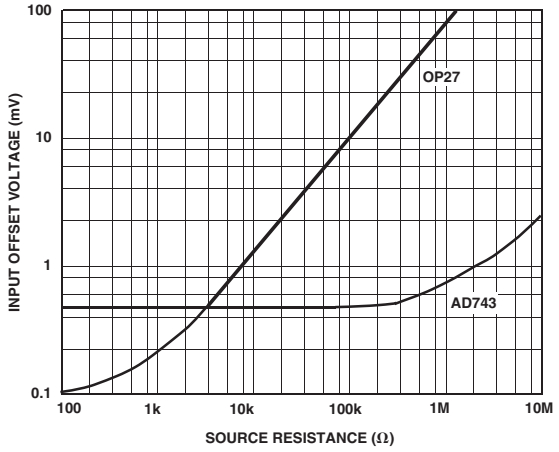


Figure 3. Input Offset Voltage vs. Source Resistance

DESIGNING CIRCUITS FOR LOW NOISE

An op amp's input voltage noise performance is typically divided into two regions: flatband and low frequency noise. The AD743 offers excellent performance with respect to both. The figure of 2.9 nV/√Hz @ 10 kHz is excellent for a JFET input amplifier. The 0.1 Hz to 10 Hz noise is typically 0.38 μV p-p. The user should pay careful attention to several design details in order to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise; therefore, sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways. First, the low frequency noise is strongly dependent on the ambient temperature and increases above +25°C. Second, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current

$$\tilde{I}_n = \sqrt{2qI_B\Delta f}$$

and increases below approximately 100 Hz with a 1/f power spectral density. For the AD743, the typical value of current noise is 6.9 fA/√Hz at 1 kHz. Using the formula

$$\tilde{I}_n = \sqrt{4kT / R\Delta f}$$

to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD743 is equivalent to that of a 3.45×10^8 Ω source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the "real" part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS

As stated, the AD743 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships

$$Q = CV \text{ and } I = \frac{dQ}{dt}$$

As shown, voltage, current, and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built in charge (Q/ΔC).

Figures 4 and 5 show two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier that has a very high input impedance, such as the AD743. Figure 4 shows a model of a charge amplifier circuit. Here, amplification depends on the principle of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor C_S be transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifier's input voltage noise will appear at the output amplified by the noise gain $(1 + (C_S/C_F))$ of the circuit.

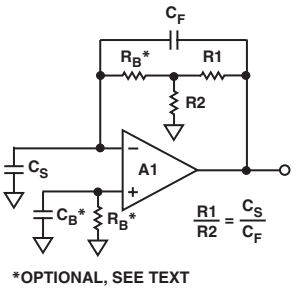


Figure 4. Charge Amplifier Circuit

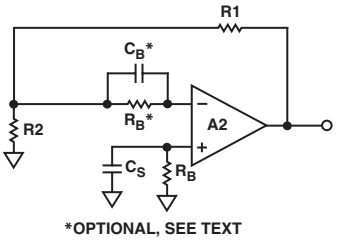


Figure 5. Model for a High Z Follower with Gain

The circuit in Figure 5 is simply a high impedance follower with gain. Here the noise gain (1 + (R1/R2)) is the same as the gain from the transducer to the output. In both circuits, resistor R_B is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor R_B contributes a current noise of

$$\tilde{N} = \sqrt{4k\frac{T}{R_B}\Delta f}$$

where

k = Boltzman's Constant = 1.381×10^{-23} joules/kelvin
T = Absolute Temperature, kelvin (0°C = 273.2 kelvin)
Δf = Bandwidth—in Hz (assuming an ideal "brick wall" filter)

This must be root-sum-squared with the amplifier's own current noise.

Figure 6 shows that these circuits in Figures 4 and 5 have an identical frequency response and noise performance (provided that C_S/C_F = R1/ R2). One feature of the first circuit is that a "T" network is used to increase the effective resistance of R_B and to improve the low frequency cutoff point by the same factor.

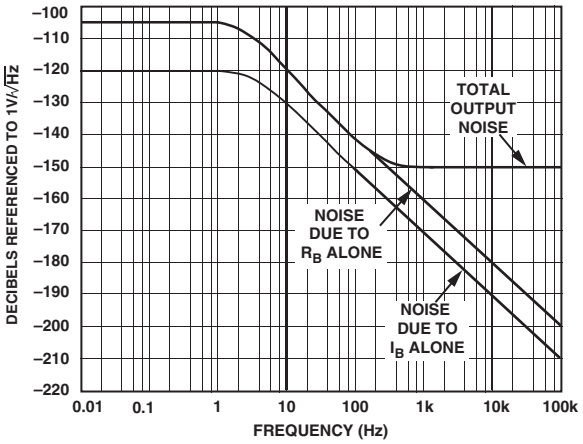


Figure 6. Noise at the Outputs of the Circuits of Figures 4 and 5. Gain = +10, C_S = 3000 pF, R_B = 22 MΩ

However, this does not change the noise contribution of R_B which, in this example, dominates at low frequencies. The graph of Figure 7 shows how to select an R_B large enough to minimize this resistor's contribution to overall circuit noise. When the equivalent current noise of R_B $(\sqrt{4kT)/R}$ equals the noise of I_B $(\sqrt{2qI_B})$, there is diminishing return in making R_B larger.

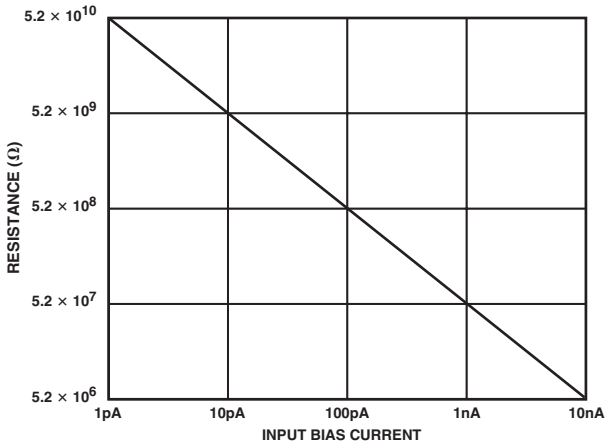


Figure 7. Graph of Resistance vs. Input Bias Current Where the Equivalent Noise $\sqrt{4kT/R}$, Equals the Noise of the Bias Current $\sqrt{2qI_B}$

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B in Figures 4 and 5. As previously mentioned, for best noise performance, care should be taken to also balance the source capacitance designated by C_B. The value for C_B in Figure 4 would be equal to C_S in Figure 5. At values of C_B over 300 pF, there is a diminishing impact on noise; capacitor C_B can then be simply a large bypass of 0.01 µF or greater.

HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD743 is a direct function of device junction temperature, I_B approximately doubling every 10°C. Figure 8 shows the relationship between the bias current and the junction temperature for the AD743. This graph shows that lowering the junction temperature will dramatically improve I_B.

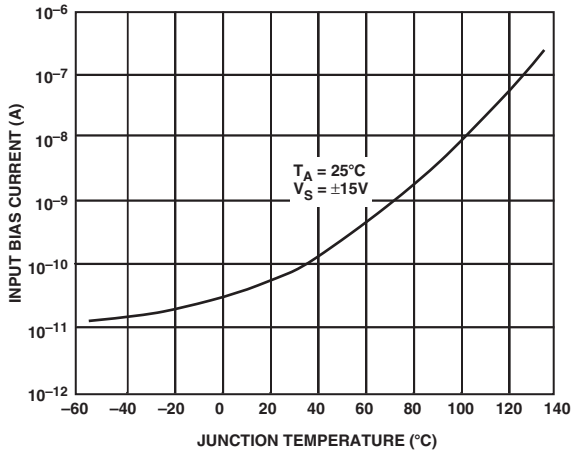
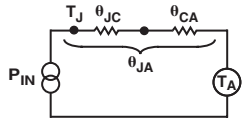


Figure 8. Input Bias Current vs. Junction Temperature

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 9, where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (θ in °C/W).



P_{IN} = DEVICE DISSIPATION
T_A = AMBIENT TEMPERATURE
T_J = JUNCTION TEMPERATURE
θ_{JC} = THERMAL RESISTANCE—JUNCTION TO CASE
θ_{CA} = THERMAL RESISTANCE—CASE TO AMBIENT

Figure 9. Device Thermal Model

From this model, $T_J = T_A + \theta_{JA} P_{IN}$. Therefore, I_B can be determined in a particular application by using Figure 8 together with the published data for θ_{JA} and power dissipation. The user can modify θ_{JA} by using of an appropriate clip-on heat sink, such as the Aavid No. 5801. θ_{JA} is also a variable when using the AD743 in chip form. Figure 10 shows the bias current versus the supply voltage with θ_{JA} as the third variable. This graph can be used to predict bias current after θ_{JA} has been computed. Again, bias current will double for every 10°C. The designer using the AD743 in chip form (Figure 11) must also be concerned with both θ_{JC} and θ_{CA}, since θ_{JC} can be affected by the type of die mount technology used.

Typically, θ_{JC} will be in the 3°C/W to 5°C/W range; therefore, for normal packages, this small power dissipation level may be ignored. But, with a large hybrid substrate, θ_{JC} will dominate proportionately more of the total θ_{JA}.

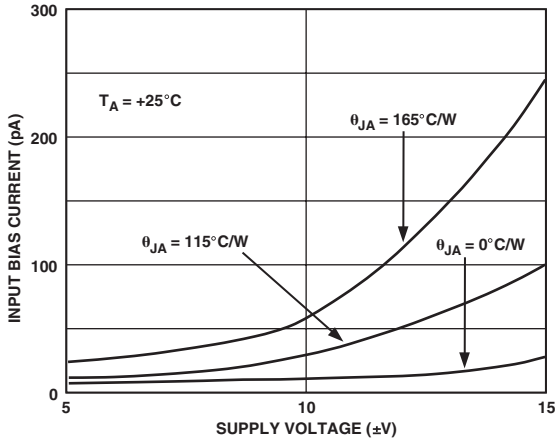


Figure 10. Input Bias Current vs. Supply Voltage for Various Values of θ_{JA}

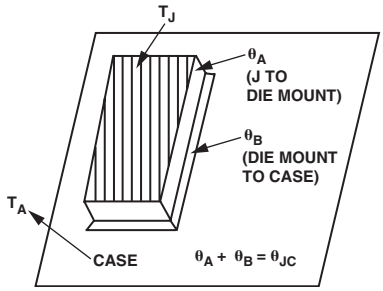
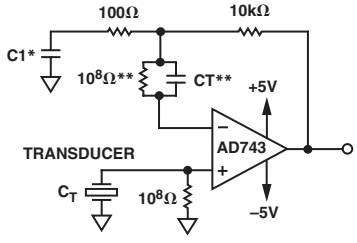


Figure 11. Breakdown of Various Package Thermal Resistances

REDUCED POWER SUPPLY OPERATION FOR LOWER I_B

Reduced power supply operation lowers I_B in two ways: first, by lowering both the total power dissipation and second, by reducing the basic gate-to-junction leakage (Figure 10). Figure 12 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac-coupling capacitor over the –40°C to +85°C temperature range. If the optional coupling capacitor is used, this circuit will operate over the entire –55°C to +125°C military temperature range.



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

Figure 12. Piezoelectric Transducer

AN INPUT IMPEDANCE COMPENSATED, SALLEN-KEY FILTER

The simple high-pass filter of Figure 13 has an important source of error which is often overlooked. Even 5 pF of input capacitance in amplifier A will contribute an additional 1% of pass-band amplitude error, as well as distortion, proportional to the C/V characteristics of the input junction capacitance. The addition of the network designated Z will balance the source impedance—as seen by A—and thus eliminate these errors.

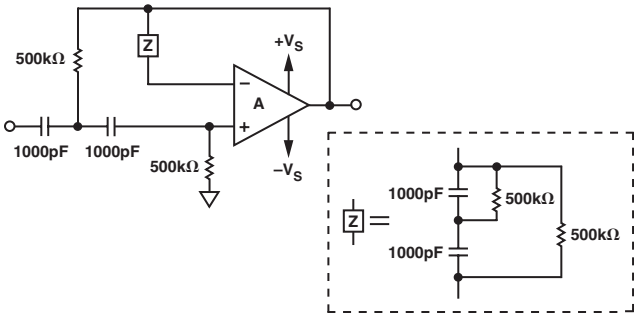


Figure 13. Input Impedance Compensated Sallen-Key Filter

TWO HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/*g*).* Figures 14a and 14b show two ways in which to configure the AD743 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor *C*1 and is equal to

$$\Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1}$$

The ratio of capacitor *C*1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit ($1 + C_T/C1$). The amplifier's voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor *R*1. If a T network is used, the effective value is $R1(1 + R2/R3)$.

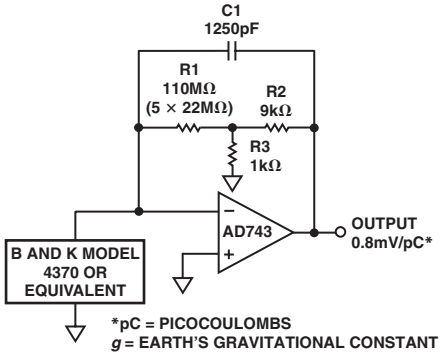


Figure 14a. Basic Accelerometer Circuit

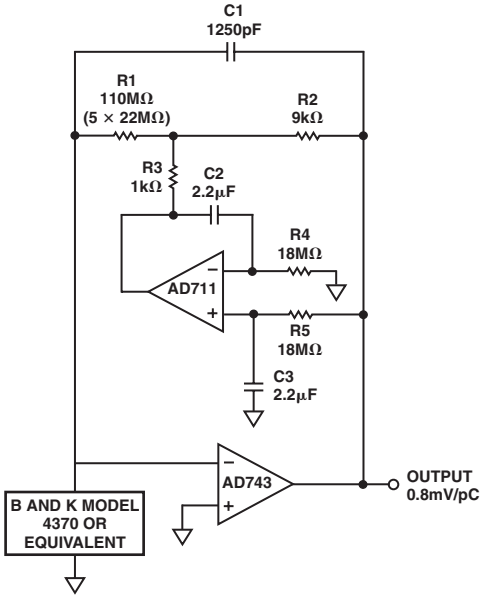


Figure 14b. Accelerometer Circuit Using a DC Servo Amplifier

A dc servo loop (Figure 14b) can be used to assure a dc output which is <10 mV, without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop ($R4C2 = R5C3$) should be

$$Time\ Constant \geq 10\ R1\left(1+\frac{R2}{R3}\right)C1$$

LOW NOISE HYDROPHONE AMPLIFIER

Hydrophones are usually calibrated in the voltage out mode. The circuits of Figures 15a and 15b can be used to amplify the output of a typical hydrophone. Figure 15a shows a typical dc-coupled circuit. The optional resistor and capacitor serve to counteract the dc offset caused by bias currents flowing through resistor R1. Figure 15b, a variation of the original circuit, has a low frequency cutoff determined by an RC time constant equal to

$$Time\ Constant = \frac{1}{2\pi \times C_C \times 100\ \Omega}$$

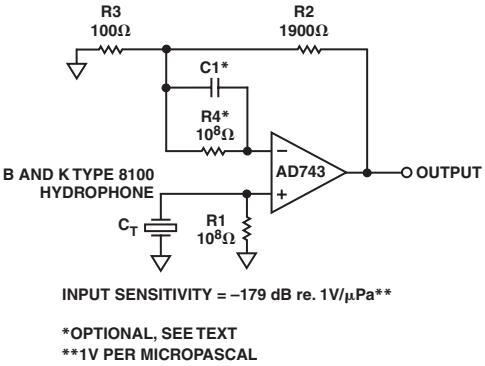


Figure 15a. Basic Hydrophone Amplifier

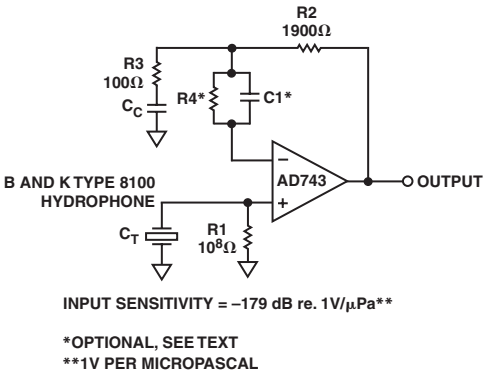


Figure 15b. AC-Coupled, Low Noise Hydrophone Amplifier

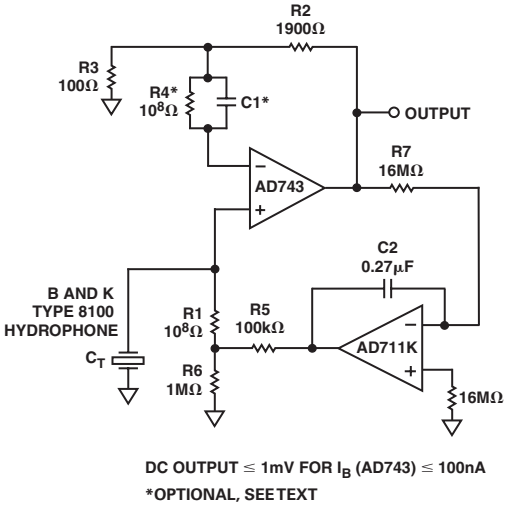


Figure 15c. Hydrophone Amplifier Incorporating a DC Servo Loop

where the dc gain is 1 and the gain above the low frequency cutoff ($1/(2\pi C_C(100\ \Omega))$) is the same as the circuit of Figure 15a. The circuit of Figure 15c uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for I_B up to 100 nA. The time constant of R7 and C2 should be larger than that of R1 and C_T for a smooth low frequency response.

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances (≤300 pF), the lowest noise can be achieved by adding a parallel RC network (R4 = R1, C1 = C_T) in series with the inverting input of the AD743.

BALANCING SOURCE IMPEDANCES

As mentioned previously, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of the AD743. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing input capacitance will minimize ac response errors due to the amplifier's input capacitance and, as shown in Figure 16, noise performance will be optimized. Figure 17 shows the required external components for noninverting (A) and inverting (B) configurations.

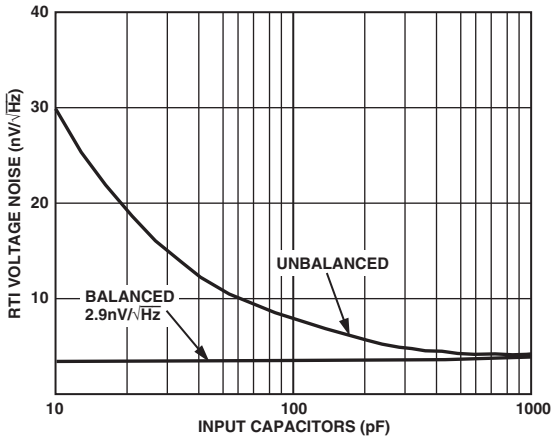


Figure 16. RTI Voltage Noise vs. Input Capacitance

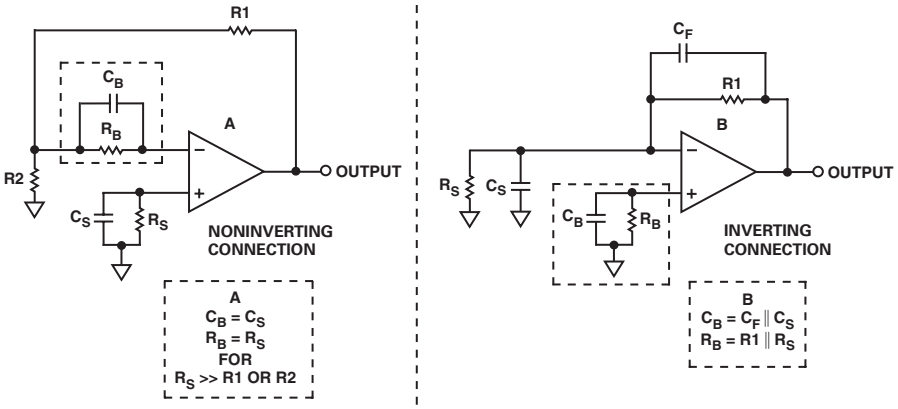
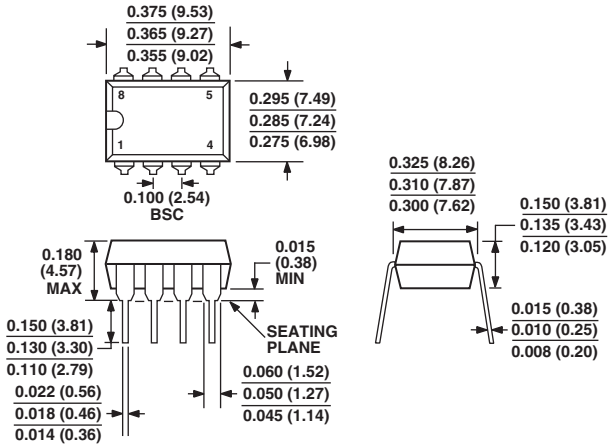


Figure 17. Optional External Components for Balancing Source Impedances

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



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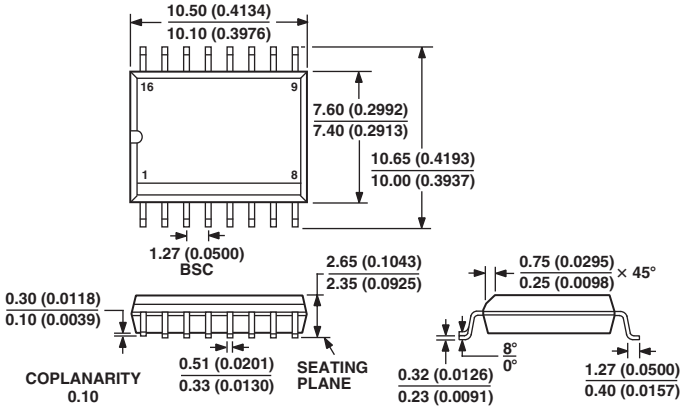
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-16)
Dimensions shown in millimeters and (inches)



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C00830–0–7/03(E)

Revision History

Location	Page
7/03—Data Sheet changed from REV. D to REV. E.	
Deleted K Model	Universal
Changes to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Changes to ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	12
2/02—Data Sheet changed from REV. C to REV. D.	
Edits to PRODUCT DESCRIPTION	1
Edits to CONNECTION DIAGRAMS	1
Deleted AD7435 column from SPECIFICATIONS	1
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Deleted METALLIZATION PHOTOGRAPH	3
Edits to REDUCE POWER SUPPLY OPERATION FOR LOWER I_B	9
Deleted 8-Pin CERDIP (Q) package drawing	12

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