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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

December 2014

FCP104N60F

N-Channel SuperFET® II FRFET® MOSFET

600 V, 37 A, 104 mΩ

Features

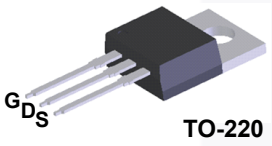
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 91 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 110 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 313 pF)
- 100% Avalanche Tested

Applications

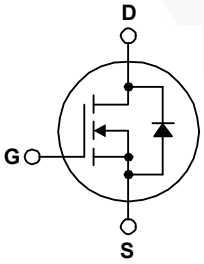
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET® II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



TO-220



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCP104N60F	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f > 1Hz)	±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	37	A
		- Continuous (T_C = 100°C)	24	
I_{DM}	Drain Current	- Pulsed (Note 1)	114	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	809	mJ
I_{AR}	Avalanche Current	(Note 1)	6.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.57	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	50	V/ns
	MOSFET dv/dt		100	
P_D	Power Dissipation	(T_C = 25°C)	357	W
		- Derate Above 25°C	2.85	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCP104N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ,Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP104N60F	FCP104N60F	TO220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, $T_J = 25^oC$	600	-	-	V
		V_{GS} = 0 V, I_D = 10 mA, $T_J = 150^oC$	650	-	-	
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25^oC	-	0.67	-	$V/^oC$
BV_{DS}	Drain-Source Avlanche Breakdown Voltage	V_{GS} = 0 V, I_D = 18.5 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0 V	-	-	10	μA
		V_{DS} = 480 V, $T_C = 125^oC$	-	16	-	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 18.5 A	-	91	104	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 18.5 A	-	33	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	4610	6130	pF
C_{oss}	Output Capacitance		-	3255	4330	pF
C_{rss}	Reverse Transfer Capacitance		-	155	235	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	74	-	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	313	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 18.5 A, V_{GS} = 10 V (Note 4)	-	110	145	nC
Q_{gs}	Gate to Source Gate Charge		-	24	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	44	-	nC
ESR	Equivalent Series Resistance	Drain open		0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 18.5 A, V_{GS} = 10 V, R_{GEN} = 4.7 Ω (Note 4)	-	34	78	ns
t_r	Turn-On Rise Time		-	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	102	214	ns
t_f	Turn-Off Fall Time		-	5.7	21.4	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	37	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	114	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 18.5 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 18.5 A, dI_F/dt = 100 A/μs	-	144	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.91	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 6.8 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 18.5 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

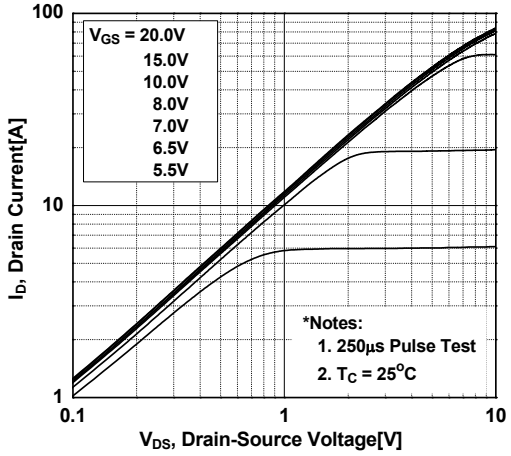


Figure 2. Transfer Characteristics

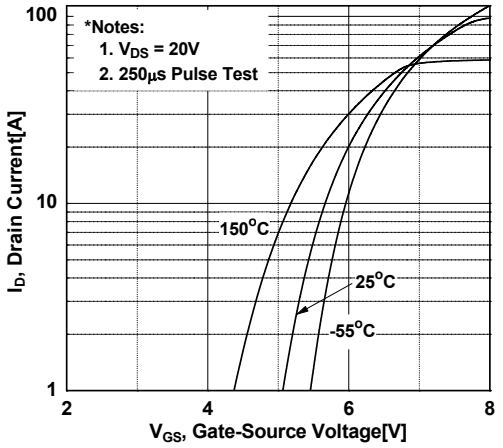


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

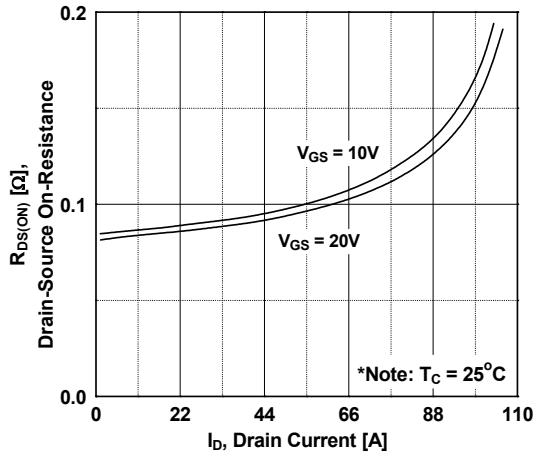


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

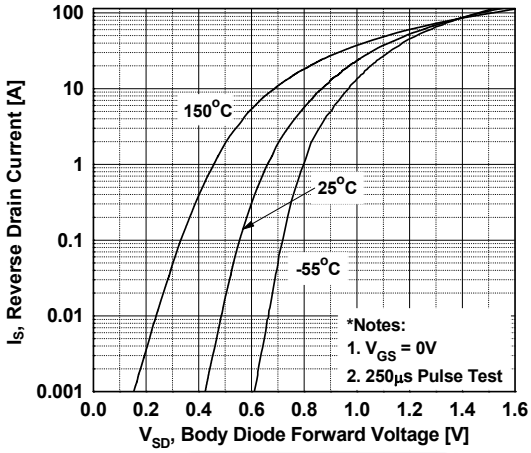


Figure 5. Capacitance Characteristics

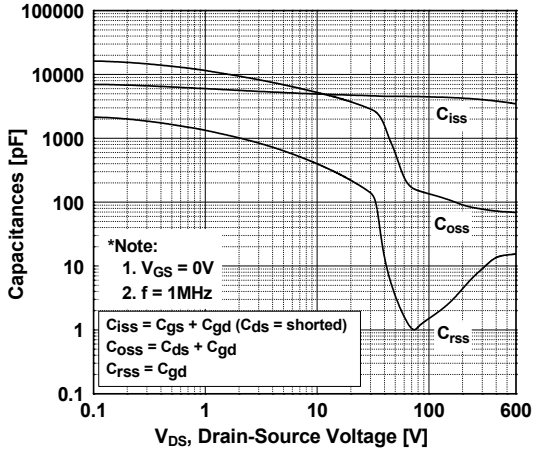
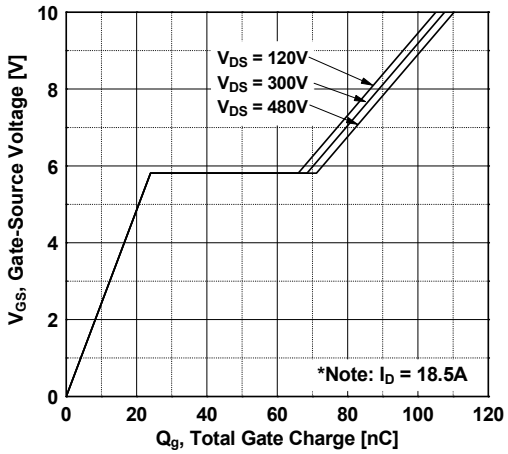


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

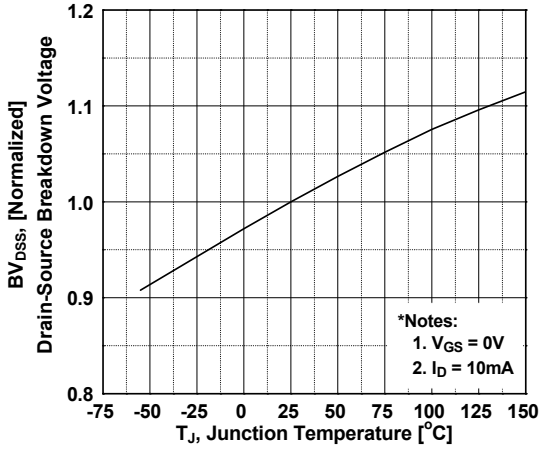


Figure 8. On-Resistance Variation vs. Temperature

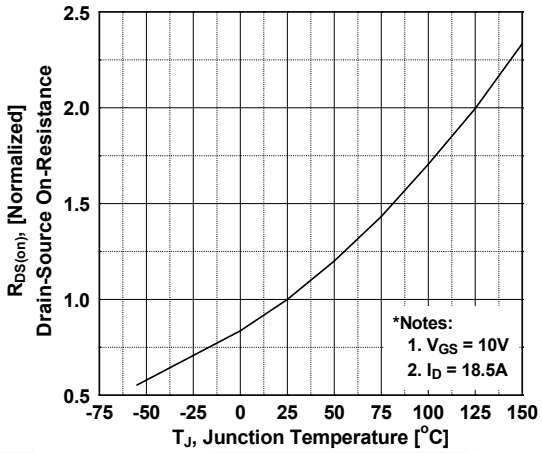


Figure 9. Maximum Safe Operating Area

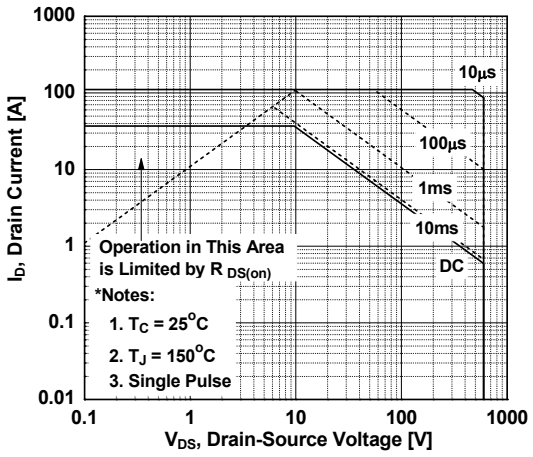


Figure 10. Maximum Drain Current vs. Case Temperature

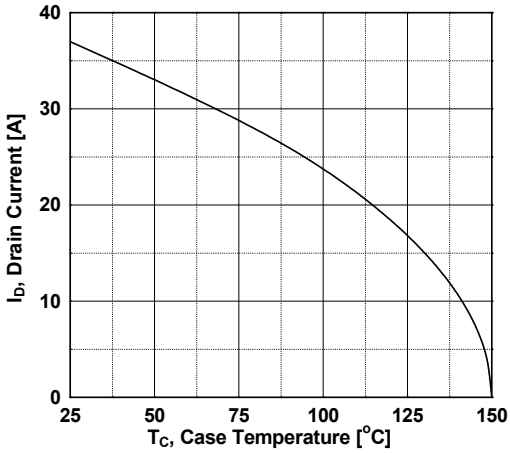


Figure 11. Transient Thermal Response Curve

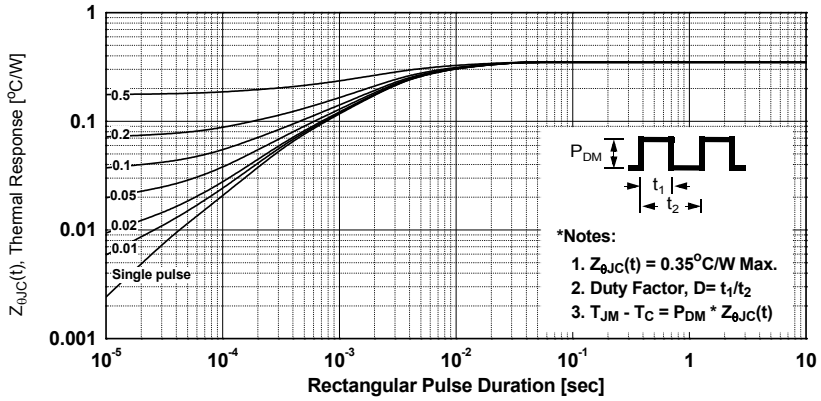


Figure 12. Gate Charge Test Circuit & Waveform

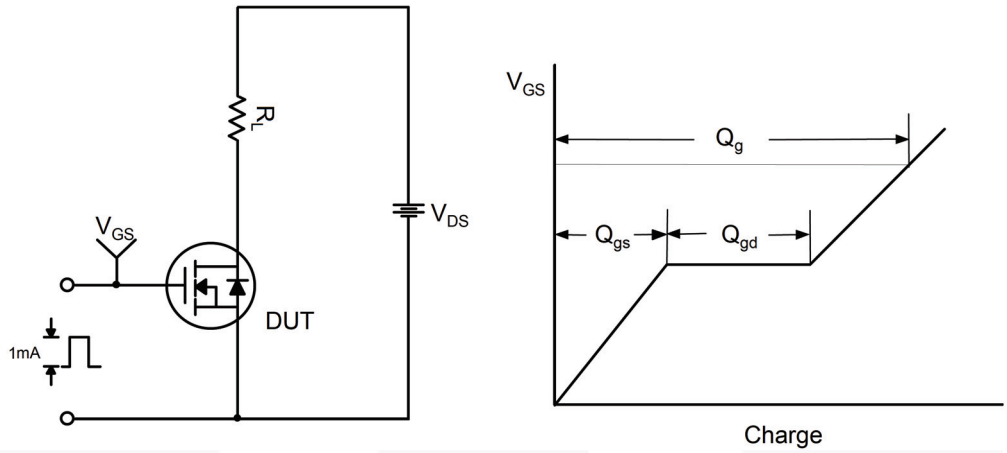


Figure 13. Resistive Switching Test Circuit & Waveforms

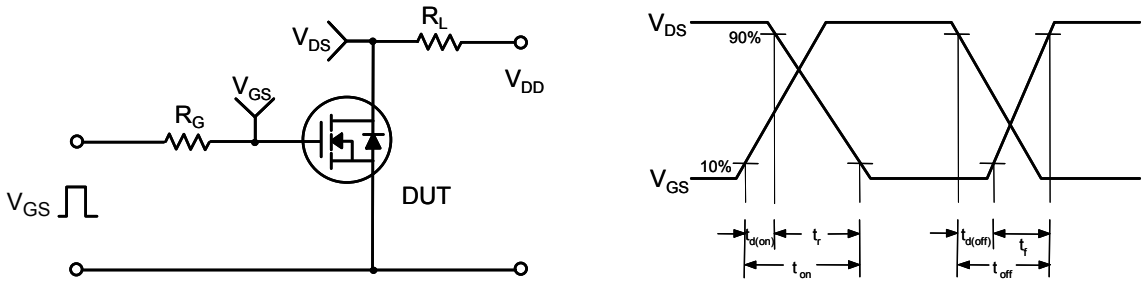


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

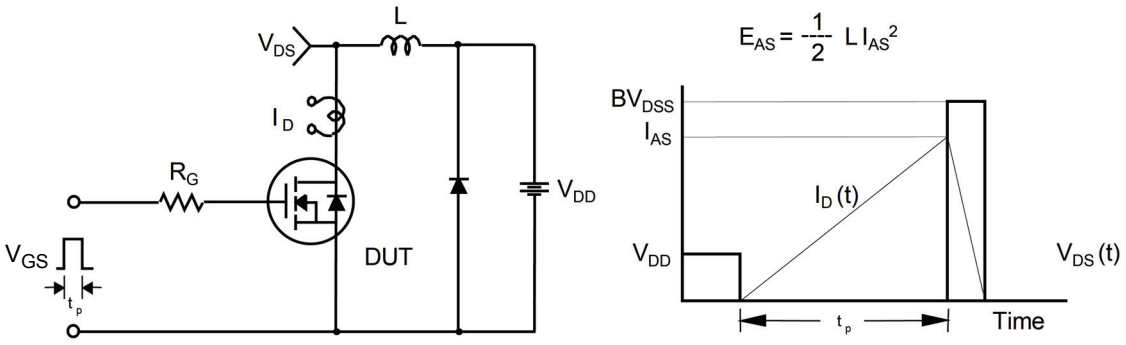
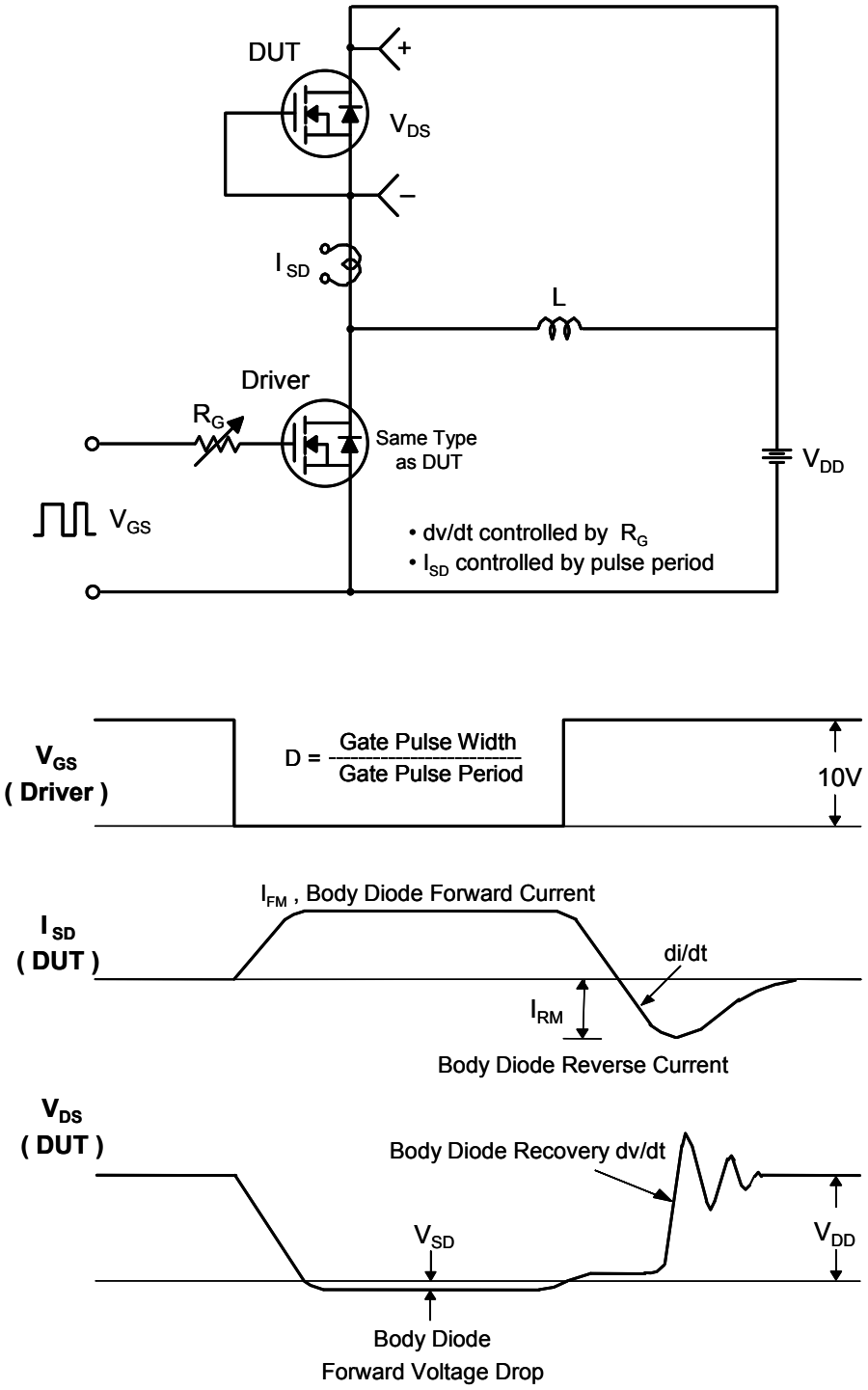
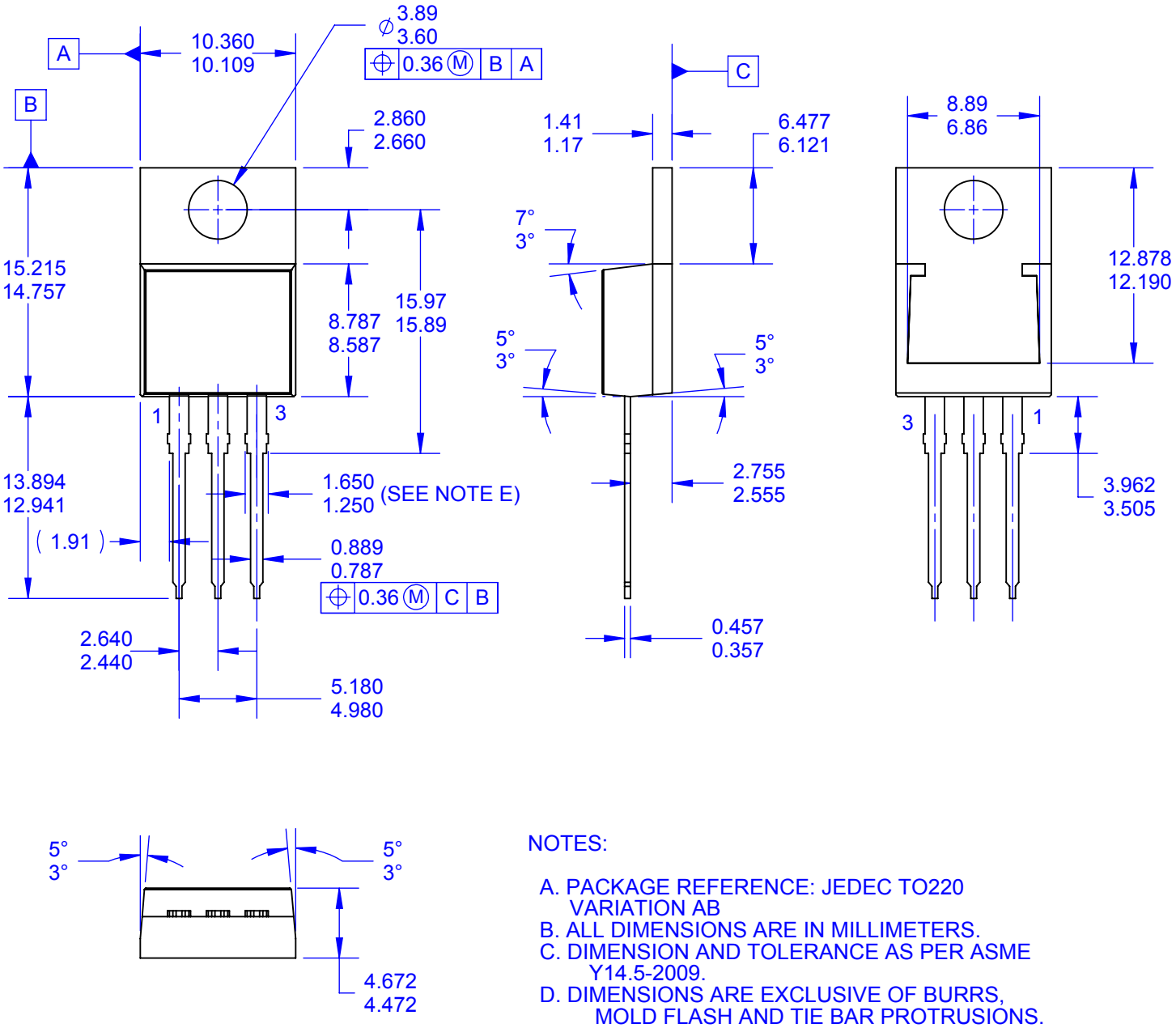


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





NOTES:

A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. MAX WIDTH FOR F102 DEVICE = 1.35mm.
F. DRAWING FILE NAME: TO220T03REV4.
G. FAIRCHILD SEMICONDUCTOR.

PUBLICATION ORDERING INFORMATION

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