5-V Dual TTL-to-Differential PECL Translator

FEATURES

- **1.1-ns (max) Propagation Delay**
- **Operating Range: V_{CC} = 4.2V to 5.7V with GND = 0 V**
- **< 50-ps (typ) Output-to-Output Skew**
- **Built-In Temperature Compensation**
- **Drop-In Compatible to the MC10ELT22, MC100ELT22**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65ELT22 is a dual TTL-to-differential PECL translator. It operates on +5-V supply and ground only. The output is undetermined when the inputs are left floating. The low output skew makes the device an ideal solution for clock or data signal translation.

The SN65ELT22 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT

D or DGK PACKAGE
(TOP VIEW)

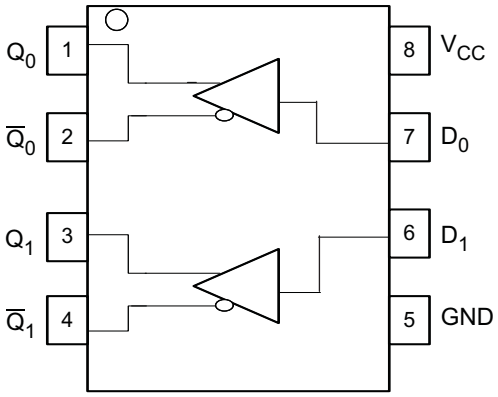


Table 1. Pin Descriptions

PIN	FUNCTION
D_0, D_1	TTL inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	PECL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT22D	SN65ELT22	SOIC	NiPdAu
SN65ELT22DGK	SN65ELT22	SOIC-TSSOP	NiPdAu

(1) Leaded device options are not initially available; contact a sales representative for further details

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage, V_{CC}	GND = 0 V	6	V
Input voltage, V_{IN}	GND = 0 V	GND + 0.025 < V_{IN} < V_{CC} – 0.025	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC		79		°C/W
		SOIC-TSSOP		120		
θ_{JC}	Junction-to-case thermal resistance	SOIC		98		°C/W
		SOIC-TSSOP		74		

KEY ATTRIBUTES

CHARACTERISTICS		VALUE
Moisture sensitivity level		Level 1
Flammability rating (oxygen index: 28 to 34)		UL 94 V-0 at 0.125 in
Electrostatic discharge	Human body model	4 kV
	Charge device model	2 kV
	Machine model	200 V
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

PECL DC CHARACTERISTICS

At V_{CC} = 5.0 V, GND = 0.0 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current			17.3	20		18.2	20		19.4	22	mA
V_{OH}	High-level output voltage	See (3)	3915	3954	4120	3915	3958	4120	3915	3961	4120	mV
V_{OL}	Low-level output voltage	See (3)	3170	3236	3380	3170	3231	3380	3170	3229	3380	mV

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.7 V /–0.8 V.
(3) Outputs are terminated through a 50-Ω resistor to V_{CC} – 2.0 V.

TTL DC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{IN} = 2.7 V, V_{IN} = (V_{CC} – 0.025) V			20	µA
I_{IHH}	High-level input current	V_{IN} = V_{CC}			20	µA
I_{IL}	Low-level input current	V_{IN} = 0.5 V, V_{IN} = (GND + 0.025) V			–200	µA
V_{IK}	Input clamp diode voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	High-level input voltage		2.0		Vcc– 0.025	V
V_{IL}	Low-level input voltage		GND + 0.025		0.8	V

(1) The device meets the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously

AC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, GND = 0.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency(2), see Figure 5			500			490			470		MHz
t_{PLH}	Propagation delay time	1.5 V to 50%	0.6	0.83	1.1	0.6	0.84	1.1	0.6	0.85	1.1	ns
t_{PHL}			0.5		0.9	0.5		0.9	0.5		0.9	
t_{SKEW}	Within device skew	See(3)		25	90		25	90		25	90	ps
	Device-to-device skew	See (4)		25	100		25	100		25	100	
t_{JITTER}	Random clock jitter (RMS)				0.5			0.5			0.5	ps
t_r/t_f	Output rise/fall times	Q (20%–80%)	0.7		1.1	0.7		1.1	0.7		1.1	ns

(1) The device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Maximum switching frequency measured at output amplitude of 300 mV_{pp}.
(3) Measured between outputs under the identical transitions and conditions on any one device.
(4) Device-to-device skew for identical transitions at identical V_{CC} levels.

Typical Termination for Output Driver

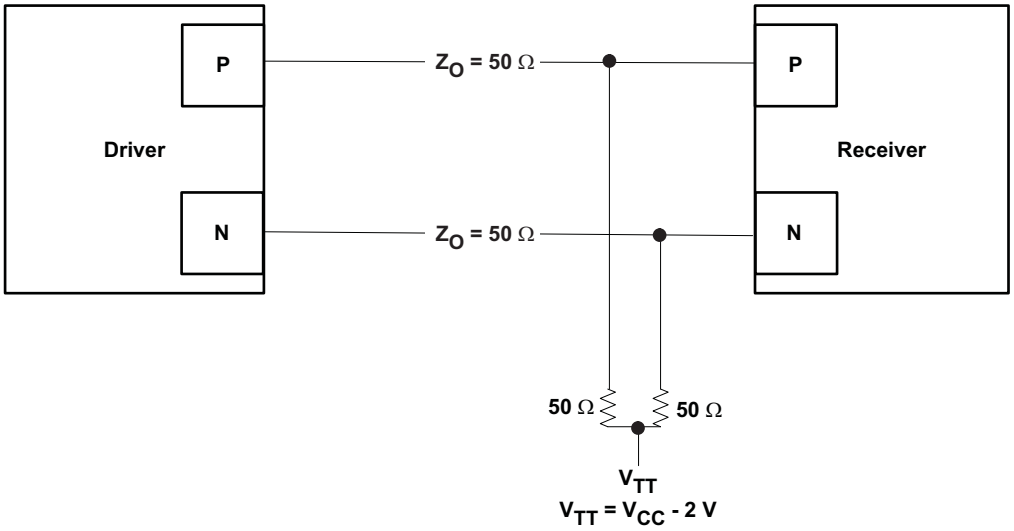


Figure 1. Typical Termination for Driver

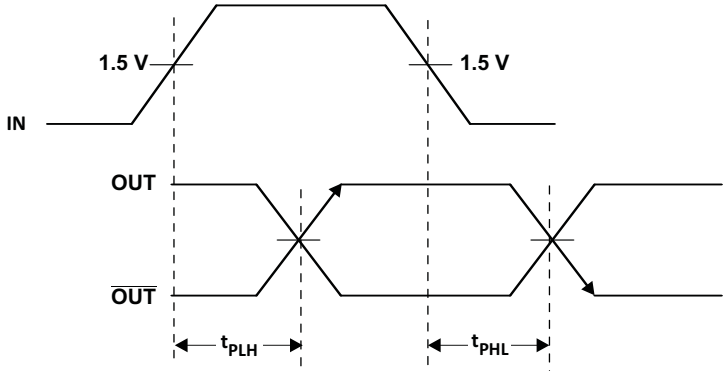


Figure 2. Output Propagation Delay

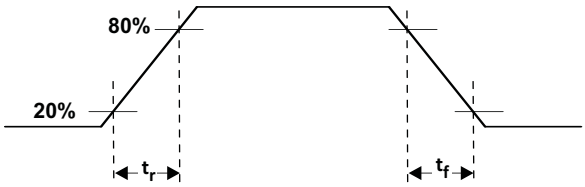


Figure 3. Output Rise and Fall Times

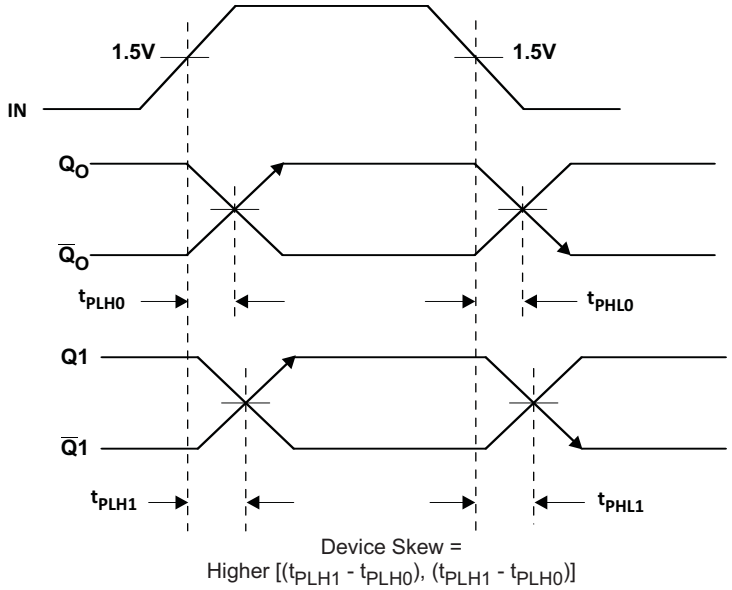


Figure 4. Device Skew

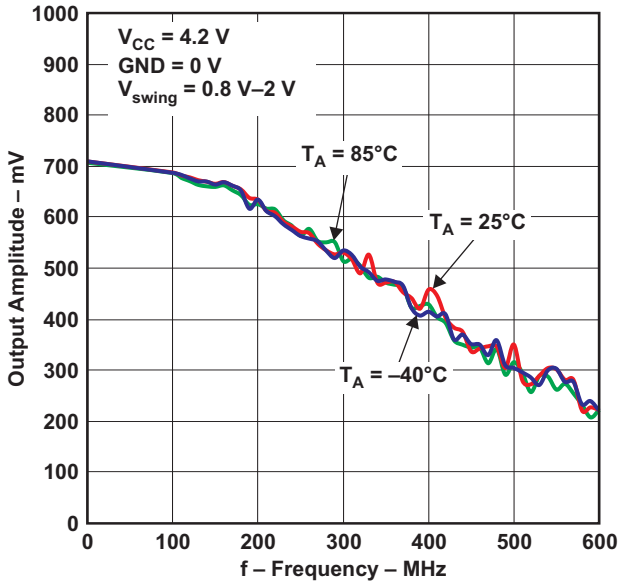


Figure 5. Output Amplitude vs. Frequency

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65ELT22D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22	Samples
SN65ELT22DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI	Samples
SN65ELT22DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIPI	Samples
SN65ELT22DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT22	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

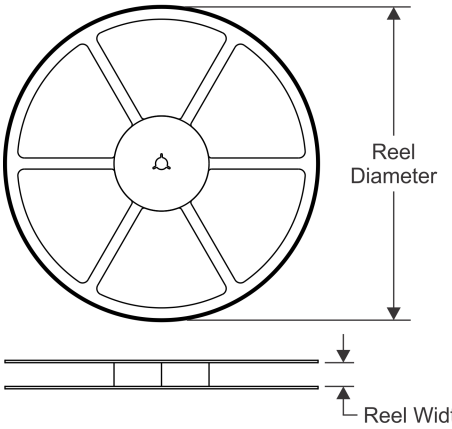
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

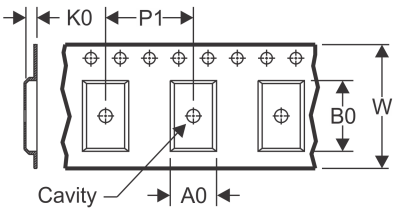
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

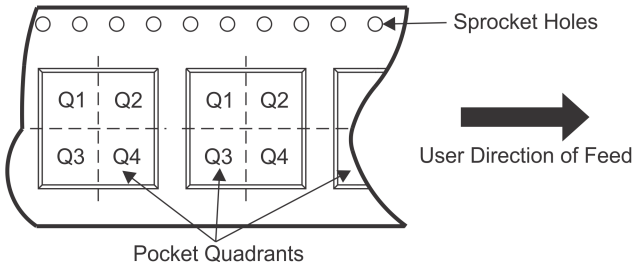


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

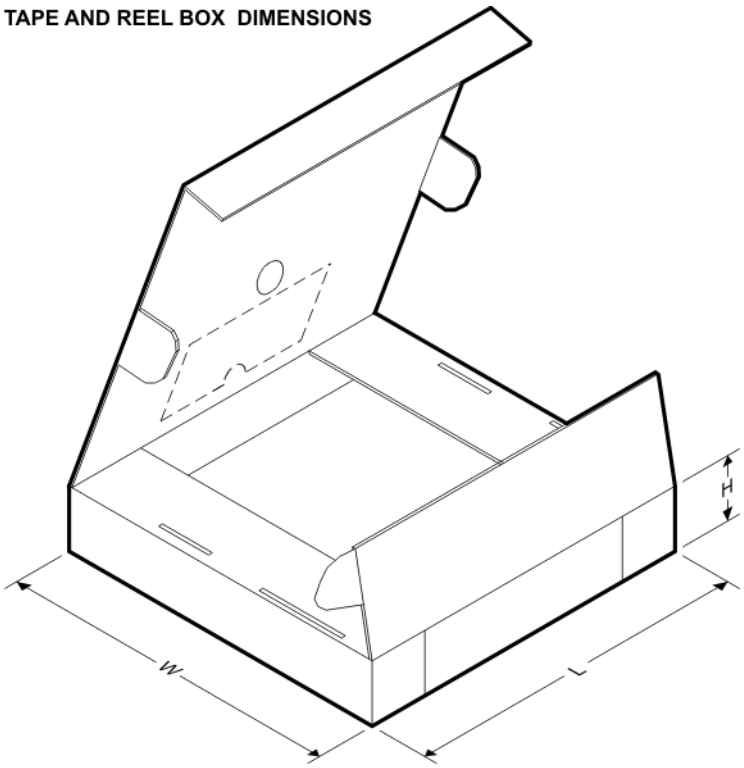
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

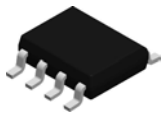
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT22DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT22DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65ELT22DR	SOIC	D	8	2500	367.0	367.0	35.0

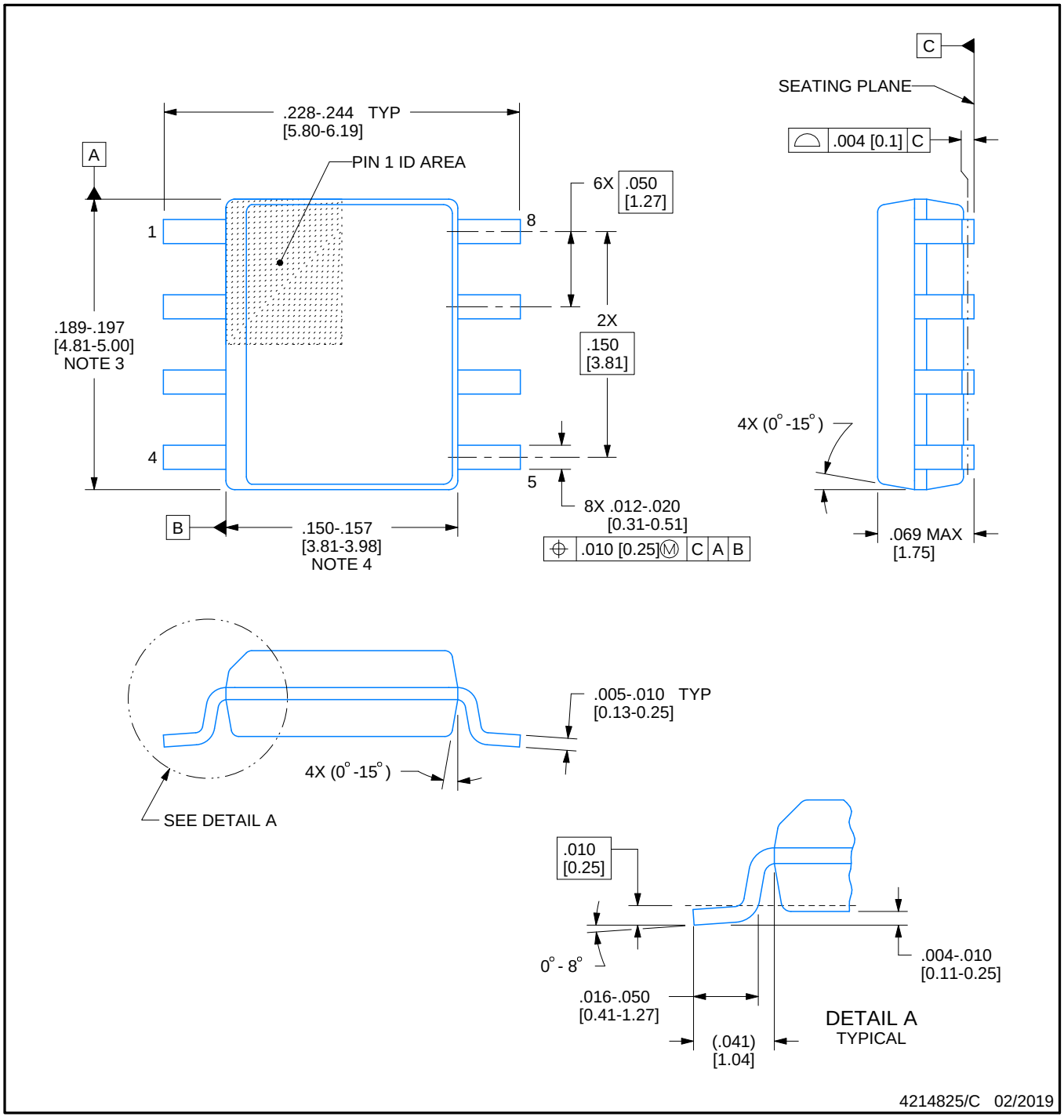


PACKAGE OUTLINE

D0008A

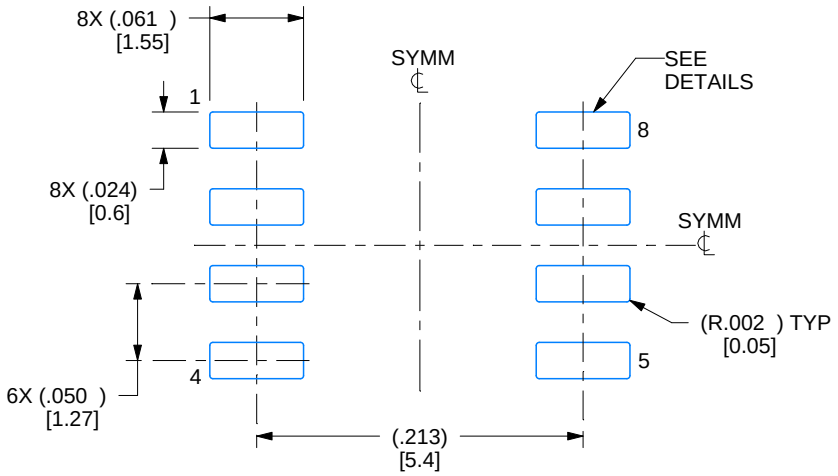
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

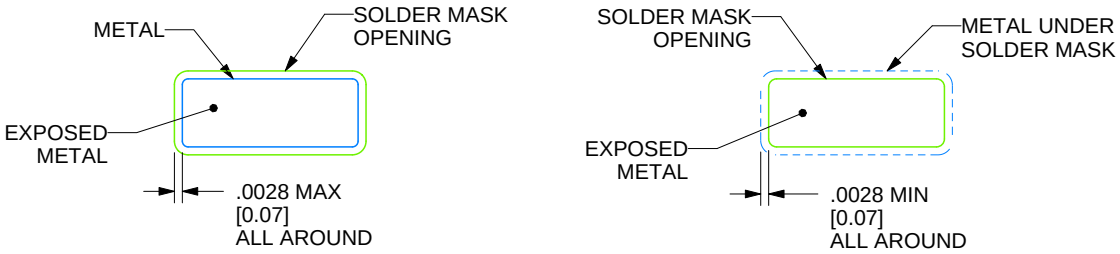


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

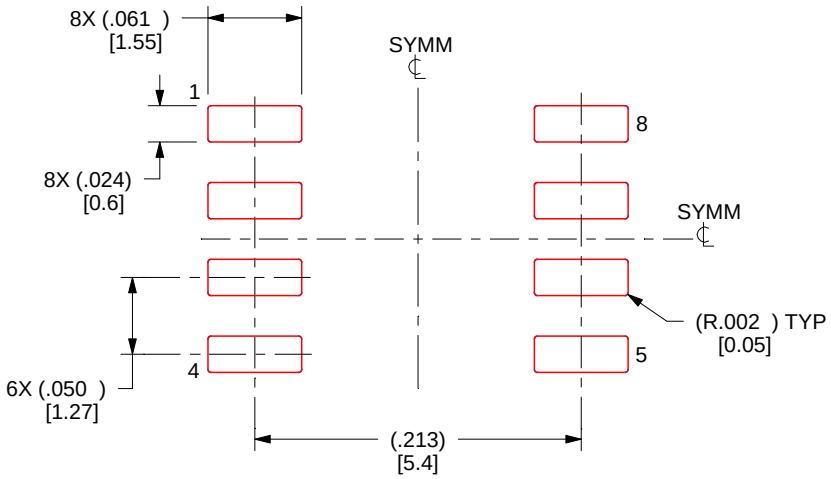
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



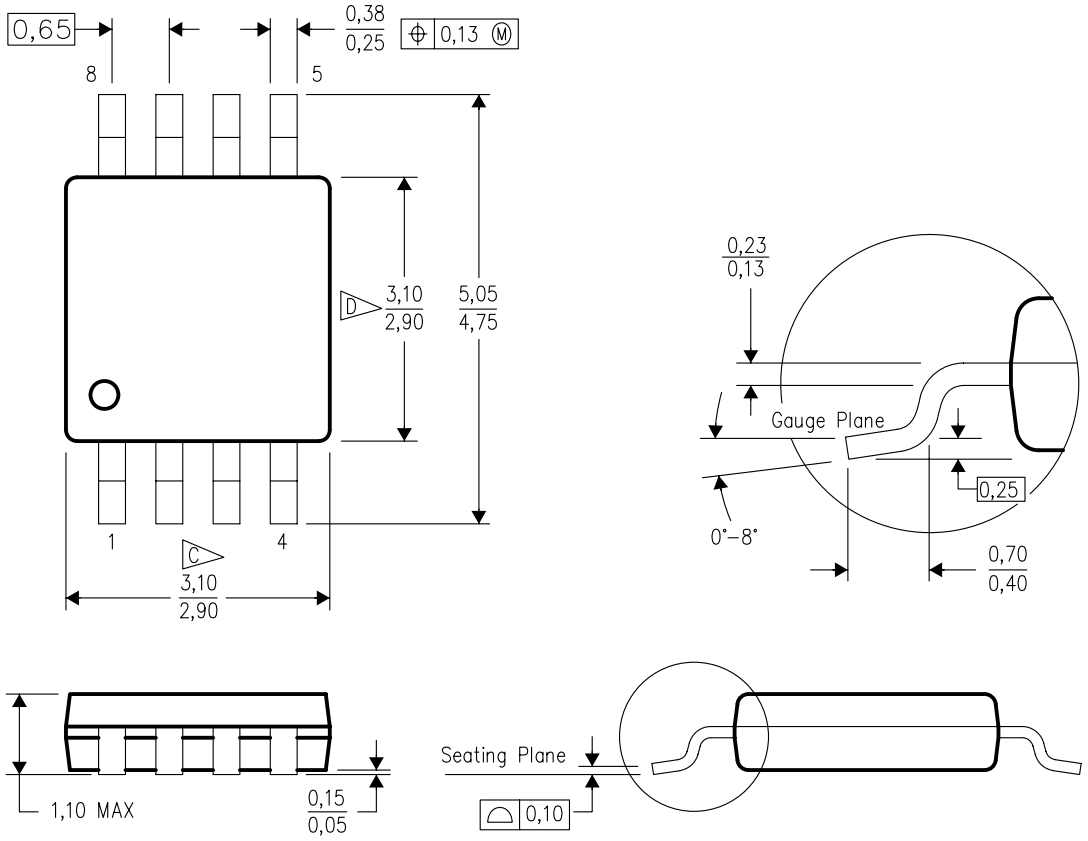
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

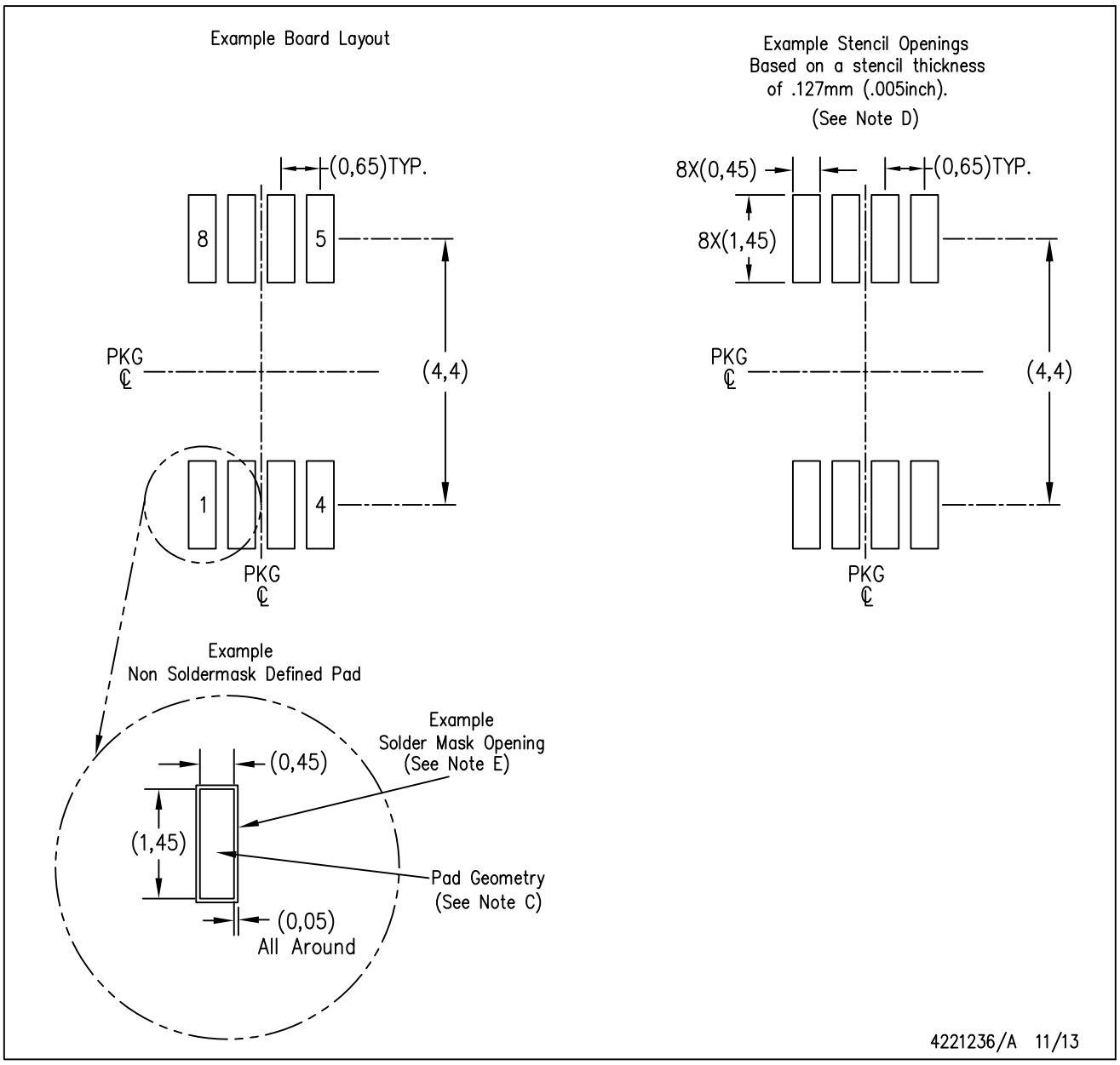
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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