MAX16807

Integrated 8-Channel LED Driver with Switch-Mode Boost and SEPIC Controller

General Description

The MAX16807 is an integrated, high-efficiency white or RGB LED driver. It is designed for LCD backlighting and other LED lighting applications with multiple strings of LEDs. The MAX16807 current-mode PWM controller regulates the necessary voltage to the LED array. Depending on the input voltage and LED voltage range, it can be used with boost or buck-boost (SEPIC) topologies. The MAX16807 features an 8V to 26.5V input voltage range. A wide range of adjustable frequency (20kHz to 1MHz) allows design optimization for efficiency and minimum board space.

The MAX16807 LED driver includes eight open-drain, constant-current-sinking LED driver outputs rated for 36V continuous operation. The LED current-control circuitry achieves ±3% current matching among strings and enables paralleling of outputs for LED string currents higher than 55mA. The output-enable pin is used for simultaneous PWM dimming of all output channels. Dimming frequency range is 50Hz to 30kHz and dimming ratio is up to 5000:1. The constant-current outputs are single resistor programmable and the LED current can be adjusted up to 55mA per output channel.

The MAX16807 operates either in stand-alone mode or with a microcontroller (μC) using an industry-standard, 4-wire serial interface.

The MAX16807 includes overtemperature protection, operates over the full -40°C to +125°C temperature range, and is available in a thermally enhanced, 28-pin TSSOP exposed pad package.

Features

- Eight Constant-Current Output Channels (Up to 55mA Each)
- ±3% Current Matching Among Outputs
- Paralleling Channels Allows Higher Current per LED String
- Output Rated for 36V Continuous Voltage
- Output-Enable Pin for PWM Dimming (Up to 30kHz)
- One Resistor Sets LED Current for All Channels
- Wide Dimming Ratio Up to 5000:1
- Low Current-Sense Reference (300mV) for High Efficiency
- 8V to 26.5V Input Voltage or Higher with External Biasing Devices
- 4-Wire Serial Interface to Control Individual Output Channels

Applications

- LCD White or RGB LED Backlighting:
  LCD TVs, Desktop and Notebook Panels, Industrial and Medical Displays
- Ambient, Mood, and Accent Lighting

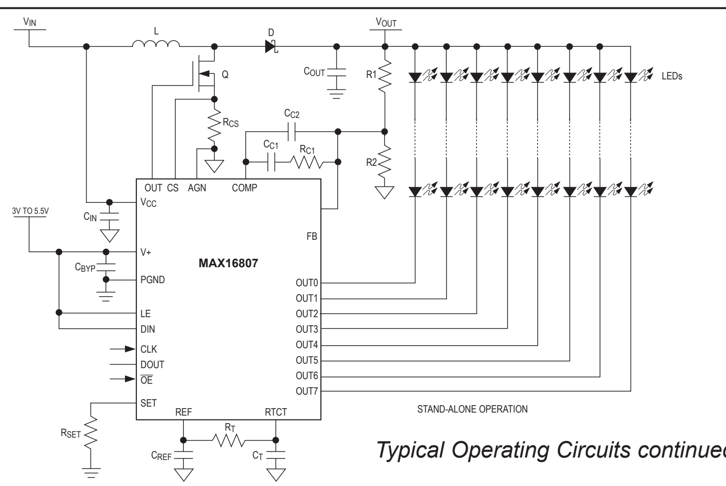
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16807AU I+	- 40°C to + 125°C	28 TSSOP-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

Absolute Maximum Ratings

V_{CC} to AGND...-0.3V to +30V
Current into V_{CC} (V_{CC} > 24V)..±30mA
V+ to PGND...-0.3V to +6V
OUT to AGND..-0.3V to (V_{CC} + 0.3V)
OUT Current (10µs duration)..±1A
FB, COMP, CS, RTCT, REF to AGND......................-0.3V to +6V
COMP Sink Current...10mA
OUT0–OUT7 to PGND...-0.3V to +40V
DIN, CLK, LE, $\overline{OE}$, SET to PGND.................-0.3V to (V+ + 0.3V)
DOUT Current...±10mA
OUT0–OUT7 Sink Current..60mA
Total PGND Current 480mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 27mW/°C* above +70°C)......2162mW
Operating Temperature Range..........................-40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

**Per JEDEC51 Standard (Multilayer Board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (PWM Controller)

(V_{CC} = +15V, V+ = +3V to +5.5V referenced to PGND, R_T = 10kΩ, C_T = 3.3nF, REF = open, COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND, V_{AGND} = V_{PGND} = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T_J = T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage	V_{REF}	I_{REF} = 1mA, T_J = +25°C	4.95	5	5.05	V
Line Regulation	ΔV_{LINE}	12V < V_{CC} < 25V, I_{REF} = 1mA		0.4	4	mV
Load Regulation	ΔV_{LOAD}	1mA < I_{REF} < 20mA		6	50	mV
Total Output-Voltage Variation	V_{REFT}	(Note 2)	4.875		5.125	V
Output Noise Voltage	V_{NOISE}	10Hz < f < 10kHz		50		µV
Output Short-Circuit Current	I_{SHORT}	V_{REF} = 0V	30		180	mA
OSCILLATOR						
Initial Accuracy		T_J = +25°C	51	54	57	kHz
Voltage Stability		12V < V_{CC} < 25V		0.2	0.5	%
Temperature Stability				1		%
RTCT Ramp Peak-to-Peak				1.7		V
RTCT Ramp Valley				1.1		V
Discharge Current	I_{DIS}	V_{RTCT} = 2V, T_J = +25°C	7.9	8.3	8.7	mA
		V_{RTCT} = 2V, -40°C ≤ T_J ≤ +125°C	7.5	8.3	9.0	
Frequency Range	f_{OSC}		20		1000	kHz
ERROR AMPLIFIER						
FB Input Voltage	V_{FB}	FB shorted to COMP	2.45	2.50	2.55	V
Input Bias Current	$I_{B(FB)}$			-0.01	-0.1	µA
Open-Loop Gain	A_{VOL}	2V ≤ V_{COMP} ≤ 4V		100		dB
Unity-Gain Bandwidth	f_{GBW}			1		MHz
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V	60	80		dB
COMP Sink Current	I_{SINK}	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
COMP Source Current	I_{SOURCE}	V_{FB} = 2.3V, V_{COMP} = 5V	0.5	1.2	1.8	mA
COMP Output-Voltage High	V_{OH}	V_{FB} = 2.3V, R_{COMP} = 15kΩ to AGND	5	5.8		V
COMP Output-Voltage Low	V_{OL}	V_{FB} = 2.7V, R_{COMP} = 15kΩ to V_{REF}		0.1	1.1	V

Electrical Characteristics (PWM Controller) (continued)

(V_{CC} = +15V, V+ = +3V to +5.5V referenced to PGND, R_T = 10kΩ, C_T = 3.3nF, REF = open, COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND, V_{AGND} = V_{PGND} = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T_J = T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER							
Current-Sense Gain	A_{CS}	(Notes 3, 4)		2.85	3.00	3.40	V/V
Maximum Current-Sense Signal	V_{CS_MAX}	(Note 3)		0.275	0.300	0.325	V
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V			70		dB
Current-Sense Input Bias Current	I_{CS}	V_{COMP} = 0V			-1	-2.5	µA
Current Sense to OUT Delay	t_{PWM}	50mV overdrive			60		ns
MOSFET DRIVER							
OUT Low-Side On-Resistance	V_{RDS_ONL}	I_{SINK} = 200mA	T_J = -40°C to +85°C (Note 2)		4.5	10	Ω
			T_J = -40°C to +125°C		4.5	12	
OUT High-Side On-Resistance	V_{RDS_ONH}	I_{SOURCE} = 100mA	T_J = -40°C to +85°C (Note 2)		3.5	7.5	Ω
			T_J = -40°C to +125°C		3.5	10	
Source Current (Peak)	I_{SOURCE}	C_{LOAD} = 10nF			2		A
Sink Current (Peak)	I_{SINK}	C_{LOAD} = 10nF			1		A
Rise Time	t_R	C_{LOAD} = 1nF			15		ns
Fall Time	t_F	C_{LOAD} = 1nF			22		ns
UNDERVOLTAGE LOCKOUT/STARTUP							
Startup Voltage Threshold	V_{CC_START}			7.98	8.4	8.82	V
Minimum Operating Voltage After Turn-On	V_{CC_MIN}			7.1	7.6	8.0	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$				0.8		V
PULSE-WIDTH MODULATION (PWM)							
Maximum Duty Cycle	D_{MAX}			94.5	96	97.5	%
Minimum Duty Cycle	D_{MIN}					0	%
SUPPLY CURRENT							
Startup Supply Current	I_{START}	V_{CC} = 7.5V			32	65	µA
Operating Supply Current	I_{CC}	V_{FB} = V_{CS} = 0V			3	5	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25mA		24	26.5		V

Electrical Characteristics (LED Driver)

(V+ = +3V to +5.5V, V_{AGND} = V_{PGND} = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		3.0		5.5	V
Output Voltage	$V_{OUT\_}$				36	V
Standby Current (Interface Idle, All Output Ports High Impedance)		R_{SET} = 360Ω, DIN, LE, CLK = PGND or V+, $\overline{OE}$ = V+, DOUT unconnected		3.6	4.5	mA
Standby Current (Interface Active, All Output Ports High Impedance)		R_{SET} = 360Ω, f_{CLK} = 5MHz, $\overline{OE}$ = V+, DIN, LE = PGND or V+, DOUT unconnected		3.8	4.8	mA
Supply Current (Interface Idle, All Output Ports Active Low)	I+	R_{SET} = 360Ω, $\overline{OE}$ = PGND, DIN, LE = V+, DOUT unconnected		17	30	mA
INTERFACE (DIN, CLK, DOUT, LE, $\overline{OE}$)						
Input-Voltage High (DIN, CLK, LE, $\overline{OE}$)	V_{IH}		0.7 x V+			V
Input-Voltage Low (DIN, CLK, LE, $\overline{OE}$)	V_{IL}				0.3 x V+	V
Hysteresis Voltage (DIN, CLK, LE, $\overline{OE}$)	V_{HYST}			0.8		V
Input Leakage Current (DIN, CLK)	I_{LEAK}		-1		+1	µA
$\overline{OE}$ Pullup Current to V+	$I_{\overline{OE}}$	V+ = 5.5V, $\overline{OE}$ = PGND	0.25	1.5	25.0	µA
LE Pulldown Current to PGND	I_{LE}	V+ = 5.5V, LE = V+	0.25	1.5	25.0	µA
Output-Voltage High (DOUT)	V_{OH}	I_{SOURCE} = 4mA	V+ - 0.5V			V
Output-Voltage Low (DOUT)	V_{OL}	I_{SINK} = 4mA			0.5	V
OUT_ Output Current	$I_{OUT\_}$	0°C ≤ T_A ≤ +125°C, V_{OUT} = 1V to 2.5V, R_{SET} = 360Ω	46.5	50	53.5	mA
		T_A = -40°C, V_{OUT} = 1V to 2.5V, R_{SET} = 360Ω	43		57	
OUT_ Leakage Current		$\overline{OE}$ = V+			1	µA

5V Timing Characteristics

(V+ = +4.5V to +5.5V, V_{AGND} = V_{PGND} = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INTERFACE TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		40			ns
CLK Pulse-Width High	t_{CH}		19			ns
CLK Pulse-Width Low	t_{CL}		19			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		12		50	ns
DOUT Rise Time	t_{DR}	C_{DOUT} = 10pF, 20% to 80%			10	ns
DOUT Fall Time	t_{DF}	C_{DOUT} = 10pF, 80% to 20%			10	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		15			ns
LE Rising to OUT_ Rising Delay	t_{LRR}	(Note 6)			110	ns
LE Rising to OUT_ Falling Delay	t_{LRF}	(Note 6)			325	ns
CLK Rising to OUT_ Rising Delay	t_{CRR}	(Note 6)			110	ns
CLK Rising to OUT_ Falling Delay	t_{CRF}	(Note 6)			325	ns
$\overline{OE}$ Rising to OUT_ Rising Delay	$t_{\overline{OE}R}$	(Note 6)			110	ns
$\overline{OE}$ Falling to OUT_ Falling Delay	$t_{\overline{OE}F}$	(Note 6)			325	ns
OUT_ Turn-On Fall Time	t_F	80% to 20% (Note 6)			210	ns
OUT_ Turn-Off Rise Time	t_R	20% to 80% (Note 6)			130	ns

3.3V Timing Characteristics

($V+$ = +3V to < +4.5V, V_{AGND} = V_{PGND} = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

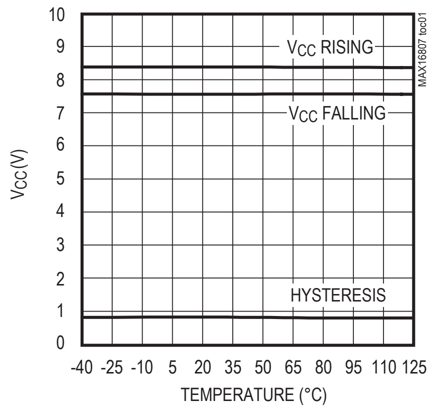
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERFACE TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		52			ns
CLK Pulse-Width High	t_{CH}		24			ns
CLK Pulse-Width Low	t_{CL}		24			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		12		70	ns
DOUT Rise Time	t_{DR}	C_{DOUT} = 10pF, 20% to 80%			12	ns
DOUT Fall Time	t_{DF}	C_{DOUT} = 10pF, 80% to 20%			12	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		15			ns
LE Rising to OUT_ Rising Delay	t_{LRR}	(Note 6)			140	ns
LE Rising to OUT_ Falling Delay	t_{LRF}	(Note 6)			350	ns
CLK Rising to OUT_ Rising Delay	t_{CRR}	(Note 6)			140	ns
CLK Rising to OUT_ Falling Delay	t_{CRF}	(Note 6)			350	ns
$\overline{OE}$ Rising to OUT_ Rising Delay	$t_{\overline{OE}R}$	(Note 6)			140	ns
$\overline{OE}$ Falling to OUT_ Falling Delay	$t_{\overline{OE}F}$	(Note 6)			350	ns
OUT_ Turn-On Fall Time	t_F	80% to 20% (Note 6)			275	ns
OUT_ Turn-Off Rise Time	t_R	20% to 80% (Note 6)			150	ns

Note 1: All devices are 100% production tested at T_J = +25°C and T_J = +125°C. Limits to T_A = -40°C are guaranteed by design.
Note 2: Guaranteed by design, not production tested.
Note 3: Parameter is measured at trip point of latch with V_{FB} = 0V.
Note 4: Gain is defined as $A = \Delta V_{COMP}/\Delta V_{CS}$, $0.05V \le V_{CS} \le 0.25V$.
Note 5: See Figures 3 and 4.
Note 6: A 65Ω pullup resistor is connected from OUT_ to 5.5V. Rising refers to $V_{OUT\_}$ when current through OUT_ is turned off and falling refers to $V_{OUT\_}$ when current through OUT_ is turned on.

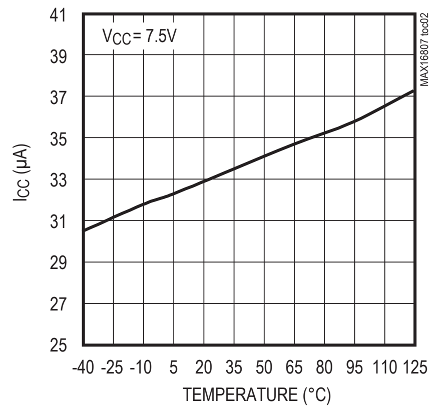
Typical Operating Characteristics

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, V_{CS} = V_{AGND} = V_{PGND} = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

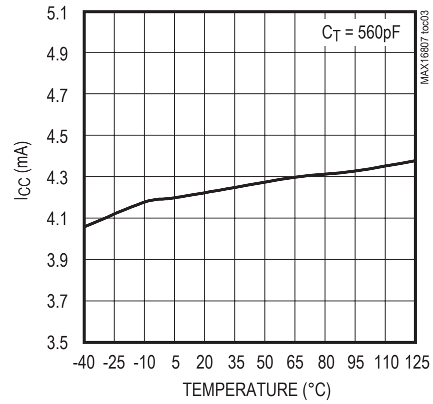
BOOTSTRAP UVLO vs. TEMPERATURE



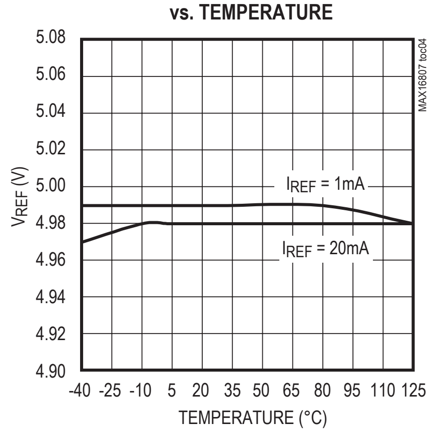
STARTUP CURRENT vs. TEMPERATURE



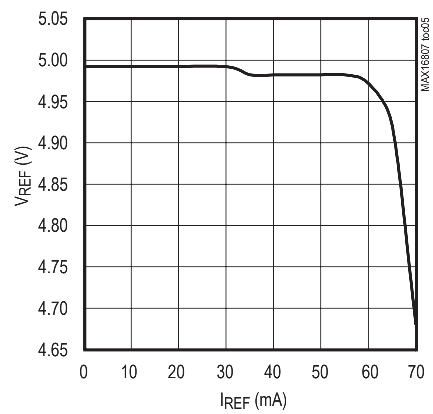
OPERATING SUPPLY CURRENT vs. TEMPERATURE AFTER STARTUP (f_{OSC} = f_{SW} = 300kHz)



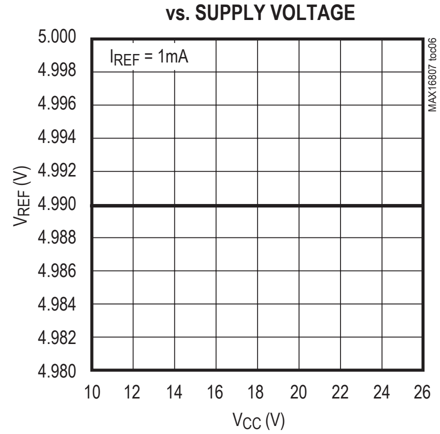
REFERENCE VOLTAGE vs. TEMPERATURE



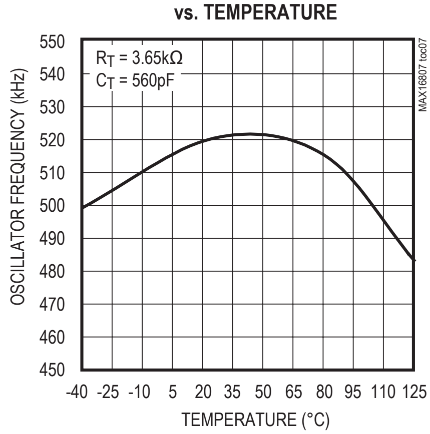
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



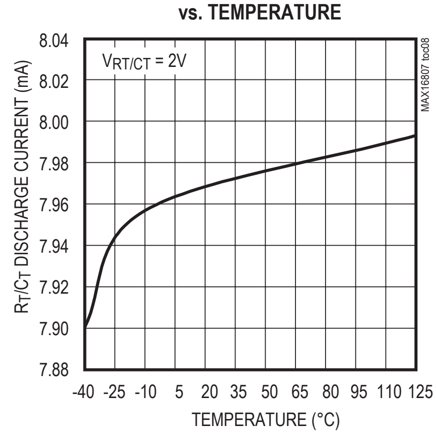
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



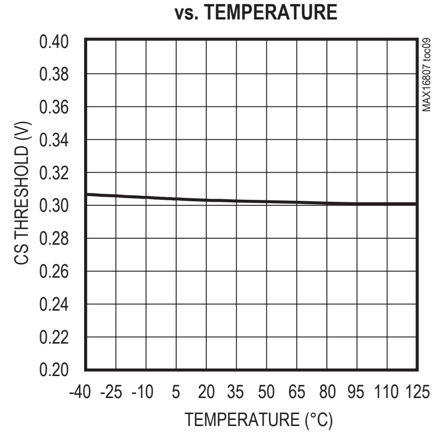
OSCILLATOR FREQUENCY (f_{OSC}) vs. TEMPERATURE



OSCILLATOR R_T/C_T DISCHARGE CURRENT vs. TEMPERATURE



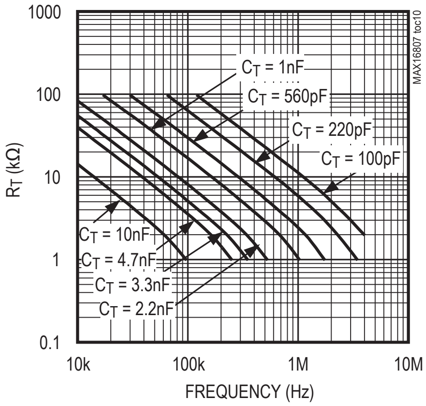
CURRENT-SENSE TRIP THRESHOLD vs. TEMPERATURE



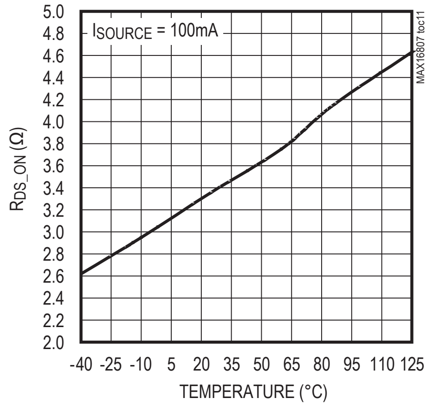
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, V_{CS} = V_{AGND} = V_{PGND} = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

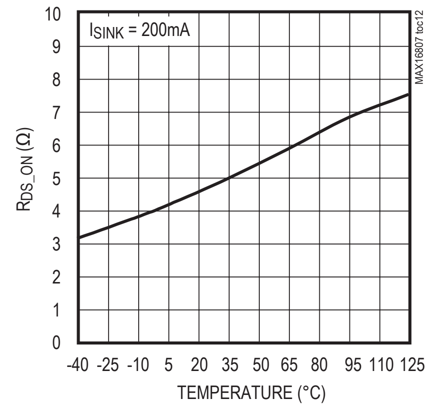
TIMING RESISTANCE vs. OSCILLATOR FREQUENCY



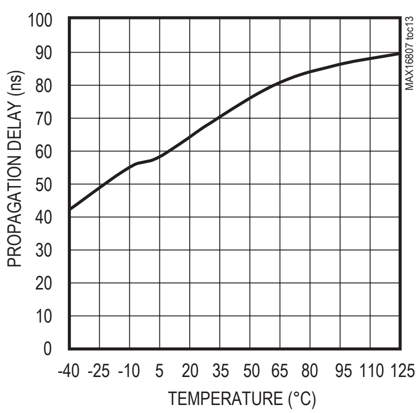
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} PMOS DRIVER)



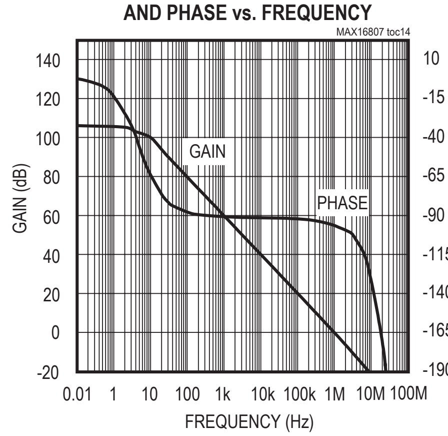
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} NMOS DRIVER)



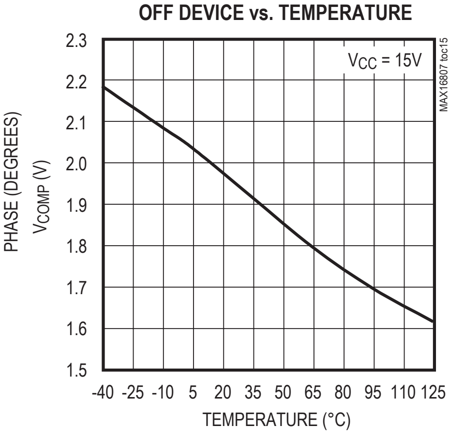
PROPAGATION DELAY FROM CURRENT-LIMIT COMPARATOR TO OUT vs. TEMPERATURE



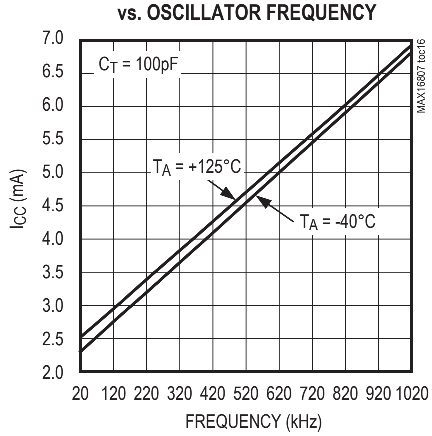
ERROR-AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



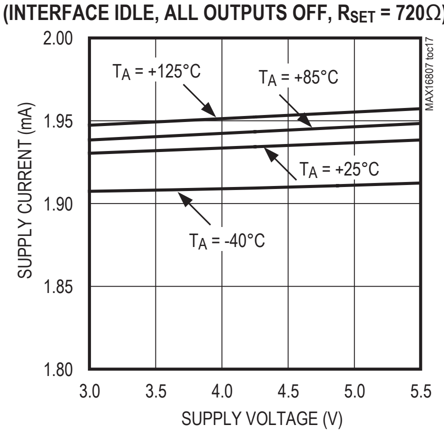
COMP VOLTAGE LEVEL TO TURN OFF DEVICE vs. TEMPERATURE



SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



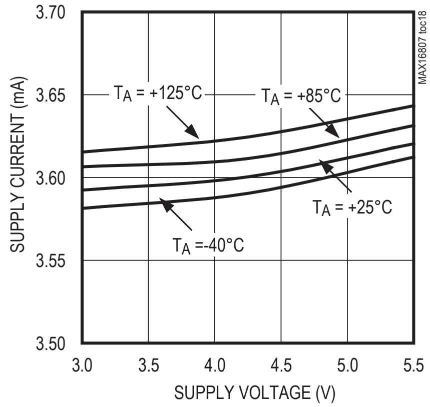
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS OFF, R_{SET} = 720Ω)



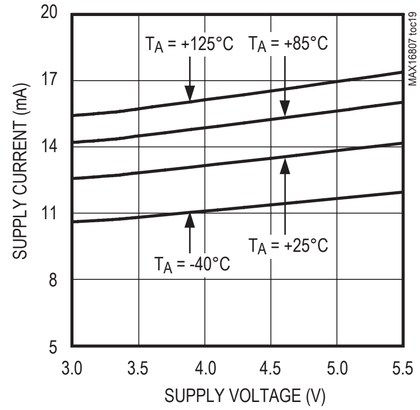
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1μF, V_{FB} = 2V, V_{CS} = V_{AGND} = V_{PGND} = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

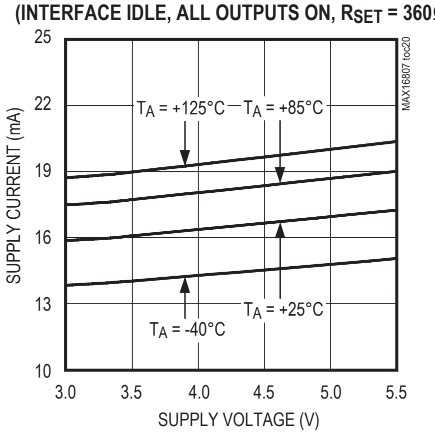
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS OFF, R_{SET} = 360Ω)



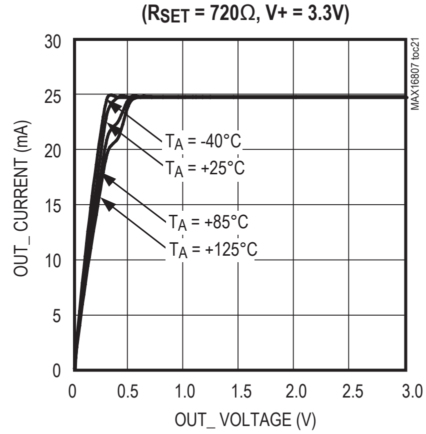
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS ON, R_{SET} = 720Ω)



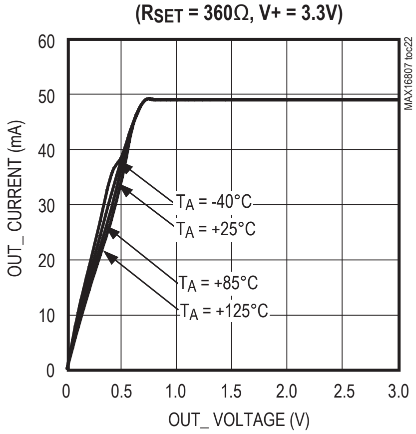
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS ON, R_{SET} = 360Ω)



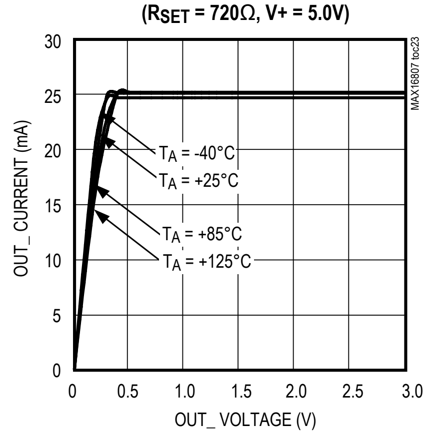
OUT_ CURRENT vs. OUT_ VOLTAGE (R_{SET} = 720Ω, V+ = 3.3V)



OUT_ CURRENT vs. OUT_ VOLTAGE (R_{SET} = 360Ω, V+ = 3.3V)

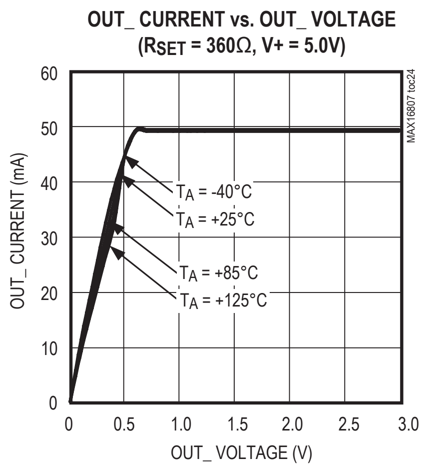


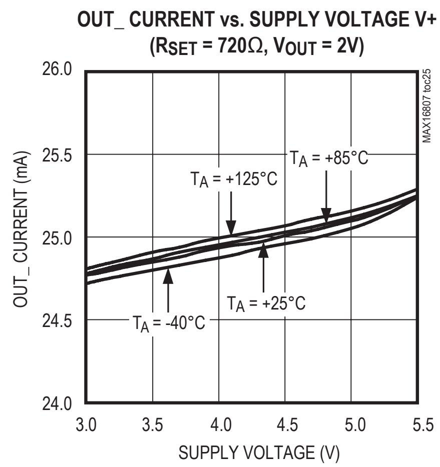
OUT_ CURRENT vs. OUT_ VOLTAGE (R_{SET} = 720Ω, V+ = 5.0V)

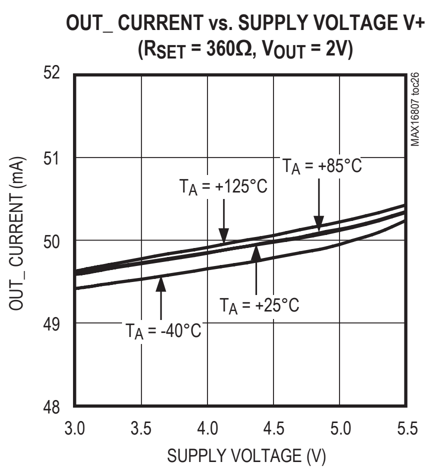


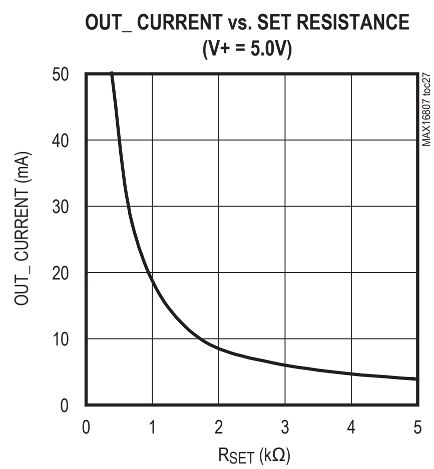
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, V_{CS} = V_{AGND} = V_{PGND} = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1, 13, 28	N.C.	No Connection. Not internally connected. Leave unconnected.
2	AGND	Analog Ground
3	OUT	MOSFET Driver Output OUT. Connects to the gate of the external n-channel MOSFET.
4	V_{CC}	Power-Supply Input. Bypass V_{CC} to AGND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor.
5	REF	5V Reference Output. Bypass REF to AGND with a 0.1µF ceramic capacitor.
6–9	OUT4–OUT7	LED Driver Outputs. OUT4–OUT7 are open-drain, constant-current-sinking outputs rated for 36V.
10	$\overline{OE}$	Active-Low Output Enable Input. Drive $\overline{OE}$ low to PGND to enable the OUT0–OUT7. Drive $\overline{OE}$ high to disable OUT0–OUT7.
11	DOUT	Serial-Data Output. Data is clocked out of the 8-bit internal shift register to DOUT on CLK's rising edge.
12	SET	LED Current Setting. Connect R_{SET} from SET to PGND to set the LED current.
14	V+	LED Driver Positive Supply Voltage. Bypass V+ to PGND with a 0.1µF ceramic capacitor.
15, 16	PGND	Power Ground
17	DIN	Serial-Data Input
18	CLK	Serial-Clock Input
19	LE	Latch-Enable Input. Data is loaded transparently from the internal shift register(s) to the output latch(es) while LE is high. Data is latched into the output latch(es) on LE's falling edge, and retained while LE is low.
20–23	OUT0–OUT3	LED Driver Outputs. OUT0–OUT3 are open-drain, constant-current-sinking outputs rated for 36V.
24	COMP	Error-Amplifier Output
25	FB	Error-Amplifier Inverting Input
26	CS	PWM Controller Current-Sense Input
27	RTCT	PWM Controller Timing Resistor/Capacitor Connection. A resistor R_T from RTCT to REF and a capacitor C_T from RTCT to AGND set the oscillator frequency.
—	EP	Exposed Pad. Connect to the ground plane for improved power dissipation. Do not use as the only ground connection for the part.

Detailed Description

The MAX16807 LED driver includes an internal switch-mode controller that can be used as boost or buck-boost (SEPIC) converters to generate the voltage necessary to drive the multiple strings of LEDs. This device incorporates an integrated low-side driver, programmable oscillator (20kHz to 1MHz), error amplifier, low-voltage (300mV) current sense for higher efficiency, and a 5V reference to power up external circuitry (see Figures 1a and 1b).

The MAX16807 LED driver includes a 4-wire serial interface and a current-mode PWM controller to generate the necessary voltage for driving eight open-drain, constant-current-sinking output ports. The driver uses current-sensing feedback circuitry (not simple current mirrors) to ensure very small current variations over the full allowed range of output voltage (see the *Typical Operating Characteristics*). The 4-wire serial interface comprises an 8-bit shift register and an 8-bit transparent latch. The shift register is written through a clock input (CLK) and a data input (DIN), and the data propagates to a data output (DOUT). The data output allows multiple drivers to be cascaded and operated together. The contents of the 8-bit shift register are loaded into the transparent latch through a latch-enable input (LE). The latch is transparent to the shift-register outputs when high and latches the current state on the falling edge of LE. Each driver output is an open-drain, constant-current sink that should be connected to the cathode of a string of LEDs connected in series. The constant-current capability is up to 55mA per output, set for all eight outputs by an external resistor (R_{SET}). The device can operate in stand-alone mode (see the *Typical Operating Circuits.*)

The number of channels can be expanded by using the MAX6970 and MAX6971 family in conjunction with the MAX16807.

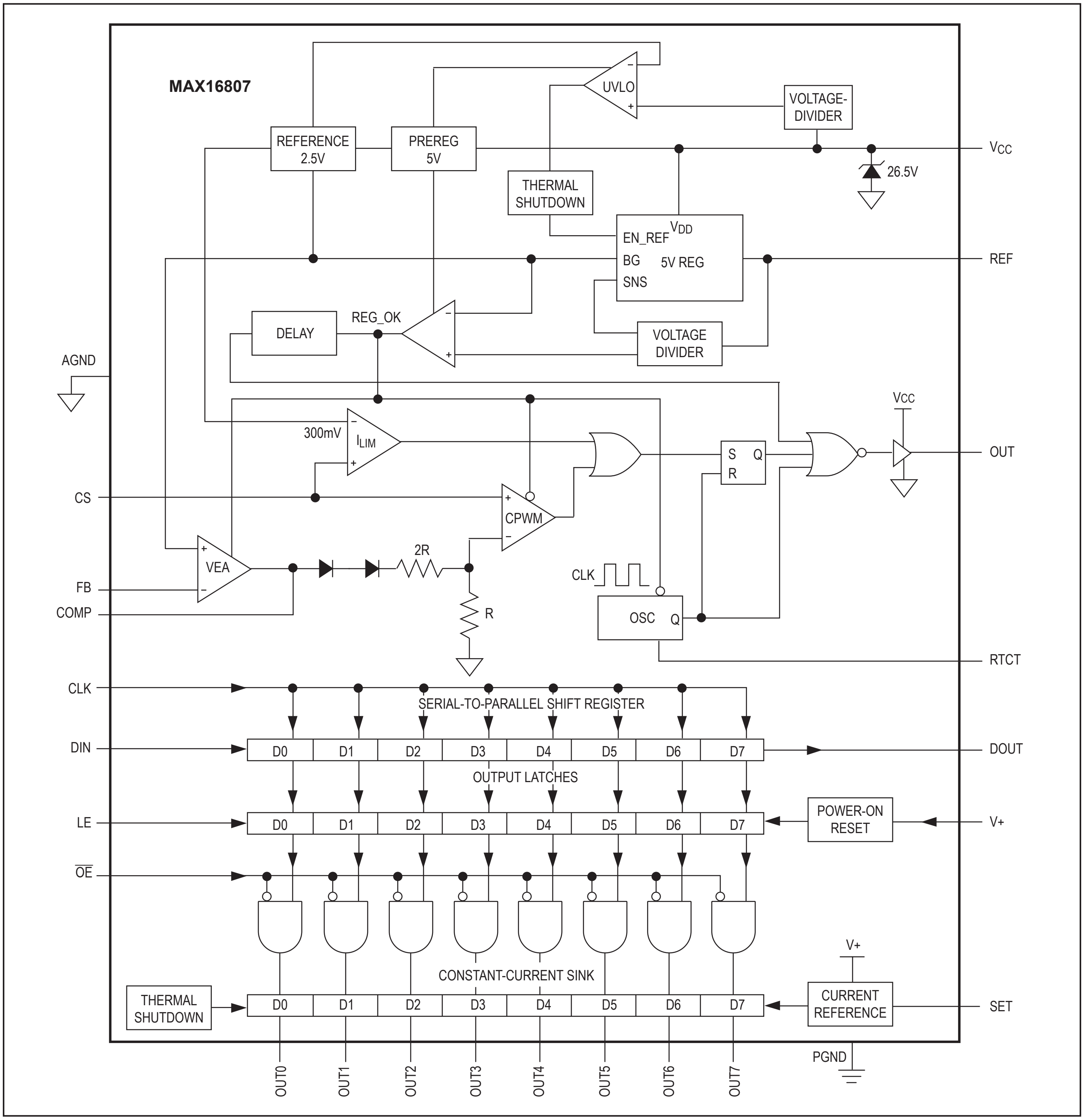


Figure 1a. Internal Block Diagram (MAX16807)

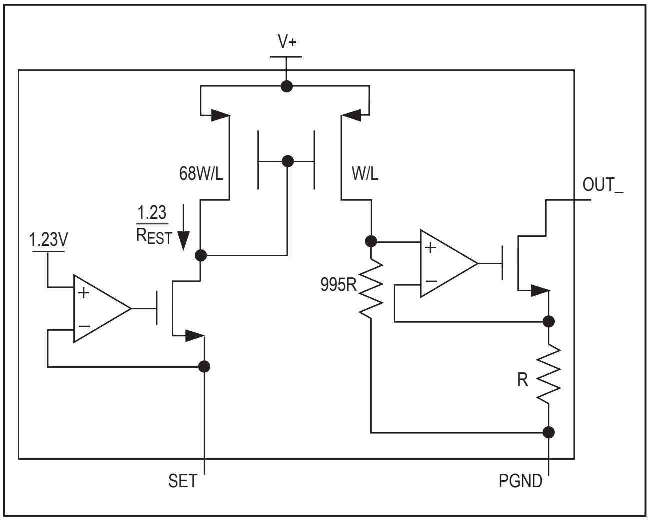


Figure 1b. OUT_ Driver Internal Diagram

Switch-Mode Controller

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in the voltage-mode control scheme. The MAX16807 uses a current-mode control loop where the output of the error amplifier is compared to the current-sense voltage (V_{CS}). When the current-sense signal is lower than the inverting input of the CPWM comparator, the output of the comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM comparator, the output is high and the switch is turned off.

Undervoltage Lockout (UVLO)

The turn-on supply voltage for the MAX16807 is 8.4V (typ). Once V_{CC} reaches 8.4V, the reference powers up. There is 0.8V of hysteresis from the turn-on voltage to the UVLO threshold. Once V_{CC} reaches 8.4V, the MAX16807 operates with V_{CC} down to 7.6V (typ). Once V_{CC} goes below 7.6V, the device is in UVLO. When in UVLO, the quiescent supply current into V_{CC} falls back to 32µA (typ), and OUT and REF are pulled low.

MOSFET Driver

OUT drives an external n-channel MOSFET and swings from AGND to V_{CC}. Ensure that V_{CC} remains below the absolute maximum V_{GS} rating of the external MOSFET. OUT is a push-pull output with the on-resistance of the pMOS (typically 3.5Ω) and the on-resistance of the nMOS (typically 4.5Ω). The driver can source 2A and sink 1A (typ). This allows for the MAX16807 to quickly turn on and off high gate-charge MOSFETs. Bypass V_{CC} with one or more 0.1µF ceramic capacitors to AGND, placed close to the V_{CC} pin. The average current sourced to drive the external MOSFET depends on the total gate charge (Q_G) and operating frequency of the converter. The power dissipation in the device is a function of the average output drive current (I_{DRIVE}). Use the following equation to calculate the power dissipation in the device due to I_{DRIVE}:

$$I_{DRIVE} = (Q_G \times f_{SW})$$

$$PD = (I_{DRIVE} + I_{CC}) \times V_{CC}$$

where I_{CC} is the operating supply current. See the *Typical Operating Characteristics* for the operating supply current at a given frequency.

Error Amplifier

The MAX16807 includes an internal error amplifier. The inverting input is at FB and the noninverting input is internally connected to a 2.5V reference. Set the output voltage using a resistive divider between the output of the converter (V_{OUT}, FB, and AGND). Use the following formula to set the output voltage:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{FB}$$

where V_{FB} = 2.5V.

Oscillator

The oscillator frequency is programmable using an external capacitor and a resistor at RTCT (see R_T and C_T in the *Typical Operating Circuits*). R_T is connected from RTCT to the 5V reference (REF), and C_T is connected from RTCT to AGND. REF charges C_T through R_T until its voltage reaches 2.8V. C_T then discharges through an 8.3mA internal current sink until C_T's voltage reaches 1.1V, at which time C_T is allowed to charge through R_T again. The oscillator's period is the sum of the charge and discharge times of C_T. Calculate the charge time as follows:

$$t_C = 0.57 \times R_T \times C_T$$

where t_C is in seconds, RT in ohms (Ω), and C_T in Farads (F).

The discharge time is then:

$$t_D = (R_T \times C_T \times 1000)/[(4.88 \times R_T) - (1.8 \times 1000)]$$

where t_D is in seconds, R_T in ohms (Ω), and C_T in Farads (F).

The oscillator frequency is then:

$$OSC \quad \frac{}{(t_C \quad t_D)}$$

Reference Output (REF)

REF is a 5V reference output that can source 20mA. Bypass REF to AGND with a 0.1µF capacitor.

Current Limit

The MAX16807 includes a fast current-limit comparator to terminate the on-cycle during an overload or a fault condition. The current-sense resistor (R_{CS}) connected between the source of the external MOSFET and AGND, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 0.3V. Use the following equation to calculate R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{P-P}}$$

I_{P-P} is the peak current that flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) turns the switch off within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the time constant of the RC filter at 50ns.

Buck-Boost (SEPIC) Operation

Figure 2 shows a buck-boost application circuit using the MAX16807 in stand-alone mode of operation. SEPIC topology is necessary when the total forward voltage of the LEDs in a string is such that V_{OUT} can be below or above V_{IN}.

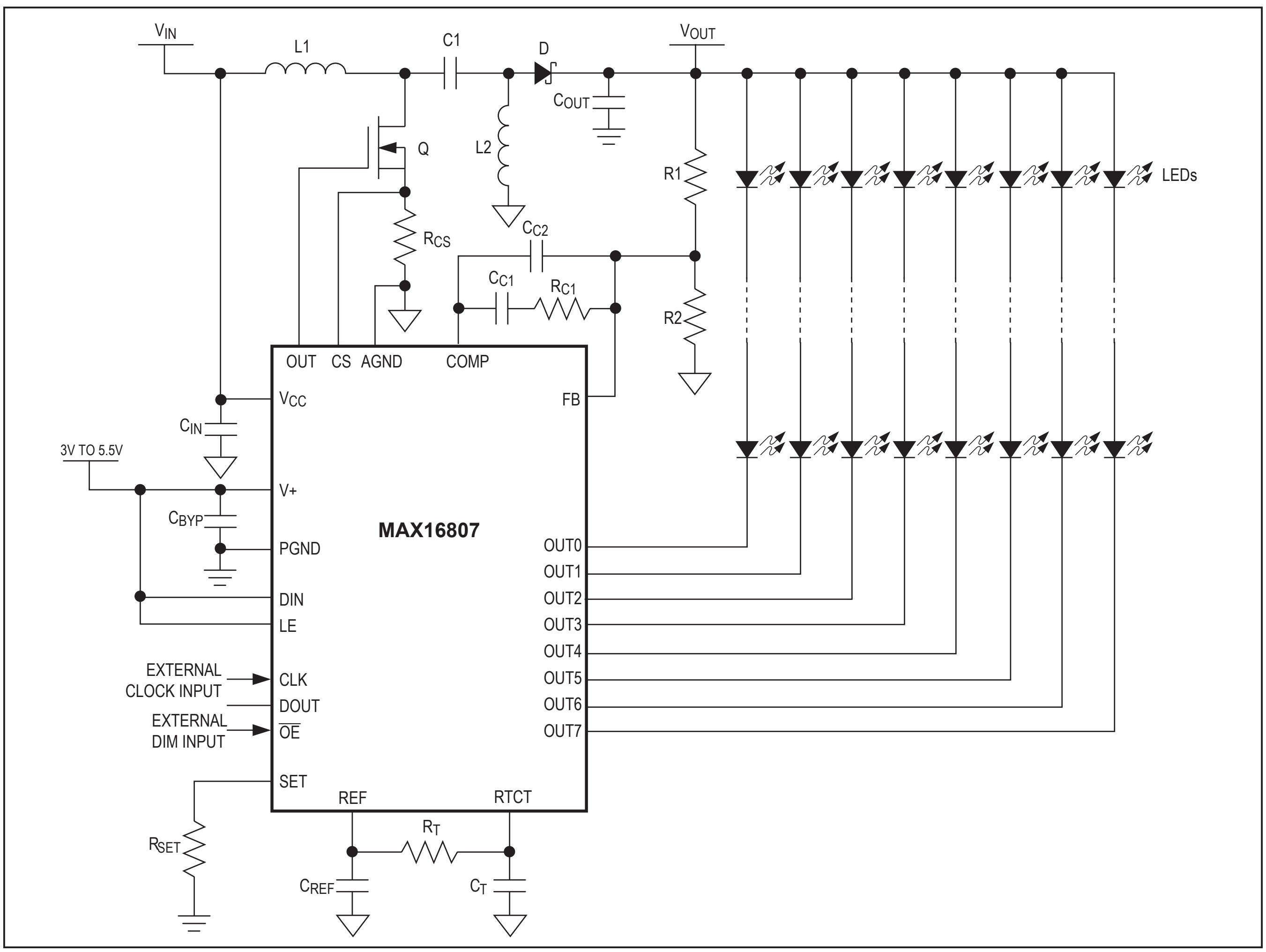


Figure 2. Buck-Boost (SEPIC) Configuration

LED Driver

4-Wire Interface

The MAX16807 also operates in stand-alone mode (see the *Typical Operating Circuits*). For use with a microcontroller, the MAX16807 features a 4-wire serial interface using DIN, CLK, LE, $\overline{OE}$ inputs and DOUT as a data output. This interface is used to write the LED channels' data to the MAX16807. The serial-interface data word length is 8 bits (D0–D7). See Figure 3.

The functions of the five interface pins are as follows:

DIN is the serial-data input, and must be stable when it is sampled on the rising edge of CLK. Data is shifted in MSB first. This means that data bit D7 is clocked in first, followed by seven more data bits, finishing with the LSB (D0).

CLK is the serial-clock input that shifts data at DIN into the MAX16807's 8-bit shift register on its rising edge.

LE is the latch-enable input of the MAX16807 that transfers data from the 8-bit shift register to its 8-bit output latch (transparent latch). The data is latched on the falling edge of LE (Figure 4). The fourth input ($\overline{OE}$) provides output-enable control of the output drivers. When $\overline{OE}$ is driven high, the outputs (OUT0–OUT7) are forced to high impedance without altering the contents of the output latches. Driving $\overline{OE}$ low enables the outputs to follow the state of the output latches. $\overline{OE}$ is independent of the operation of the serial interface operation. Data can be shifted into the serial-interface shift register and latched, regardless of the state of $\overline{OE}$. DOUT is the serial-data output that shifts data out from the MAX16807's 8-bit shift register on the rising edge of CLK. Data at DIN propagates through the shift register and appears at DOUT eight clock cycles later. Table 1 shows the 4-wire serial-interface truth table.

Selecting External Component R_{SET} to Set LED Output Current

The MAX16807 uses an external resistor (R_{SET}) to set the LED current for outputs OUT0–OUT7. The minimum allowed value of R_{SET} is 330Ω, which sets the output currents to 55mA. The maximum allowed value of R_{SET} is 5kΩ ($I_{OUT\_}$ = 3.6mA) and the maximum allowed capacitance at SET is 100pF.

Use the following formula to set the output current:

$$R_{SET} = \frac{18{,}000}{I_{OUT\_}}$$

where $I_{OUT\_}$ is the desired output current in milliamps and the value for R_{SET} is in ohms.

Overtemperature Cutoff

The MAX16807 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds +165°C. The outputs are enabled again when the die temperature drops below +140°C. Register contents are not affected, so when a driver is overdissipating, the external symptom is the load LEDs cycling on and off as the driver repeatedly overheats and cools, alternately turning itself off and then back on again.

Table 1. 4-Wire Serial-Interface Truth Table

SERIAL DATA INPUT DIN	CLOCK INPUT	SHIFT REGISTER CONTENTS						LOAD INPUT	LATCH CONTENTS						BLANKING INPUT	OUTPUT CONTENTS CURRENT AT OUT_					
	CLK	D0	D1	D2	…	Dn-1	Dn	LE	D0	D1	D2	…	Dn-1	Dn	$\overline{OE}$	D0	D1	D2	…	Dn-1	Dn
H	↑	H	R0	R1	…	Rn-2	Rn-1														
L	↑	L	R0	R1	…	Rn-2	Rn-1														
X	↓	R0	R1	R2	…	Rn-1	Rn														
		X	X	X	…	X	X	L	R0	R1	R2	…	Rn-1	Rn							
		P0	P1	P2	…	Pn-1	Pn	H	P0	P1	P2	…	Pn-1	Pn	L	P0	P1	P2	…	Pn-1	Pn
									X	X	X	…	X	X	H	L	L	L	…	L	L

L = Low Logic Level
H = High Logic Level
X = Don't Care
P = Present State (Shift Register)
R = Previous State (Latched)

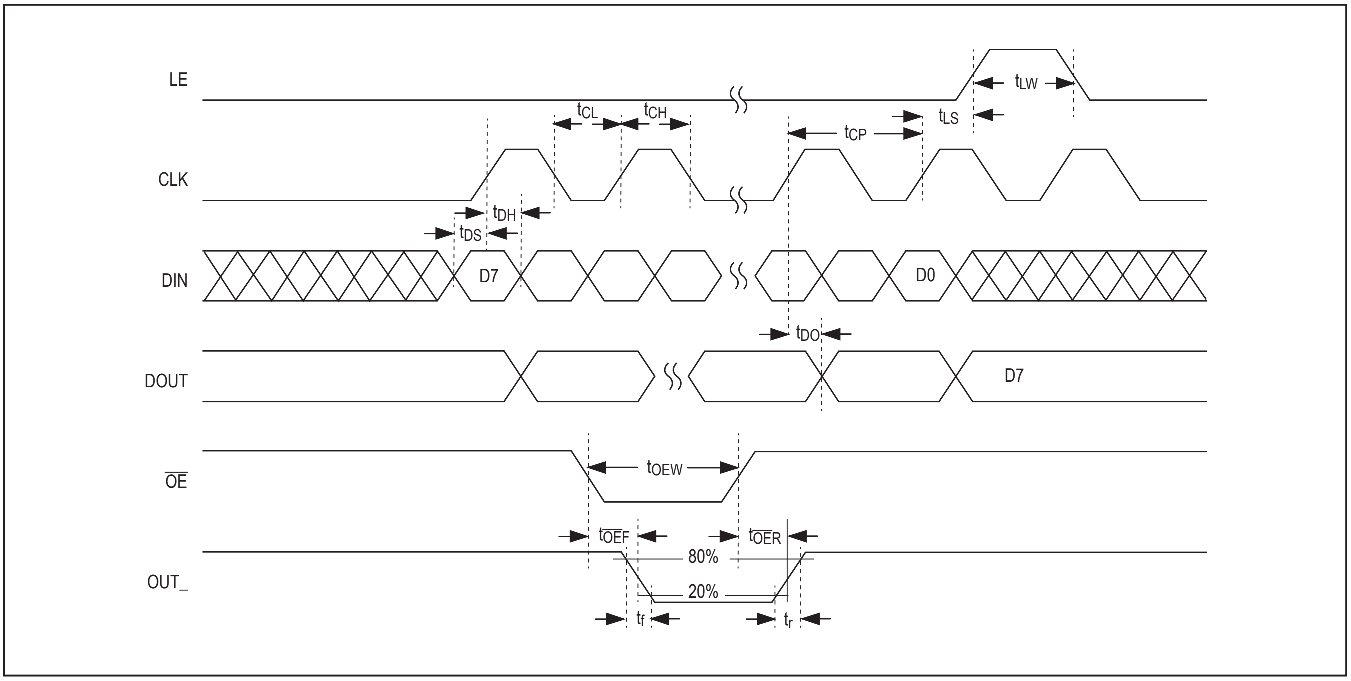


Figure 3. 4-Wire Serial-Interface Timing Diagram

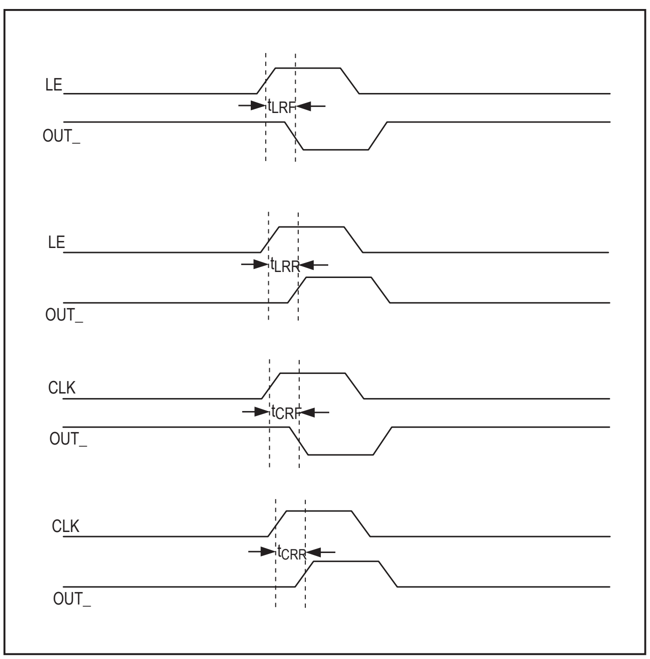


Figure 4. LE and CLK to OUT_ Timing

Stand-Alone Operation

In stand-alone operation, the MAX16807 does not use the 4-wire interface (see the *Typical Operating Circuits*). Connecting DIN and LE to V+ provides at least eight external clock pulses to CLK to enable the R_{SET} outputs. This startup pulse sequence can be provided either using an external clock or the PWM signal. The external clock can also be generated using the signal at RTCT and an external comparator.

LED Dimming

PWM Dimming

All the output channels can be dimmed simultaneously by applying a PWM signal (50Hz to 30kHz) to $\overline{OE}$. This allows for a wide range of dimming up to a 5000:1 ratio. Each channel can be independently turned on and off using a 4-wire serial interface. The dimming is proportional to the PWM duty cycle.

LED Current-Amplitude Adjustment

Using an analog or digital potentiometer as R_{SET} allows for LED current-amplitude adjustment and linear dimming.

Computing Power Dissipation

Use the following equation to estimate the upper-limit power dissipation (PD) for the MAX16807:

$$PD = DUTY \times \left[(V+ \times I+) + \sum_{i=0}^{i=7} V_{OUTi} \times I_{OUTi} \right] + (V_{CC} \times I_{CC})$$

where:

V+ = Supply voltage

I+ = Operating supply current

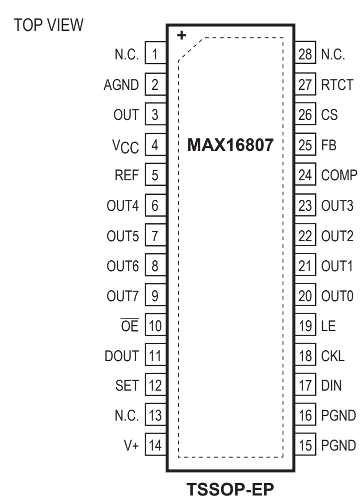
DUTY = PWM duty cycle applied to $\overline{OE}$

V_{OUTi} = MAX16807 port output voltage when driving load LED(s)

I_{OUTi} = LED drive current programmed by R_{SET}

PD = Power dissipation

Pin Configuration



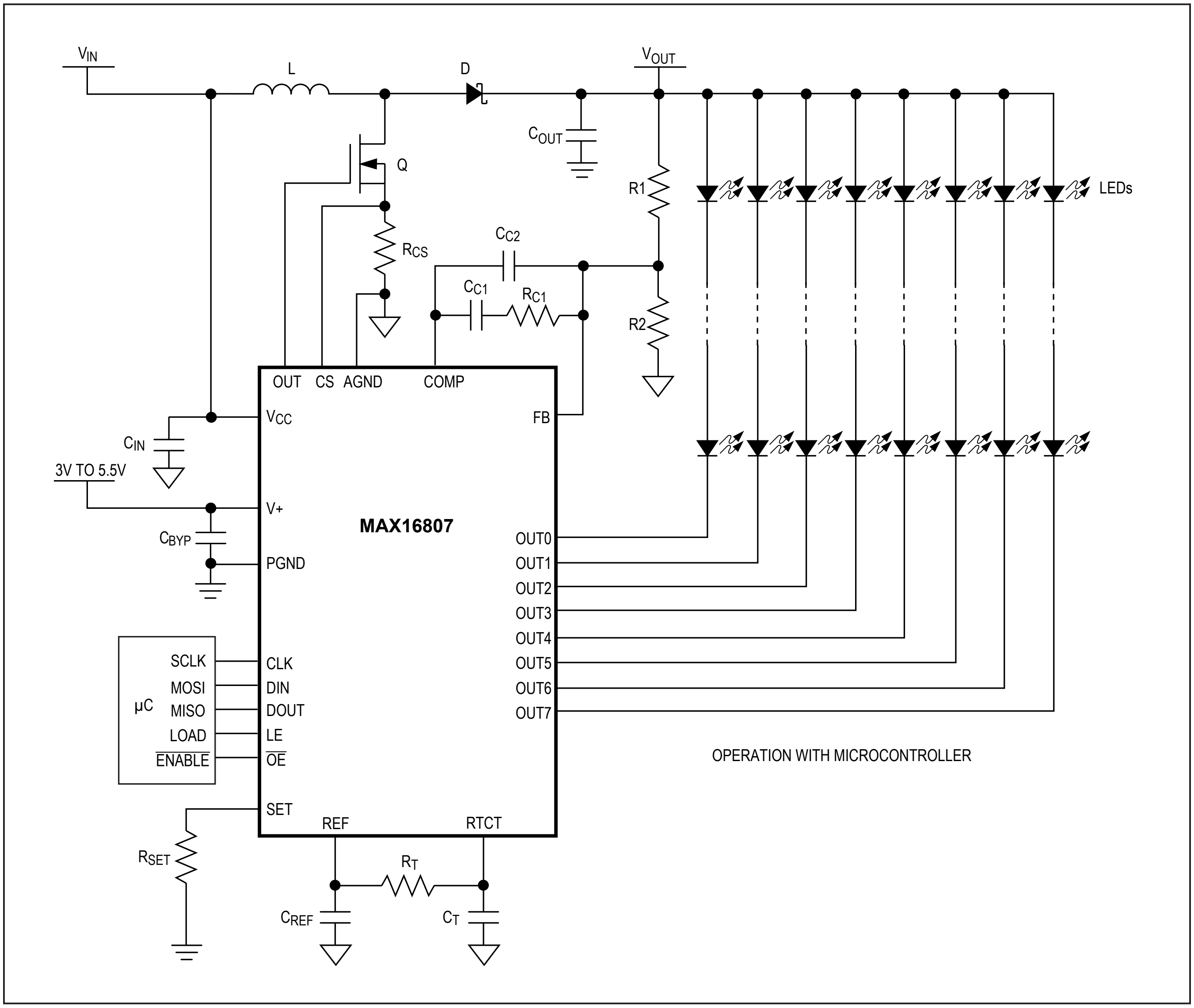
PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting AGND, PGND, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). Also, minimize trace lengths to reduce stray capacitance, trace resistance, and radiated noise. The trace between the output voltage-divider and the FB pin must be kept short, as well as the trace between AGND and PGND.

Chip Information

PROCESS: BiCMOS

Typical Operating Circuits (continued)



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	U28ME+1	21-0108

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/06	Initial release	—
1	4/07	Release of the MAX16808	1
2	8/09	Removal of the MAX16808 from the data sheet.	1–21
3	11/14	No /V OPN in *Ordering Information*, removed automotive reference in *Applications* section	1

