



Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

General Description

The MAX199 multi-range, 12-bit data-acquisition system (DAS) requires only a single +5V supply for operation, and converts analog signals up to $\pm 4V$ at its inputs. This system provides eight analog input channels that are independently software programmable for a variety of ranges: $\pm V_{REF}$, $\pm V_{REF}/2$, $0V$ to V_{REF} , or $0V$ to $V_{REF}/2$. This increases effective dynamic range to 14 bits, and provides the user flexibility to interface 4mA-to-20mA, $\pm 12V$, and $\pm 15V$ powered sensors to a single +5V system. In addition, the converter is fault-protected to $\pm 16.5V$; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, 100ksps throughput rate, internal/external clock, internal/external acquisition control, 8+4 parallel interface, and operation with an internal 4.096V or external reference.

A hardware \overline{SHDN} pin and two programmable power-down modes (STBYPD, FULLPD) provide low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX199 employs a standard microprocessor (μP) interface. Its three-state data I/O interface is configured to operate with 8-bit data buses, and data-access and bus-release timing specifications are compatible with most popular μPs . All logic inputs and outputs are TTL/CMOS compatible.

The MAX199 is available in 28-pin DIP, wide SO, SSOP, and ceramic SB packages.

For a different combination of input ranges ($\pm 10V$, $\pm 5V$, $0V$ to $10V$, $0V$ to $5V$), see the MAX197 data sheet. For 12-bit bus interfaces, see the MAX196/MAX198 data sheet.

Applications

- Industrial-Control Systems
- Robotics
- Data-Acquisition Systems
- Automatic Testing Systems
- Medical Instruments
- Telecommunications

Functional Diagram appears at end of data sheet.

Features

- ◆ 12-Bit Resolution, 1/2LSB Linearity
- ◆ Single +5V Operation
- ◆ Software-Selectable Input Ranges: $\pm V_{REF}$, $\pm V_{REF}/2$, $0V$ to V_{REF} , $0V$ to $V_{REF}/2$
- ◆ Internal 4.096V or External Reference
- ◆ Fault-Protected Input Multiplexer ($\pm 16.5V$)
- ◆ 8 Analog Input Channels
- ◆ 6 μs Conversion Time, 100ksps Sampling Rate
- ◆ Internal or External Acquisition Control
- ◆ Two Power-Down Modes
- ◆ Internal or External Clock

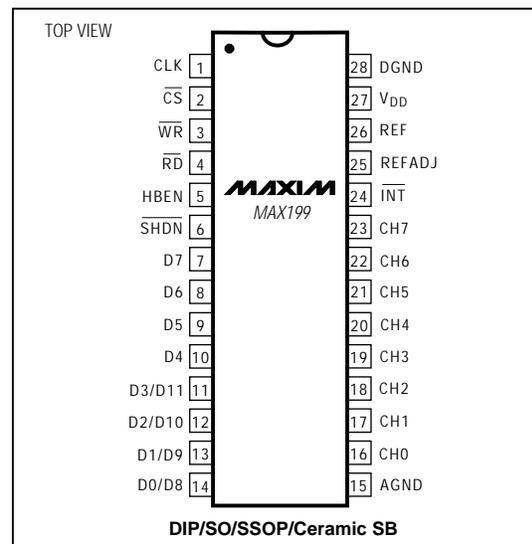
Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|--------------|-----------------------|
| MAX199ACNI | 0°C to +70°C | 28 Narrow Plastic DIP |
| MAX199BCNI | 0°C to +70°C | 28 Narrow Plastic DIP |
| MAX199ACWI | 0°C to +70°C | 28 Wide SO |
| MAX199BCWI | 0°C to +70°C | 28 Wide SO |
| MAX199ACAI | 0°C to +70°C | 28 SSOP |
| MAX199BCAI | 0°C to +70°C | 28 SSOP |
| MAX199BC/D | 0°C to +70°C | Dice* |

Ordering Information continued at end of data sheet.

*Dice are specified at $T_A = +25^\circ C$, DC parameters only.

Pin Configuration



Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|-----------------------------------|--|-----------------|
| V _{DD} to AGND..... | -0.3V to +7V | Wide SO (derate 12.50mW/°C above +70°C)..... | 1000mW |
| AGND to DGND..... | -0.3V to +0.3V | SSOP (derate 9.52mW/°C above +70°C)..... | 762mW |
| REF to AGND..... | -0.3V to (V _{DD} + 0.3V) | Narrow Ceramic SB (derate 20.00mW/°C above +70°C)..... | 1600mW |
| REFADJ to AGND..... | -0.3V to (V _{DD} + 0.3V) | Operating Temperature Ranges | |
| Digital Inputs to DGND..... | -0.3V to (V _{DD} + 0.3V) | MAX199_C_..... | 0°C to +70°C |
| Digital Outputs to DGND..... | -0.3V to (V _{DD} + 0.3V) | MAX199_E_..... | -40°C to +85°C |
| CH0-CH7 to AGND..... | $\pm 16.5V$ | MAX199_M_..... | -55°C to +125°C |
| Continuous Power Dissipation (T _A = +70°C) | | Storage Temperature Range..... | -65°C to +150°C |
| Narrow Plastic DIP (derate 14.29mW/°C above +70°C)..... | 1143mW | Lead Temperature (soldering, 10sec)..... | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V $\pm 5\%$; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7 μ F at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--------|---|---------|-----|-----|-----------|--------|
| ACCURACY (Note 1) | | | | | | | |
| Resolution | | | | 12 | | | Bits |
| Integral Nonlinearity | INL | MAX199A | | | | $\pm 1/2$ | LSB |
| | | MAX199B | | | | ± 1 | |
| Differential Nonlinearity | DNL | | | | | ± 1 | LSB |
| Offset Error | | Unipolar | MAX199A | | | ± 3 | LSB |
| | | | MAX199B | | | ± 5 | |
| | | Bipolar | MAX199A | | | ± 5 | |
| | | | MAX199B | | | ± 10 | |
| Channel-to-Channel Offset Error Matching | | Unipolar | | | | ± 0.1 | LSB |
| | | Bipolar | | | | ± 0.5 | |
| Gain Error (Note 2) | | Unipolar | MAX199A | | | ± 7 | LSB |
| | | | MAX199B | | | ± 10 | |
| | | Bipolar | MAX199A | | | ± 7 | |
| | | | MAX199B | | | ± 10 | |
| Gain Temperature Coefficient (Note 2) | | Unipolar | | | | 3 | ppm/°C |
| | | Bipolar | | | | 5 | |
| DYNAMIC SPECIFICATIONS (10kHz sine-wave input, $\pm 4.096Vp-p$, f _{SAMPLE} = 100ksps) | | | | | | | |
| Signal-to-Noise + Distortion Ratio | SINAD | | MAX199A | 70 | | | dB |
| | | | MAX199B | 69 | | | |
| Total Harmonic Distortion | THD | Up to the 5th harmonic | | | -85 | -78 | dB |
| Spurious-Free Dynamic Range | SFDR | | | 80 | | | dB |
| Channel-to-Channel Crosstalk | | 50kHz, V _{IN} = $\pm 4V$ (Note 3) | | | -86 | | dB |
| Aperture Delay | | External CLK mode/external acquisition control | | | 15 | | ns |
| Aperture Jitter | | External CLK mode/external acquisition control | | | <50 | | ps |
| | | Internal CLK mode/internal acquisition control (Note 4) | | | 10 | | ns |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|--------------|--------------------------------------|------------------------------------|-----------------|-----------|-------------|-----------------|
| ANALOG INPUT | | | | | | | |
| Track/Hold Acquisition Time | | $f_{CLK} = 2.0MHz$ | | | | 3 | μs |
| Small-Signal Bandwidth | | -3dB rolloff | $\pm V_{REF}$ range | | 5 | | MHz |
| | | | $\pm V_{REF/2}$ range | | 2.5 | | |
| | | | 0V to V_{REF} range | | 2.5 | | |
| | | | 0V to $V_{REF/2}$ range | | 1.25 | | |
| Input Voltage Range | | Unipolar (see Table 2) | | 0 | | V_{REF} | V |
| | | | | 0 | | $V_{REF/2}$ | |
| | | Bipolar (see Table 2) | | $-V_{REF}$ | | V_{REF} | |
| | | | | $-V_{REF/2}$ | | $V_{REF/2}$ | |
| Input Current | | Unipolar range | | | 0.1 | 10 | μA |
| | | Bipolar | $\pm V_{REF}$ range | -1200 | | 10 | |
| | | | $\pm V_{REF/2}$ range | -600 | | 10 | |
| Input Dynamic Resistance | | Unipolar | | | 40 | | $M\Omega$ |
| | | Bipolar | | | 10 | | $k\Omega$ |
| Input Capacitance | | (Note 5) | | | | 40 | pF |
| INTERNAL REFERENCE | | | | | | | |
| REF Output Voltage | V_{REF} | $T_A = +25^\circ C$ | | 4.076 | 4.096 | 4.116 | V |
| REF Output Tempco (Contact Maxim Applications for guaranteed temperature drift specifications) | TC V_{REF} | MAX199_C | | | ± 15 | | ppm/ $^\circ C$ |
| | | MAX199_E | | | ± 30 | | |
| | | MAX199_M | | | ± 40 | | |
| Output Short-Circuit Current | | | | | | 30 | mA |
| Load Regulation | | 0mA to 0.5mA output current (Note 6) | | | | 7.5 | mV |
| | | 0mA to 0.1mA output current (Note 6) | | | | 0.8 | |
| Capacitive Bypass at REF | | | | 4.7 | | | μF |
| REFADJ Output Voltage | | | | 2.465 | 2.500 | 2.535 | V |
| REFADJ Adjustment Range | | With recommended circuit (Figure 1) | | | ± 1.5 | | % |
| Buffer Voltage Gain | | | | | 1.6384 | | V/V |
| REFERENCE INPUT (Buffer disabled, reference input applied to REF pin) | | | | | | | |
| Input Voltage Range | | | | 2.4 | | 4.18 | V |
| Input Current | | $V_{REF} = 4.18V$ | Normal, or STANDBY power-down mode | | 400 | | μA |
| | | | FULL power-down mode | | 1 | | |
| Input Resistance | | Normal, or STANDBY power-down mode | | 10 | | | $k\Omega$ |
| | | FULL power-down mode | | 5 | | | $M\Omega$ |
| REFADJ Threshold for Buffer Disable | | | | $V_{DD} - 50mV$ | | | V |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|---|--|----------------------|--------------|------|-----------|---------|
| POWER REQUIREMENTS | | | | | | | |
| Supply Voltage | V_{DD} | | | 4.75 | | 5.25 | V |
| Supply Current | I_{DD} | Normal mode, bipolar ranges | | | | 18 | mA |
| | | Normal mode, unipolar ranges | | | 6 | 10 | |
| | | Standby power-down (STBYPD) | | | 700 | 850 | μA |
| | | Full power-down mode (FULLPD) (Note 7) | | | 60 | 120 | |
| Power-Supply Rejection Ratio (Note 8) | PSRR | External reference = 4.096V | | | | $\pm 1/2$ | LSB |
| | | Internal reference | | | | $\pm 1/2$ | |
| TIMING | | | | | | | |
| Internal Clock Frequency | f_{CLK} | $C_{CLK} = 100pF$ | | 1.25 | 1.56 | 2.00 | MHz |
| External Clock Frequency Range | f_{CLK} | | | 0.1 | | 2.0 | MHz |
| Acquisition Time | t_{ACQI} | Internal acquisition | External CLK | 3.0 | | | μs |
| | | | Internal CLK | 3.0 | | 5.0 | |
| | t_{ACQE} | External acquisition (Note 9) | | 3.0 | | | |
| Conversion Time | t_{CONV} | After FULLPD or STBYPD | | 5 | | | μs |
| | | External CLK | | 6.0 | | | |
| | | Internal CLK, $C_{CLK} = 100pF$ | | 6.0 | 7.7 | 10.0 | |
| Throughput Rate | External CLK | | | | 100 | | ksps |
| | Internal CLK, $C_{CLK} = 100pF$ | | 62 | | | | |
| Bandgap Reference Start-Up Time | | Power-up (Note 10) | | 200 | | | μs |
| Reference Buffer Settling | To 0.1mV, REF bypass capacitor fully discharged | | $C_{REF} = 4.7\mu F$ | 8 | | | ms |
| | | | $C_{REF} = 33\mu F$ | 60 | | | |
| DIGITAL INPUTS (D7–D0, CLK, \overline{RD} , \overline{WR} , CS, HBEN, SHDN) (Note 11) | | | | | | | |
| Input High Voltage | V_{INH} | | | 2.4 | | | V |
| Input Low Voltage | V_{INL} | | | | | 0.8 | V |
| Input Leakage Current | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | | ± 10 | μA |
| Input Capacitance | C_{IN} | (Note 5) | | | | 15 | pF |
| DIGITAL OUTPUTS (D7–D4, D3/D11, D2/D10, D1/D9, D0/D8, \overline{INT}) | | | | | | | |
| Output Low Voltage | V_{OL} | $V_{DD} = 4.75V$, $I_{SINK} = 1.6mA$ | | | | 0.4 | V |
| Output High Voltage | V_{OH} | $V_{DD} = 4.75V$, $I_{SOURCE} = 1mA$ | | $V_{DD} - 1$ | | | V |
| Three-State Output Capacitance | C_{OUT} | (Note 5) | | | | 15 | pF |

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TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|-----------------------------------|-----|-----|-----|-------|
| \overline{CS} Pulse Width | t_{CS} | | 80 | | | ns |
| \overline{WR} Pulse Width | t_{WR} | | 80 | | | ns |
| \overline{CS} to \overline{WR} Setup Time | t_{CSWS} | | 0 | | | ns |
| \overline{CS} to \overline{WR} Hold Time | t_{CSWH} | | 0 | | | ns |
| \overline{CS} to \overline{RD} Setup Time | t_{CSRS} | | 0 | | | ns |
| \overline{CS} to \overline{RD} Hold Time | t_{CSRH} | | 0 | | | ns |
| CLK to \overline{WR} Setup Time | t_{CWS} | | | | 100 | ns |
| CLK to \overline{WR} Hold Time | t_{CWH} | | | | 50 | ns |
| Data Valid to \overline{WR} Setup | t_{DS} | | 60 | | | ns |
| Data Valid to \overline{WR} Hold | t_{DH} | | 0 | | | ns |
| \overline{RD} Low to Output Data Valid | t_{DO} | Figure 2, $C_L = 100pF$ (Note 12) | | | 120 | ns |
| HBEN High or HBEN Low to Output Valid | t_{DO1} | Figure 2, $C_L = 100pF$ (Note 12) | | | 120 | ns |
| \overline{RD} High to Output Disable | t_{TR} | (Note 13) | | | 70 | ns |
| \overline{RD} Low to \overline{INT} High Delay | t_{INT1} | | | | 120 | ns |

Note 1: Accuracy specifications tested at $V_{DD} = 5.0V$. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the $\pm 4.096V$ input range.

Note 2: External reference: $V_{REF} = 4.096V$, offset error nulled, ideal last code transition = $FS - 3/2LSB$.

Note 3: Ground "on" channel; sine wave applied to all "off" channels.

Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.

Note 5: Guaranteed by design. Not tested.

Note 6: Use static loads only.

Note 7: Tested using internal reference.

Note 8: PSRR measured at full-scale. $V_{DD} = 4.75V$ to $5.25V$.

Note 9: External acquisition timing: starts at rising edge of \overline{WR} with control bit ACQMOD = low; ends at rising edge of \overline{WR} with ACQMOD = high.

Note 10: Not subject to production testing. Provided for design guidance only.

Note 11: All input control signals specified with $t_R = t_F = 5ns$ from a voltage level of 0.8V to 2.4V.

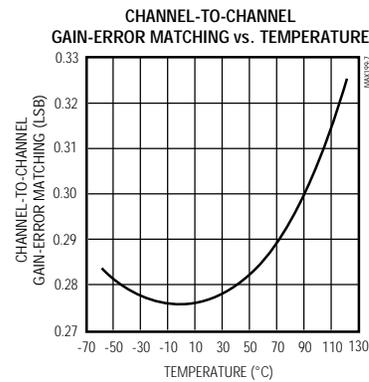
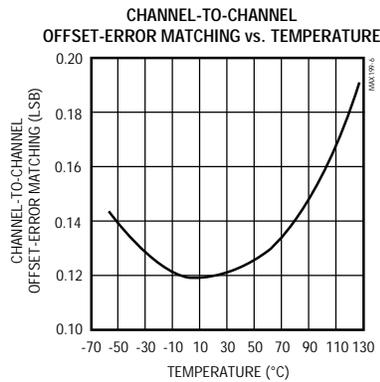
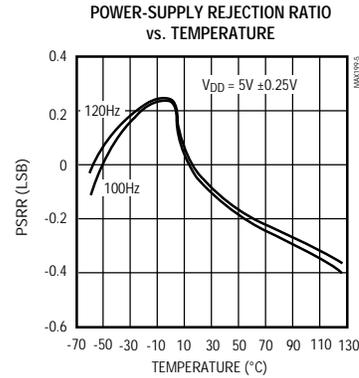
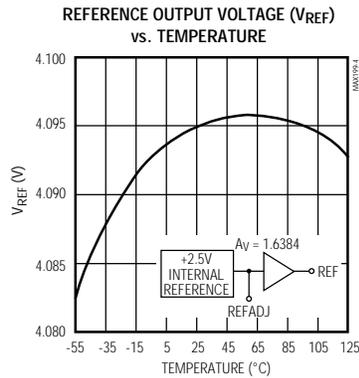
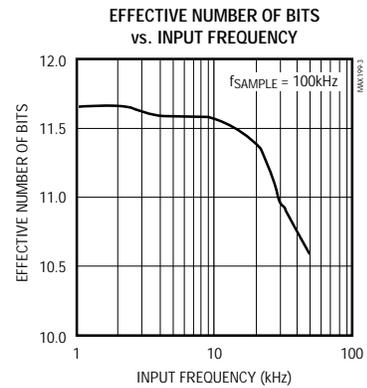
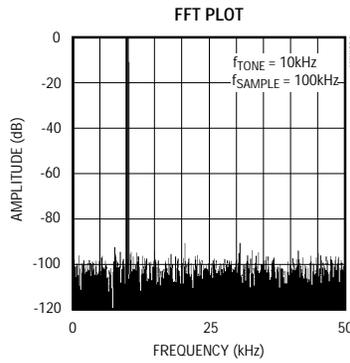
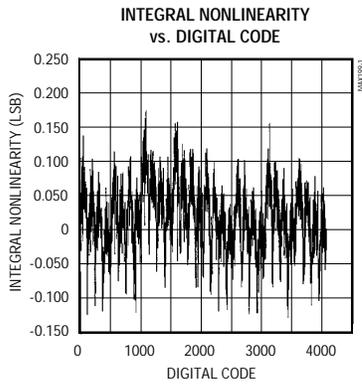
Note 12: t_{DO} and t_{DO1} are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

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Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)



Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Pin Description

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| PIN | NAME | FUNCTION |
|-------|-------------------|--|
| 1 | CLK | Clock Input. In external clock mode, drive CLK with a TTL/CMOS compatible clock. In internal clock mode, place a capacitor (C_{CLK}) from this pin to ground to set the internal clock frequency; $f_{CLK} = 1.56\text{MHz}$ typical with $C_{CLK} = 100\text{pF}$. |
| 2 | \overline{CS} | Chip Select, active low. |
| 3 | \overline{WR} | When \overline{CS} is low, in the internal acquisition mode, a rising edge on \overline{WR} latches in configuration data and starts an acquisition plus a conversion cycle. When \overline{CS} is low, in the external acquisition mode, the first rising edge on \overline{WR} starts an acquisition and a second rising edge on \overline{WR} ends acquisition and starts a conversion cycle. |
| 4 | \overline{RD} | When \overline{CS} is low, a falling edge on \overline{RD} will enable a read operation on the data bus. |
| 5 | HBEN | Used to multiplex the 12-bit conversion result. When high, the 4 MSBs are multiplexed on the data bus; when low, the 8 LSBs are available on the bus. |
| 6 | \overline{SHDN} | Shutdown. Puts the device into full power-down (FULLPD) mode when pulled low. |
| 7–10 | D7–D4 | Three-State Digital I/O |
| 11 | D3/D11 | Three-State Digital I/O. D3 output (HBEN = low), D11 output (HBEN = high). |
| 12 | D2/D10 | Three-State Digital I/O. D2 output (HBEN = low), D10 output (HBEN = high). |
| 13 | D1/D9 | Three-State Digital I/O. D1 output (HBEN = low), D9 output (HBEN = high). |
| 14 | D0/D8 | Three-State Digital I/O. D0 output (HBEN = low), D8 output (HBEN = high). D0 = LSB. |
| 15 | AGND | Analog Ground |
| 16–23 | CH0–CH7 | Analog Input Channels |
| 24 | \overline{INT} | \overline{INT} goes low when conversion is complete and output data is ready. |
| 25 | REFADJ | Bandgap Voltage-Reference Output / External Adjust Pin. Bypass with a $0.01\mu\text{F}$ capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin. |
| 26 | REF | Reference Buffer Output / ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD} . |
| 27 | V_{DD} | +5V Supply. Bypass with $0.1\mu\text{F}$ capacitor to AGND. |
| 28 | DGND | Digital Ground |

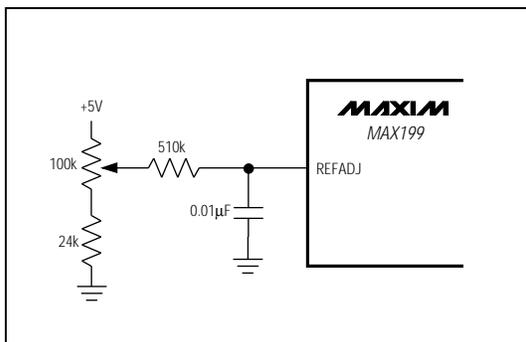


Figure 1. Reference-Adjust Circuit

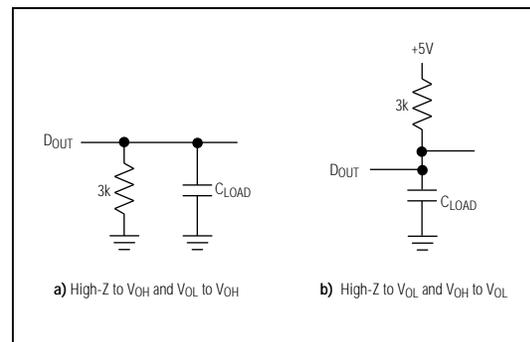


Figure 2. Load Circuits for Enable Time

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Detailed Description

Converter Operation

The MAX199, a multi-range, fault-tolerant ADC, uses successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The parallel-output format provides easy interface to microprocessors (μ Ps). Figure 3 shows the MAX199 in its simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on \overline{WR} 's rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. In bipolar mode, a low-impedance input source, which settles in less than 1.5μ s, is required to maintain conversion accuracy at the maximum conversion rate.

When configured for unipolar mode, the input does not need to be driven from a low-impedance source. The acquisition time (t_{AZ}) is a function of the source output resistance (R_S), the channel input resistance (R_{IN}), and the T/H capacitance.

Acquisition time is calculated by:

$$\text{For } 0V \text{ to } V_{REF}: t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF$$

$$\text{For } 0V \text{ to } V_{REF}/2: t_{AZ} = 9 \times (R_S + R_{IN}) \times 32pF$$

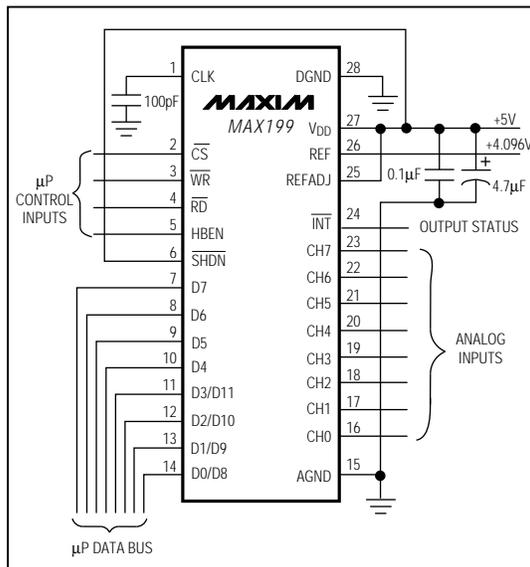


Figure 3. Operational Diagram

where $R_{IN} = 7k\Omega$, and t_{AZ} is never less than 2μ s (0V to V_{REF} range) or 3μ s (0V to $V_{REF}/2$ range).

In the external acquisition control mode ($D5 = 1$), the T/H enters its tracking mode on the first \overline{WR} rising edge and enters its hold mode when it detects the second \overline{WR} rising edge with $D5 = 0$. See the *External Acquisition* section.

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. The MAX199 can be programmed for input ranges of $\pm V_{REF}$, $\pm V_{REF}/2$, 0V to V_{REF} , or 0V to $V_{REF}/2$ by setting the appropriate control bits ($D3$, $D4$) in the control byte (see Tables 1 and 2). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ ($2.4V < V_{REF} < 4.18V$).

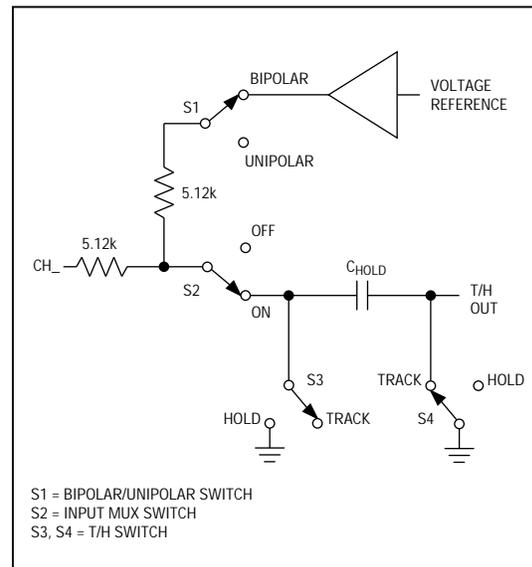


Figure 4. Equivalent Input Circuit

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The input channels are overvoltage protected to $\pm 16.5V$. This protection is active even if the device is in power-down mode.

Even with $V_{DD} = 0V$, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a μP . \overline{CS} , \overline{WR} , and \overline{RD} control the write and read operations. \overline{CS} is the standard chip-select signal, which enables a μP to address the MAX199 as an I/O port. When high, it disables the \overline{WR} and \overline{RD} inputs and forces the interface into a high-Z state.

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 1 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and two's-complement binary in bipolar mode. When reading the output data, \overline{CS} and \overline{RD} must be low. When HBEN is low, the lower eight bits are read. When HBEN is high, the upper four MSBs are available and the output data bits D4–D7 are either set low (in unipolar mode) or set to the value of the MSB (in bipolar mode) (Table 5).

Table 1. Control-Byte Format

| D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) |
|----------|-----|--------|-----|-----|----|----|----------|
| PD1 | PD0 | ACQMOD | RNG | BIP | A2 | A1 | A0 |

| BIT | NAME | DESCRIPTION |
|---------|------------|---|
| 7, 6 | PD1, PD0 | These two bits select the clock and power-down modes (Table 3). |
| 5 | ACQMOD | 0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition |
| 4 | RNG | Selects the full-scale voltage magnitude at the input (Table 2). |
| 3 | BIP | Selects unipolar or bipolar conversion mode (Table 2). |
| 2, 1, 0 | A2, A1, A0 | These are address bits for the input mux to select the "on" channel (Table 4). |

Table 2. Range and Polarity Selection

| BIP | RNG | INPUT RANGE (V) |
|-----|-----|------------------|
| 0 | 0 | 0 to $V_{REF}/2$ |
| 0 | 1 | 0 to V_{REF} |
| 1 | 0 | $\pm V_{REF}/2$ |
| 1 | 1 | $\pm V_{REF}$ |

Table 3. Clock and Power-Down Selection

| PD1 | PD0 | DEVICE MODE |
|-----|-----|---|
| 0 | 0 | Normal Operation / External Clock Mode |
| 0 | 1 | Normal Operation / Internal Clock Mode |
| 1 | 0 | Standby Power-Down (STBYPD); clock mode is unaffected |
| 1 | 1 | Full Power-Down (FULLPD); clock mode is unaffected |

Table 4. Channel Selection

| A2 | A1 | A0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 |
|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | * | | | | | | | |
| 0 | 0 | 1 | | * | | | | | | |
| 0 | 1 | 0 | | | * | | | | | |
| 0 | 1 | 1 | | | | * | | | | |
| 1 | 0 | 0 | | | | | * | | | |
| 1 | 0 | 1 | | | | | | * | | |
| 1 | 1 | 0 | | | | | | | * | |
| 1 | 1 | 1 | | | | | | | | * |

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Table 5. Data-Bus Output

| PIN | HBEN = LOW | HBEN = HIGH |
|-----|------------|-----------------------------|
| D0 | B0 (LSB) | B8 |
| D1 | B1 | B9 |
| D2 | B2 | B10 |
| D3 | B3 | B11 (MSB) |
| D4 | B4 | B11 (BIP = 1) / 0 (BIP = 0) |
| D5 | B5 | B11 (BIP = 1) / 0 (BIP = 0) |
| D6 | B6 | B11 (BIP = 1) / 0 (BIP = 0) |
| D7 | B7 | B11 (BIP = 1) / 0 (BIP = 0) |

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX199 for either unipolar or bipolar input range. A write pulse (\overline{WR} + \overline{CS}) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during the conversion cycle will abort the conversion in progress and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval ($3\mu s$ with $f_{CLK} = 2MHz$) ends. See Figure 5.

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on \overline{WR} 's rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode*).

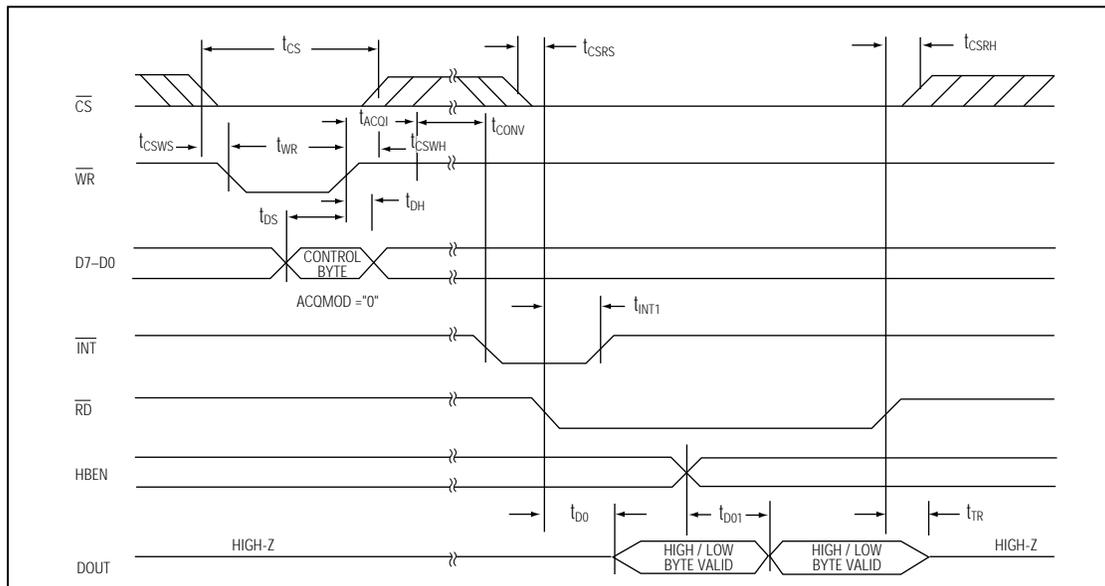


Figure 5. Conversion Timing Using Internal Acquisition Mode

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

MAX199

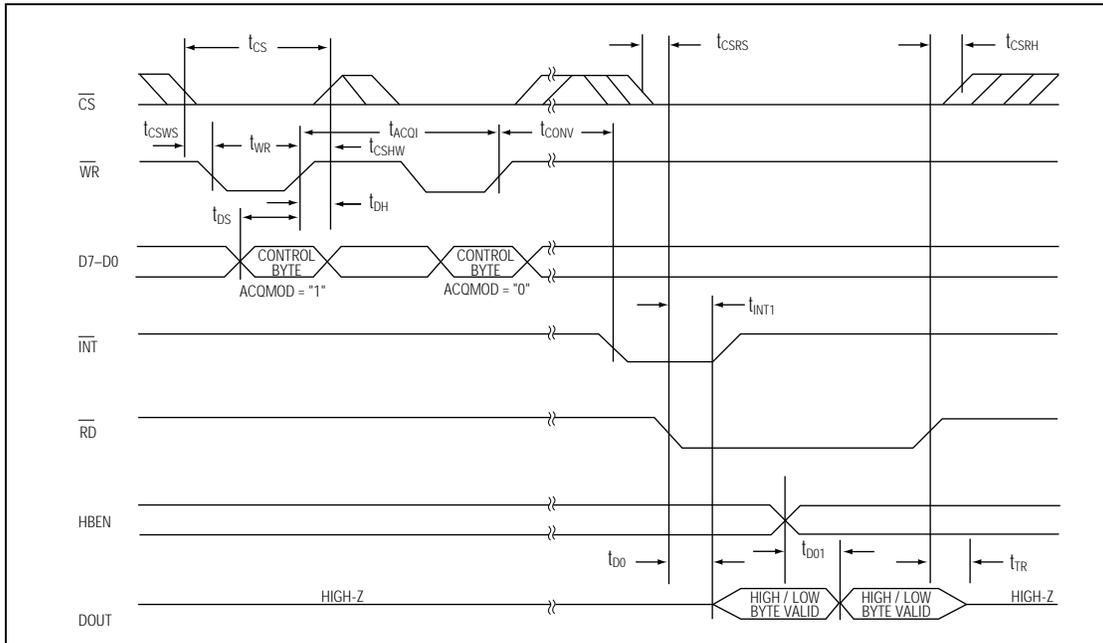


Figure 6. Conversion Timing Using External Acquisition Mode

How to Read a Conversion

A standard interrupt signal, $\overline{\text{INT}}$, is provided to allow the device to flag the μP when the conversion has ended and a valid result is available. $\overline{\text{INT}}$ goes low when the conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

Clock Modes

The MAX199 operates with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, the MAX199 defaults to external clock mode.

Internal Clock Mode

Select internal clock mode to free the μP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7

shows a linear relationship between the internal clock period and the value of the external capacitor used.

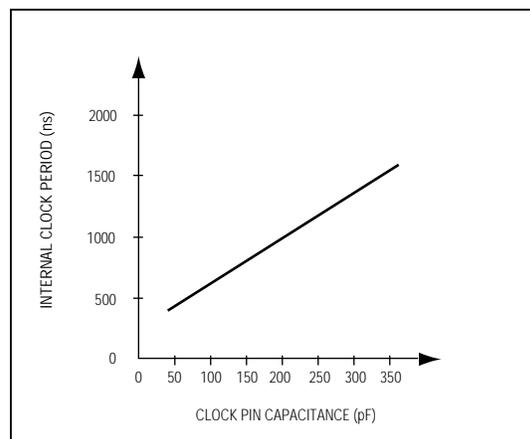


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and \overline{WR} timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz

external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

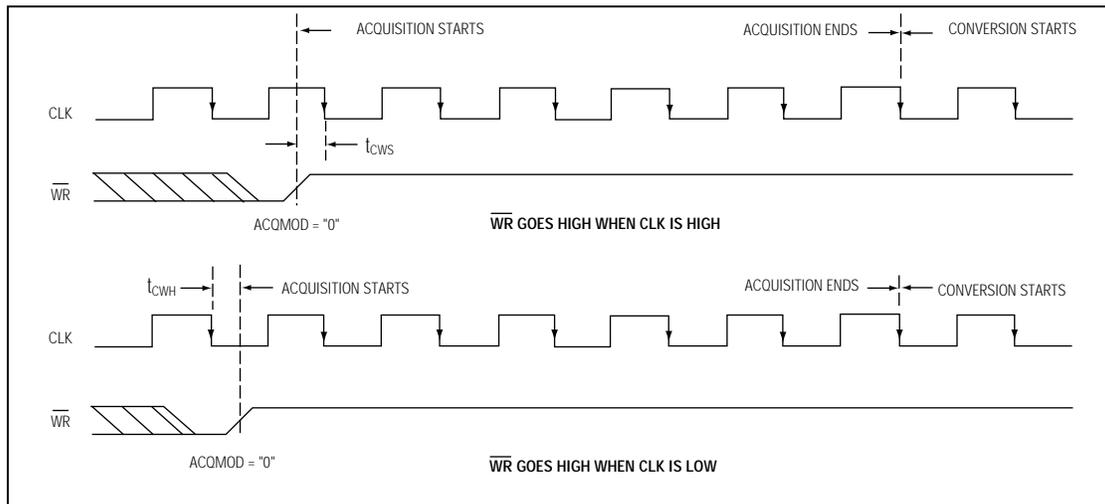


Figure 8a. External Clock and \overline{WR} Timing (Internal Acquisition Mode)

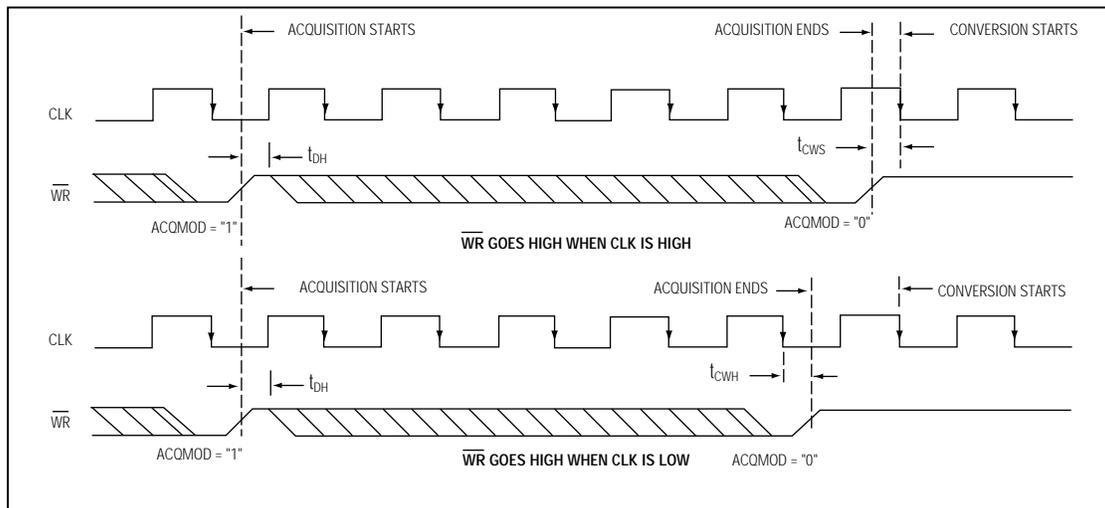


Figure 8b. External Clock and \overline{WR} Timing (External Acquisition Mode)

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

MAX199

Applications Information

Power-On Reset

At power-up, the internal power-supply circuitry sets \overline{INT} high and puts the device in normal operation / external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX199 can operate with either an internal or external reference. An external reference can be connected to either the REF pin or to the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD} . Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a $0.01\mu F$ capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a $4.7\mu F$ capacitor to AGND and the REFADJ pin with a $0.01\mu F$ capacitor to AGND. The internal reference voltage is adjustable to $\pm 1.5\%$ (± 65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of $10k\Omega$ for DC currents. During conversions, an

external reference at REF must be able to deliver $400\mu A$ DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass it close to the REF pin with a $4.7\mu F$ capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value ($FS / 4096$) results in performance degradation (loss of effective bits).

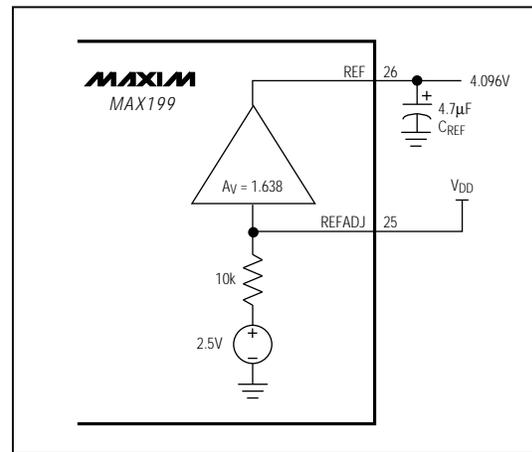


Figure 9b. External Reference at REF

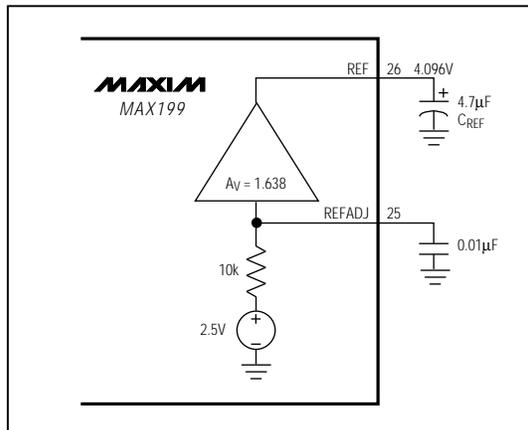


Figure 9a. Internal Reference

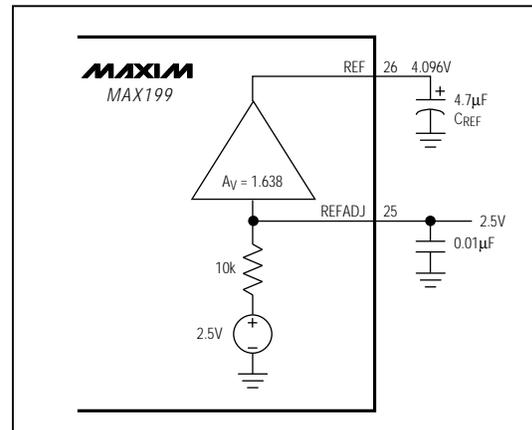


Figure 9c. The external reference at REFADJ overdrives the internal reference.

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first \overline{WR} falling edge during a write operation.

For hardware-controlled (FULLPD) power-down, pull the \overline{SHDN} pin low. When hardware shutdown is asserted, it becomes effective immediately and the conversion is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the $4.7\mu\text{F}$ capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a $33\mu\text{F}$ capacitor between REF and AGND to maintain the reference voltage between conversion and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows a conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate and add $50\mu\text{s}$ for settling time. Throughput rates of 10ksps offer typical supply currents of $470\mu\text{A}$, using the recommended $33\mu\text{F}$ capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX199 down after each conversion without requiring any start-up time on the next conversion.

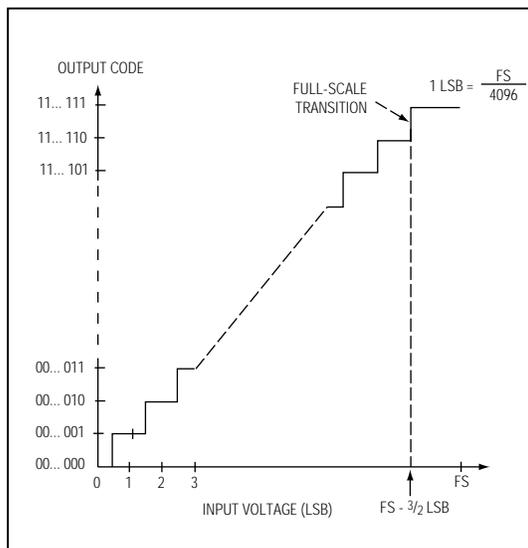


Figure 10. Unipolar Transfer Function

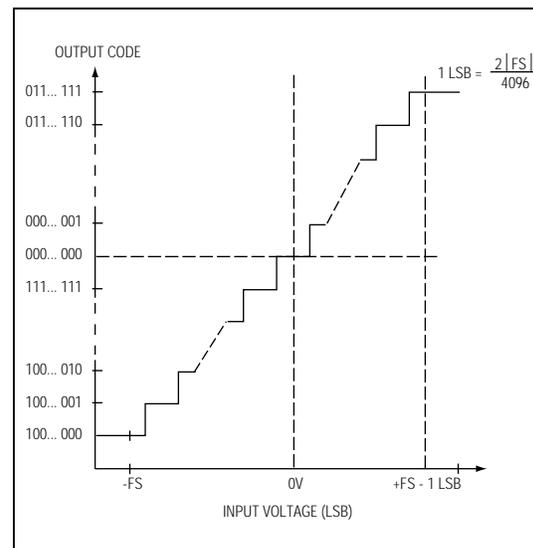


Figure 11. Bipolar Transfer Function

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

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Transfer Function

Output data coding for the MAX199 is binary in unipolar mode with $1\text{LSB} = (\text{FS} / 4096)$ and twos-complement binary in bipolar mode with $1\text{LSB} = [(2 \times |\text{FS}|) / 4096]$. Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

Layout, Grounding, and Bypassing

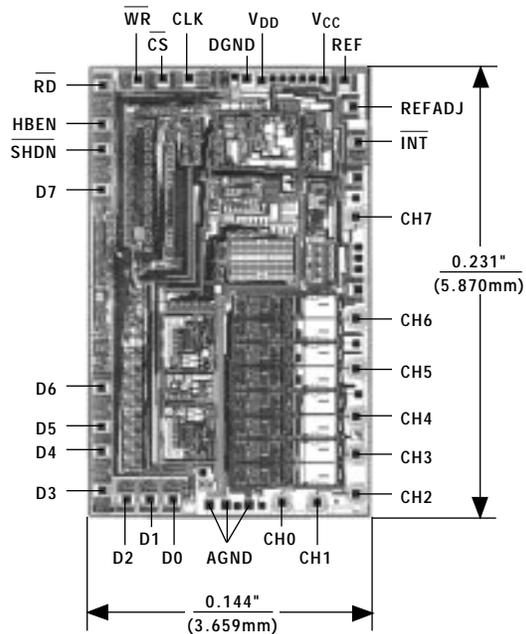
Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with $0.1\mu\text{F}$ and $4.7\mu\text{F}$ capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD} , as shown in Figure 12.

Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|-----------------|------------------------|
| MAX199AENI | -40°C to +85°C | 28 Narrow Plastic DIP |
| MAX199BENI | -40°C to +85°C | 28 Narrow Plastic DIP |
| MAX199AEWI | -40°C to +85°C | 28 Wide SO |
| MAX199BEWI | -40°C to +85°C | 28 Wide SO |
| MAX199AEAI | -40°C to +85°C | 28 SSOP |
| MAX199BEAI | -40°C to +85°C | 28 SSOP |
| MAX199AMYI | -55°C to +125°C | 28 Narrow Ceramic SB** |
| MAX199BMYI | -55°C to +125°C | 28 Narrow Ceramic SB** |

** Contact factory for availability and processing to MIL-STD-883.

Chip Topography



TRANSISTOR COUNT: 2956

SUBSTRATE CONNECTED TO GND

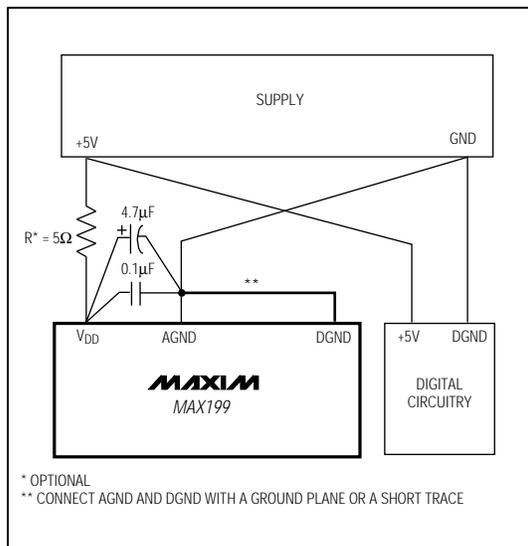
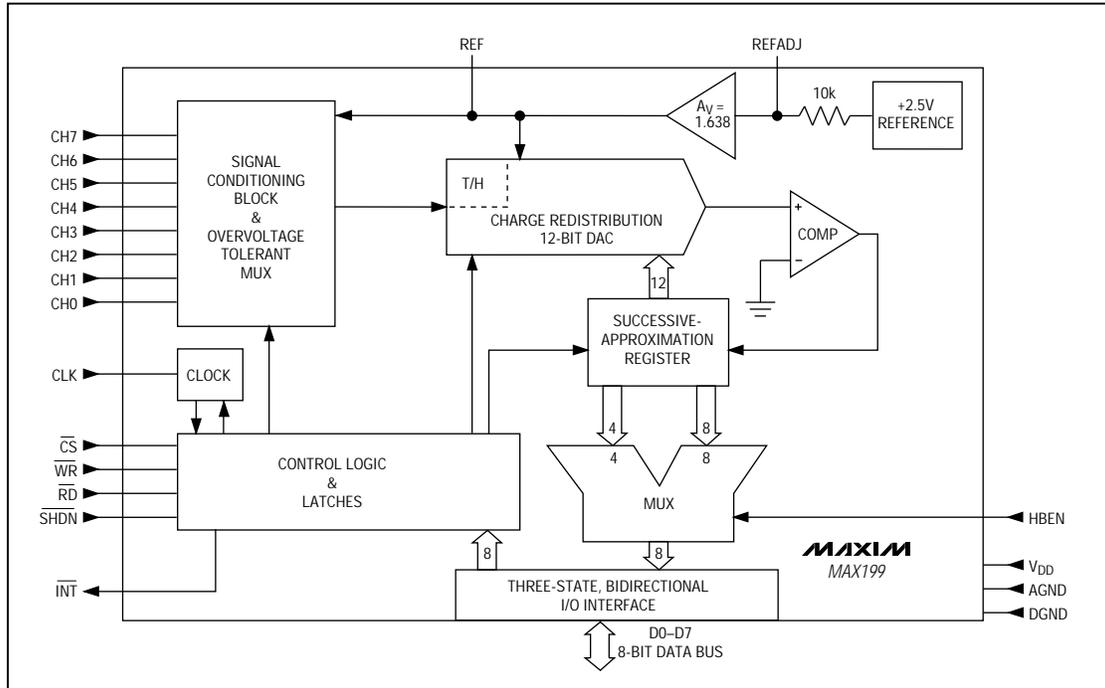


Figure 12. Power-Supply Grounding Connection

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Functional Diagram

MAX199



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